

UG1185 (v2015.2) July 26, 2015

Feature Summary

The SDSoc™ (Software-Defined System On Chip) environment is an Eclipse-based Integrated Development Environment (IDE) for implementing heterogeneous embedded systems using the Zynq®-7000 All Programmable SoC platform. Designed for software engineers and system architects, the SDSoc environment provides an embedded C/C++ application development experience with an easy-to-use Eclipse IDE and comprehensive design tools for heterogeneous Zynq SoC development.

The SDSoc environment includes a full-system optimizing C/C++ compiler that provides automated software acceleration in programmable logic, combined with automated system connectivity generation. The application programming model within the SDSoc environment is intuitive to software engineers. Working in the SDSoc environment, you do the following:

- Write an application as C/C++ code
- Identify a target platform
- Specify a subset of the functions within the application that is to be compiled into hardware

The SDSoc system compiler then compiles the application into hardware and software to realize the complete embedded system implemented on a Zynq device, including a complete boot image with firmware, operating system, and application executable.

System Compiler

- Automatic data motion network generation from C/C++ application code, including datamover IP generation and integration of AXI DMA, 2D-DMA, SGDMA, AXI FIFO, and direct memory accesses
- Supports cache coherent (ACP) and high-performance (HP) processing system / programmable logic fabric AXI interfaces
- Supports configuration of all software drivers for the data motion network
- Supports hardware pipelines with IP to IP direct connections
- Multiple clock support for accelerator IPs
- Automatic inference of accelerator hardware interfaces

User Interfaces

- Eclipse-based IDE flows for system compilation, debugging, and performance estimation
- Project view to specify hardware functions and select clocks

- One-click partition of a function to hardware or software
- Command line interface/makefile flows

Debug

- All debugging features of the Xilinx® SDK debug
- Automatic debug environment setup for SDSoC project

Performance Estimation and Measurement

- Automatic software instrumentation to measure performance
- Fast performance estimation without synthesis, placement, and routing
- Expedited analysis between software-only and hardware-accelerated versions
- Run-time measurement and visualization of HP and ACP bus activities using AXI Performance Monitor (APM)

Software run-time

- Supports Linux and baremetal applications
- Supports FreeRTOS (beta)
- Linux kernel and userspace support for Linux V4L2 and DRM managed buffers

Sample programs

- Motion detection
- Matrix multiply and addition (many variations)
- File I/O video processing
- FIR filter (using C-callable HDL IP)
- Arraycopy (using C-callable HDL IP)
- Motion-adaptive noise reduction and Sobel filter video processing

Built-in Platforms

- ZC702
- ZC706
- ZC706_mem
- Zedboard
- Microzed
- ZYBO
- ZC702_HDMI (sample)

- Zedboard OSD (sample)
- ZC702 OSD (sample)
- ZC702 ACP (teaching example)

Documentation

- *SDSoC Environment Getting Started*, installation and tutorials ([UG1028](#))
- *SDSoC Environment User Guide* ([UG1027](#))
- *SDSoC Environment Platform and Libraries* ([UG1146](#))

Find the following at <install>/SDSoC/2015.2/docs:

- ZC702_HDMI: Sample vision platforms and sample applications
- ZC706_mem: ZC706 platform with MIG controller for external DDR

Host OS support

- Red Hat Enterprise Workstation 6.4, 6.5, 6.6 and 7 (64-bit)
- Windows 7 Professional (64-bit)
- Ubuntu 14.04 LTS (64-bit)

Known Issues

See [Answer Record 64998](#).

Revision History

The following table shows the revision history for this document:

Date	Version	Revisions
07/26/2015	2015.2	Fixed minor formatting error. No content changes.
07/20/2015	2015.2	Initial Xilinx release.

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