

Virtex-5 Libraries Guide for Schematic Designs

UG622 (v 11.3) September 16, 2009

Xilinx Trademarks and Copyright Information



Xilinx is disclosing this user guide, manual, release note, and/or specification (the “Documentation”) to you solely for use in the development of designs to operate with Xilinx hardware devices. You may not reproduce, distribute, republish, download, display, post, or transmit the Documentation in any form or by any means including, but not limited to, electronic, mechanical, photocopying, recording, or otherwise, without the prior written consent of Xilinx. Xilinx expressly disclaims any liability arising out of your use of the Documentation. Xilinx reserves the right, at its sole discretion, to change the Documentation without notice at any time. Xilinx assumes no obligation to correct any errors contained in the Documentation, or to advise you of any corrections or updates. Xilinx expressly disclaims any liability in connection with technical support or assistance that may be provided to you in connection with the Information.

THE DOCUMENTATION IS DISCLOSED TO YOU “AS-IS” WITH NO WARRANTY OF ANY KIND. XILINX MAKES NO OTHER WARRANTIES, WHETHER EXPRESS, IMPLIED, OR STATUTORY, REGARDING THE DOCUMENTATION, INCLUDING ANY WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NONINFRINGEMENT OF THIRD-PARTY RIGHTS. IN NO EVENT WILL XILINX BE LIABLE FOR ANY CONSEQUENTIAL, INDIRECT, EXEMPLARY, SPECIAL, OR INCIDENTAL DAMAGES, INCLUDING ANY LOSS OF DATA OR LOST PROFITS, ARISING FROM YOUR USE OF THE DOCUMENTATION.

© Copyright 2002-2009 Xilinx Inc. All Rights Reserved. XILINX, the Xilinx logo, the Brand Window and other designated brands included herein are trademarks of Xilinx, Inc. All other trademarks are the property of their respective owners.

Table of Contents

Xilinx Trademarks and Copyright Information.....	2
Chapter 1 About this Guide.....	45
About Design Elements.....	45
Chapter 2 Design Element Retargeting.....	47
Chapter 3 Functional Categories.....	51
Chapter 4 About Design Elements.....	69
ACC16.....	70
Introduction.....	70
Logic Table.....	71
Design Entry Method.....	71
For More Information.....	71
ACC4.....	72
Introduction.....	72
Logic Table.....	73
Design Entry Method.....	73
For More Information.....	73
ACC8.....	74
Introduction.....	74
Logic Table.....	75
Design Entry Method.....	75
For More Information.....	75
ADD16.....	76
Introduction.....	76
Logic Table.....	76
Design Entry Method.....	76
For More Information.....	76
ADD4.....	77
Introduction.....	77
Logic Table.....	77
Design Entry Method.....	77
For More Information.....	77
ADD8.....	78
Introduction.....	78
Logic Table.....	78
Design Entry Method.....	78
For More Information.....	78
ADSU16.....	79
Introduction.....	79
Logic Table.....	79
Design Entry Method.....	80
For More Information.....	80
ADSU4.....	81
Introduction.....	81
Logic Table.....	81
Design Entry Method.....	82
For More Information.....	82
ADSU8.....	83
Introduction.....	83
Logic Table.....	83
Design Entry Method.....	84
For More Information.....	84
AND12.....	85
Introduction.....	85
Design Entry Method.....	85
For More Information.....	85

AND16.....	86
Introduction.....	86
Design Entry Method	86
For More Information.....	86
AND2	87
Introduction.....	87
Design Entry Method	87
For More Information.....	87
AND2B1.....	88
Introduction.....	88
Design Entry Method	88
For More Information.....	88
AND2B2.....	89
Introduction.....	89
Design Entry Method	89
For More Information.....	89
AND3	90
Introduction.....	90
Design Entry Method	90
For More Information.....	90
AND3B1.....	91
Introduction.....	91
Design Entry Method	91
For More Information.....	91
AND3B2.....	92
Introduction.....	92
Design Entry Method	92
For More Information.....	92
AND3B3.....	93
Introduction.....	93
Design Entry Method	93
For More Information.....	93
AND4	94
Introduction.....	94
Design Entry Method	94
For More Information.....	94
AND4B1.....	95
Introduction.....	95
Design Entry Method	95
For More Information.....	95
AND4B2.....	96
Introduction.....	96
Design Entry Method	96
For More Information.....	96
AND4B3.....	97
Introduction.....	97
Design Entry Method	97
For More Information.....	97
AND4B4.....	98
Introduction.....	98
Design Entry Method	98
For More Information.....	98
AND5	99
Introduction.....	99
Design Entry Method	99
For More Information.....	99
AND5B1.....	100
Introduction.....	100
Design Entry Method	100

For More Information.....	100
AND5B2.....	101
Introduction.....	101
Design Entry Method	101
For More Information.....	101
AND5B3.....	102
Introduction.....	102
Design Entry Method	102
For More Information.....	102
AND5B4.....	103
Introduction.....	103
Design Entry Method	103
For More Information.....	103
AND5B5.....	104
Introduction.....	104
Design Entry Method	104
For More Information.....	104
AND6	105
Introduction.....	105
Design Entry Method	105
For More Information.....	105
AND7	106
Introduction.....	106
Design Entry Method	106
For More Information.....	106
AND8	107
Introduction.....	107
Design Entry Method	107
For More Information.....	107
AND9	108
Introduction.....	108
Design Entry Method	108
For More Information.....	108
BRLSHFT4	109
Introduction.....	109
Logic Table	109
Design Entry Method	109
For More Information.....	109
BRLSHFT8	110
Introduction.....	110
Logic Table	110
Design Entry Method	110
For More Information.....	110
BSCAN_VIRTEX5.....	111
Introduction.....	111
Port Descriptions.....	111
Design Entry Method	111
Available Attributes	111
For More Information.....	112
BUF	113
Introduction.....	113
Design Entry Method	113
For More Information.....	113
BUFCF	114
Introduction.....	114
Design Entry Method	114
For More Information.....	114
BUFG.....	115
Introduction.....	115

Port Descriptions.....	115
Design Entry Method	115
For More Information.....	115
BUFGCE	116
Introduction.....	116
Logic Table	116
Design Entry Method	116
For More Information.....	116
BUFGCE_1	117
Introduction.....	117
Logic Table	117
Design Entry Method	117
For More Information.....	117
BUFGCTRL	118
Introduction.....	118
Port Descriptions.....	118
Design Entry Method	118
Available Attributes	119
For More Information.....	119
BUFGMUX_CTRL.....	120
Introduction.....	120
Port Descriptions.....	120
Design Entry Method	120
For More Information.....	120
BUFIO.....	121
Introduction.....	121
Port Descriptions.....	121
Design Entry Method	121
For More Information.....	121
BUFR	122
Introduction.....	122
Port Descriptions.....	122
Design Entry Method	122
Available Attributes	122
For More Information.....	122
CAPTURE_VIRTEX5.....	123
Introduction.....	123
Port Descriptions.....	123
Design Entry Method	123
Available Attributes	123
For More Information.....	123
CARRY4.....	124
Introduction.....	124
Port Descriptions.....	124
Design Entry Method	124
For More Information.....	124
CB16CE.....	125
Introduction.....	125
Logic Table	125
Design Entry Method	125
For More Information.....	125
CB16CLE.....	126
Introduction.....	126
Logic Table	127
Design Entry Method	127
For More Information.....	127
CB16CLED	128
Introduction.....	128
Logic Table	128

Design Entry Method	129
For More Information	129
CB16RE	130
Introduction.....	130
Logic Table	130
Design Entry Method	130
For More Information	130
CB2CE	131
Introduction.....	131
Logic Table	131
Design Entry Method	131
For More Information	131
CB2CLE	132
Introduction.....	132
Logic Table	132
Design Entry Method	132
For More Information	133
CB2CLED.....	134
Introduction.....	134
Logic Table	134
Design Entry Method	135
For More Information	135
CB2RE.....	136
Introduction.....	136
Logic Table	136
Design Entry Method	136
For More Information	136
CB4CE	137
Introduction.....	137
Logic Table	137
Design Entry Method	137
For More Information	137
CB4CLE	138
Introduction.....	138
Logic Table	138
Design Entry Method	138
For More Information	139
CB4CLED.....	140
Introduction.....	140
Logic Table	141
Design Entry Method	141
For More Information	141
CB4RE.....	142
Introduction.....	142
Logic Table	142
Design Entry Method	142
For More Information	142
CB8CE	143
Introduction.....	143
Logic Table	143
Design Entry Method	143
For More Information	143
CB8CLE	144
Introduction.....	144
Logic Table	145
Design Entry Method	145
For More Information	145
CB8CLED.....	146
Introduction.....	146

Logic Table	146
Design Entry Method	147
For More Information.....	147
CB8RE.....	148
Introduction.....	148
Logic Table	148
Design Entry Method	148
For More Information.....	148
CC16CE	149
Introduction.....	149
Logic Table	149
Design Entry Method	149
For More Information.....	149
CC16CLE	150
Introduction.....	150
Logic Table	150
Design Entry Method	150
For More Information.....	151
CC16CLED.....	152
Introduction.....	152
Logic Table	152
Design Entry Method	153
For More Information.....	153
CC16RE.....	154
Introduction.....	154
Logic Table	154
Design Entry Method	154
For More Information.....	154
CC8CE	155
Introduction.....	155
Logic Table	155
Design Entry Method	155
For More Information.....	155
CC8CLE	156
Introduction.....	156
Logic Table	156
Design Entry Method	156
For More Information.....	157
CC8CLED	158
Introduction.....	158
Logic Table	158
Design Entry Method	159
For More Information.....	159
CC8RE	160
Introduction.....	160
Logic Table	160
Design Entry Method	160
For More Information.....	160
CD4CE.....	161
Introduction.....	161
Logic Table	162
Design Entry Method	162
For More Information.....	162
CD4CLE.....	163
Introduction.....	163
Logic Table	164
Design Entry Method	164
For More Information.....	164
CD4RE	165

Introduction.....	165
Logic Table	166
Design Entry Method	166
For More Information.....	166
CD4RLE.....	167
Introduction.....	167
Logic Table	168
Design Entry Method	168
For More Information.....	168
CFGLUT5.....	169
Introduction.....	169
Port Descriptions.....	169
Design Entry Method	169
Available Attributes	170
For More Information.....	170
CJ4CE	171
Introduction.....	171
Logic Table	171
Design Entry Method	171
For More Information.....	171
CJ4RE	172
Introduction.....	172
Logic Table	172
Design Entry Method	172
For More Information.....	172
CJ5CE	173
Introduction.....	173
Logic Table	173
Design Entry Method	173
For More Information.....	173
CJ5RE	174
Introduction.....	174
Logic Table	174
Design Entry Method	174
For More Information.....	174
CJ8CE	175
Introduction.....	175
Logic Table	175
Design Entry Method	175
For More Information.....	175
CJ8RE	176
Introduction.....	176
Logic Table	176
Design Entry Method	176
For More Information.....	176
COMP16	177
Introduction.....	177
Design Entry Method	177
For More Information.....	177
COMP2	178
Introduction.....	178
Design Entry Method	178
For More Information.....	178
COMP4	179
Introduction.....	179
Design Entry Method	179
For More Information.....	179
COMP8	180
Introduction.....	180

Design Entry Method	180
For More Information	180
COMPM16	181
Introduction.....	181
Logic Table	181
Design Entry Method	181
For More Information	182
COMPM2.....	183
Introduction.....	183
Logic Table	183
Design Entry Method	183
For More Information	183
COMPM4.....	184
Introduction.....	184
Logic Table	184
Design Entry Method	184
For More Information	184
COMPM8.....	185
Introduction.....	185
Logic Table	185
Design Entry Method	185
For More Information	186
COMPMC16.....	187
Introduction.....	187
Logic Table	187
Design Entry Method	187
For More Information	188
COMPMC8	189
Introduction.....	189
Logic Table	189
Design Entry Method	189
For More Information	190
CRC32.....	191
Introduction.....	191
Port Descriptions.....	191
Design Entry Method	191
Available Attributes	192
For More Information	192
CRC64.....	193
Introduction.....	193
Port Descriptions.....	193
Design Entry Method	194
Available Attributes	194
For More Information	194
D2_4E	195
Introduction.....	195
Logic Table	195
Design Entry Method	195
For More Information	195
D3_8E	196
Introduction.....	196
Logic Table	196
Design Entry Method	196
For More Information	196
D4_16E.....	197
Introduction.....	197
Design Entry Method	197
For More Information	197
DCIRESET.....	198

Introduction.....	198
Port Descriptions.....	198
Design Entry Method	198
Available Attributes	198
For More Information.....	198
DCM_ADV	199
Introduction.....	199
Port Descriptions.....	199
Design Entry Method	202
Available Attributes	202
For More Information.....	203
DCM_BASE.....	204
Introduction.....	204
Port Descriptions.....	204
Design Entry Method	206
Available Attributes	206
For More Information.....	207
DCM_PS	208
Introduction.....	208
Port Descriptions.....	208
Design Entry Method	210
Available Attributes	210
For More Information.....	211
DEC_CC16.....	212
Introduction.....	212
Logic Table	212
Design Entry Method	212
For More Information.....	213
DEC_CC4.....	214
Introduction.....	214
Logic Table	214
Design Entry Method	214
For More Information.....	214
DEC_CC8.....	215
Introduction.....	215
Logic Table	215
Design Entry Method	215
For More Information.....	215
DSP48E	216
Introduction.....	216
Port Descriptions.....	216
Design Entry Method	219
Available Attributes	219
For More Information.....	220
FD	221
Introduction.....	221
Logic Table	221
Design Entry Method	221
Available Attributes	221
For More Information.....	221
FD_1	222
Introduction.....	222
Logic Table	222
Design Entry Method	222
Available Attributes	222
For More Information.....	222
FD16CE.....	223
Introduction.....	223
Logic Table	223

Design Entry Method	223
Available Attributes	223
For More Information.....	223
FD16RE	224
Introduction.....	224
Logic Table	224
Design Entry Method	224
Available Attributes	224
For More Information.....	224
FD4CE	225
Introduction.....	225
Logic Table	225
Design Entry Method	225
Available Attributes	225
For More Information.....	225
FD4RE	226
Introduction.....	226
Logic Table	226
Design Entry Method	226
Available Attributes	226
For More Information.....	226
FD8CE	227
Introduction.....	227
Logic Table	227
Design Entry Method	227
Available Attributes	227
For More Information.....	227
FD8RE	228
Introduction.....	228
Logic Table	228
Design Entry Method	228
Available Attributes	228
For More Information.....	228
FDC	229
Introduction.....	229
Logic Table	229
Design Entry Method	229
Available Attributes	229
For More Information.....	229
FDC_1.....	230
Introduction.....	230
Logic Table	230
Design Entry Method	230
Available Attributes	230
For More Information.....	230
FDCE	231
Introduction.....	231
Logic Table	231
Design Entry Method	231
Available Attributes	231
For More Information.....	231
FDCE_1.....	232
Introduction.....	232
Logic Table	232
Design Entry Method	232
Available Attributes	232
For More Information.....	232
FDCP	233
Introduction.....	233

Logic Table	233
Design Entry Method	233
Available Attributes	233
For More Information.....	233
FDCP_1.....	234
Introduction.....	234
Logic Table	234
Design Entry Method	234
Available Attributes	234
For More Information.....	234
FDCPE.....	235
Introduction.....	235
Logic Table	235
Port Descriptions.....	235
Design Entry Method	236
Available Attributes	236
For More Information.....	236
FDCPE_1.....	237
Introduction.....	237
Logic Table	237
Port Descriptions.....	237
Design Entry Method	237
Available Attributes	238
For More Information.....	238
FDE	239
Introduction.....	239
Logic Table	239
Design Entry Method	239
Available Attributes	239
For More Information.....	239
FDE_1	240
Introduction.....	240
Logic Table	240
Design Entry Method	240
Available Attributes	240
For More Information.....	240
FDP	241
Introduction.....	241
Logic Table	241
Design Entry Method	241
Available Attributes	241
For More Information.....	241
FDP_1	242
Introduction.....	242
Logic Table	242
Design Entry Method	242
Available Attributes	242
For More Information.....	242
FDPE	243
Introduction.....	243
Logic Table	243
Design Entry Method	243
Available Attributes	243
For More Information.....	243
FDPE_1	244
Introduction.....	244
Logic Table	244
Design Entry Method	244
Available Attributes	244

For More Information	244
FDR	245
Introduction.....	245
Logic Table	245
Design Entry Method	245
Available Attributes	245
For More Information.....	245
FDR_1	246
Introduction.....	246
Logic Table	246
Design Entry Method	246
Available Attributes	246
For More Information.....	246
FDRE	247
Introduction.....	247
Logic Table	247
Design Entry Method	247
Available Attributes	247
For More Information.....	247
FDRE_1	248
Introduction.....	248
Logic Table	248
Design Entry Method	248
Available Attributes	248
For More Information.....	248
FDRS	249
Introduction.....	249
Logic Table	249
Design Entry Method	249
Available Attributes	249
For More Information.....	249
FDRS_1	250
Introduction.....	250
Logic Table	250
Design Entry Method	250
Available Attributes	250
For More Information.....	250
FDRSE	251
Introduction.....	251
Logic Table	251
Design Entry Method	251
Available Attributes	251
For More Information.....	251
FDRSE_1	252
Introduction.....	252
Logic Table	252
Design Entry Method	252
Available Attributes	252
For More Information.....	252
FDS	253
Introduction.....	253
Logic Table	253
Design Entry Method	253
Available Attributes	253
For More Information.....	253
FDS_1	254
Introduction.....	254
Logic Table	254
Design Entry Method	254

Available Attributes	254
For More Information	254
FDSE	255
Introduction	255
Logic Table	255
Design Entry Method	255
Available Attributes	255
For More Information	255
FDSE_1	256
Introduction	256
Logic Table	256
Design Entry Method	256
Available Attributes	256
For More Information	256
FIFO18	257
Introduction	257
Port Descriptions	257
Design Entry Method	258
Available Attributes	258
For More Information	259
FIFO18_36	260
Introduction	260
Port Descriptions	260
Design Entry Method	261
Available Attributes	261
For More Information	262
FIFO36	263
Introduction	263
Port Descriptions	263
Design Entry Method	264
Available Attributes	265
For More Information	265
FIFO36_72	266
Introduction	266
Port Descriptions	266
Design Entry Method	267
Available Attributes	268
For More Information	268
FJKC	269
Introduction	269
Logic Table	269
Design Entry Method	269
Available Attributes	269
For More Information	269
FJKCE	270
Introduction	270
Logic Table	270
Design Entry Method	270
Available Attributes	270
For More Information	270
FJKP	271
Introduction	271
Logic Table	271
Design Entry Method	271
Available Attributes	271
For More Information	271
FJKPE	272
Introduction	272
Logic Table	272

Design Entry Method	272
Available Attributes	272
For More Information.....	273
FJKRSE	274
Introduction.....	274
Logic Table	274
Design Entry Method	274
Available Attributes	274
For More Information.....	275
FJKSRE	276
Introduction.....	276
Logic Table	276
Design Entry Method	276
Available Attributes	276
For More Information.....	277
FRAME_ECC_VIRTEX5	278
Introduction.....	278
Port Descriptions.....	278
Design Entry Method	278
For More Information.....	278
FTC.....	279
Introduction.....	279
Logic Table	279
Design Entry Method	279
Available Attributes	279
For More Information.....	279
FTCE.....	280
Introduction.....	280
Logic Table	280
Design Entry Method	280
Available Attributes	280
For More Information.....	280
FTCLE	281
Introduction.....	281
Logic Table	281
Design Entry Method	281
Available Attributes	281
For More Information.....	281
FTCLEX	282
Introduction.....	282
Logic Table	282
Design Entry Method	282
Available Attributes	282
For More Information.....	282
FTP	283
Introduction.....	283
Logic Table	283
Design Entry Method	283
Available Attributes	283
For More Information.....	283
FTPE.....	284
Introduction.....	284
Logic Table	284
Design Entry Method	284
Available Attributes	284
For More Information.....	284
FTPLE.....	285
Introduction.....	285
Logic Table	285

Design Entry Method	285
Available Attributes	285
For More Information.....	286
FTRSE	287
Introduction.....	287
Logic Table	287
Design Entry Method	287
Available Attributes	287
For More Information.....	287
FTRSLE	288
Introduction.....	288
Logic Table	288
Design Entry Method	288
Available Attributes	288
For More Information.....	289
FTSRE	290
Introduction.....	290
Logic Table	290
Design Entry Method	290
Available Attributes	290
For More Information.....	290
FTSRLE	291
Introduction.....	291
Logic Table	291
Design Entry Method	291
Available Attributes	291
For More Information.....	292
GND	293
Introduction.....	293
Design Entry Method	293
For More Information.....	293
GTP_DUAL	294
Introduction.....	295
Design Entry Method	296
For More Information.....	296
GTX_DUAL	297
Introduction.....	301
Design Entry Method	301
For More Information.....	301
IBUF	302
Introduction.....	302
Port Descriptions.....	302
Design Entry Method	302
Available Attributes	302
For More Information.....	302
IBUF16.....	303
Introduction.....	303
Design Entry Method	303
Available Attributes	303
For More Information.....	303
IBUF4.....	304
Introduction.....	304
Design Entry Method	304
Available Attributes	304
For More Information.....	304
IBUF8.....	305
Introduction.....	305
Design Entry Method	305
Available Attributes	305

For More Information.....	305
IBUFDS.....	306
Introduction.....	306
Logic Table	306
Port Descriptions.....	306
Design Entry Method	306
Available Attributes	306
For More Information.....	307
IBUFG.....	308
Introduction.....	308
Port Descriptions.....	308
Design Entry Method	308
Available Attributes	308
For More Information.....	308
IBUFGDS	309
Introduction.....	309
Logic Table	309
Port Descriptions.....	309
Design Entry Method	309
Available Attributes	309
For More Information.....	310
ICAP_VIRTEX5	311
Introduction.....	311
Port Descriptions.....	311
Design Entry Method	311
Available Attributes	311
For More Information.....	311
IDDR	312
Introduction.....	312
Port Descriptions.....	312
Design Entry Method	313
Available Attributes	313
For More Information.....	313
IDDR_2CLK	314
Introduction.....	314
Port Descriptions.....	314
Design Entry Method	315
Available Attributes	315
For More Information.....	315
IDELAY.....	316
Introduction.....	316
Port Descriptions.....	316
Design Entry Method	318
Available Attributes	318
For More Information.....	318
IDELAYCTRL.....	319
Introduction.....	319
Port Descriptions.....	319
Design Entry Method	319
For More Information.....	319
IFD	320
Introduction.....	320
Logic Table	320
Design Entry Method	320
For More Information.....	320
IFD_1.....	321
Introduction.....	321
Logic Table	321
Design Entry Method	321

For More Information	321
IFD16	322
Introduction.....	322
Logic Table	322
Design Entry Method	322
For More Information	322
IFD4.....	323
Introduction.....	323
Logic Table	323
Design Entry Method	323
For More Information.....	323
IFD8.....	324
Introduction.....	324
Logic Table	324
Design Entry Method	324
For More Information.....	324
IFDI	325
Introduction.....	325
Logic Table	325
Design Entry Method	325
For More Information.....	325
IFDI_1.....	326
Introduction.....	326
Logic Table	326
Design Entry Method	326
For More Information.....	326
IFDX	327
Introduction.....	327
Logic Table	327
Design Entry Method	327
For More Information.....	327
IFDX_1.....	328
Introduction.....	328
Logic Table	328
Design Entry Method	328
For More Information.....	328
IFDX16.....	329
Introduction.....	329
Logic Table	329
Design Entry Method	329
For More Information.....	329
IFDX4	330
Introduction.....	330
Logic Table	330
Design Entry Method	330
For More Information.....	330
IFDX8	331
Introduction.....	331
Logic Table	331
Design Entry Method	331
For More Information.....	331
ILD	332
Introduction.....	332
Logic Table	332
Design Entry Method	332
For More Information.....	332
ILD_1.....	333
Introduction.....	333
Logic Table	333

Design Entry Method	333
For More Information	333
ILD16	334
Introduction	334
Logic Table	334
Design Entry Method	334
For More Information	334
ILD4	335
Introduction	335
Logic Table	335
Design Entry Method	335
For More Information	335
ILD8	336
Introduction	336
Logic Table	336
Design Entry Method	336
For More Information	336
ILDI	337
Introduction	337
Logic Table	337
Design Entry Method	337
For More Information	337
ILDI_1	338
Introduction	338
Logic Table	338
Design Entry Method	338
For More Information	338
ILDXI	339
Introduction	339
Logic Table	339
Design Entry Method	339
For More Information	339
ILDXI_1	340
Introduction	340
Logic Table	340
Design Entry Method	340
For More Information	340
INV	341
Introduction	341
Design Entry Method	341
For More Information	341
INV16	342
Introduction	342
Design Entry Method	342
For More Information	342
INV4	343
Introduction	343
Design Entry Method	343
For More Information	343
INV8	344
Introduction	344
Design Entry Method	344
For More Information	344
IOBUF	345
Introduction	345
Logic Table	345
Port Descriptions	345
Design Entry Method	345
Available Attributes	345

For More Information.....	346
IOBUFDS	347
Introduction.....	347
Logic Table	347
Port Descriptions.....	347
Design Entry Method	347
Available Attributes	347
For More Information.....	348
IODELAY	349
Introduction.....	349
Port Descriptions.....	349
Design Entry Method	349
Available Attributes	350
For More Information.....	350
ISERDES_NODELAY	351
Introduction.....	351
Port Descriptions.....	351
Design Entry Method	352
Available Attributes	352
For More Information.....	352
JTAGPPC440	353
Introduction.....	353
Port Descriptions.....	353
Design Entry Method	353
For More Information.....	353
KEEPER	354
Introduction.....	354
Port Descriptions.....	354
Design Entry Method	354
For More Information.....	354
KEY_CLEAR	355
Introduction.....	355
Port Descriptions.....	355
Design Entry Method	355
For More Information.....	355
LD	356
Introduction.....	356
Logic Table	356
Design Entry Method	356
Available Attributes	356
For More Information.....	356
LD_1	357
Introduction.....	357
Logic Table	357
Design Entry Method	357
Available Attributes	357
For More Information.....	357
LD16	358
Introduction.....	358
Logic Table	358
Design Entry Method	358
Available Attributes	358
For More Information.....	358
LD16CE	359
Introduction.....	359
Logic Table	359
Design Entry Method	359
Available Attributes	359
For More Information.....	359

LD4.....	360
Introduction.....	360
Logic Table	360
Design Entry Method	360
Available Attributes	360
For More Information.....	360
LD4CE	361
Introduction.....	361
Logic Table	361
Design Entry Method	361
Available Attributes	361
For More Information.....	361
LD8.....	362
Introduction.....	362
Logic Table	362
Design Entry Method	362
Available Attributes	362
For More Information.....	362
LD8CE	363
Introduction.....	363
Logic Table	363
Design Entry Method	363
Available Attributes	363
For More Information.....	363
LDC.....	364
Introduction.....	364
Logic Table	364
Design Entry Method	364
Available Attributes	364
For More Information.....	364
LDC_1.....	365
Introduction.....	365
Logic Table	365
Design Entry Method	365
Available Attributes	365
For More Information.....	365
LDCE.....	366
Introduction.....	366
Logic Table	366
Design Entry Method	366
Available Attributes	366
For More Information.....	366
LDCE_1	367
Introduction.....	367
Logic Table	367
Design Entry Method	367
Available Attributes	367
For More Information.....	367
LDCP.....	368
Introduction.....	368
Logic Table	368
Design Entry Method	368
Available Attributes	368
For More Information.....	368
LDCP_1.....	369
Introduction.....	369
Logic Table	369
Design Entry Method	369
Available Attributes	369

For More Information.....	369
LDCPE.....	370
Introduction.....	370
Logic Table	370
Port Descriptions.....	370
Design Entry Method	371
Available Attributes	371
For More Information.....	371
LDCPE_1	372
Introduction.....	372
Logic Table	372
Design Entry Method	372
Available Attributes	372
For More Information.....	372
LDE	373
Introduction.....	373
Logic Table	373
Design Entry Method	373
Available Attributes	373
For More Information.....	373
LDE_1	374
Introduction.....	374
Logic Table	374
Design Entry Method	374
Available Attributes	374
For More Information.....	374
LDP	375
Introduction.....	375
Logic Table	375
Design Entry Method	375
Available Attributes	375
For More Information.....	375
LDP_1	376
Introduction.....	376
Logic Table	376
Design Entry Method	376
Available Attributes	376
For More Information.....	376
LDPE	377
Introduction.....	377
Logic Table	377
Design Entry Method	377
Available Attributes	377
For More Information.....	377
LDPE_1	378
Introduction.....	378
Logic Table	378
Design Entry Method	378
Available Attributes	378
For More Information.....	378
LUT1	379
Introduction.....	379
Logic Table	379
Design Entry Method	379
Available Attributes	379
For More Information.....	380
LUT1_D	381
Introduction.....	381
Logic Table	381

Design Entry Method	381
Available Attributes	381
For More Information.....	381
LUT1_L	382
Introduction.....	382
Logic Table	382
Design Entry Method	382
Available Attributes	382
For More Information.....	382
LUT2	383
Introduction.....	383
Logic Table	383
Design Entry Method	383
Available Attributes	383
For More Information.....	384
LUT2_D	385
Introduction.....	385
Logic Table	385
Design Entry Method	385
Available Attributes	385
For More Information.....	386
LUT2_L	387
Introduction.....	387
Logic Table	387
Design Entry Method	387
Available Attributes	387
For More Information.....	388
LUT3	389
Introduction.....	389
Logic Table	389
Design Entry Method	389
Available Attributes	390
For More Information.....	390
LUT3_D	391
Introduction.....	391
Logic Table	391
Design Entry Method	391
Available Attributes	392
For More Information.....	392
LUT3_L	393
Introduction.....	393
Logic Table	393
Design Entry Method	393
Available Attributes	394
For More Information.....	394
LUT4	395
Introduction.....	395
Logic Table	396
Design Entry Method	396
Available Attributes	396
For More Information.....	396
LUT4_D	397
Introduction.....	397
Logic Table	398
Design Entry Method	398
Available Attributes	398
For More Information.....	398
LUT4_L	399
Introduction.....	399

Logic Table	400
Design Entry Method	400
Available Attributes	400
For More Information	400
LUT5	401
Introduction.....	401
Logic Table	402
Port Description	403
Design Entry Method	403
Available Attributes	403
For More Information.....	403
LUT5_D	404
Introduction.....	404
Logic Table	405
Port Description	406
Design Entry Method	406
Available Attributes	406
For More Information.....	406
LUT5_L.....	407
Introduction.....	407
Logic Table	408
Port Description	409
Design Entry Method	409
Available Attributes	409
For More Information.....	409
LUT6	410
Introduction.....	410
Logic Table	410
Port Description	412
Design Entry Method	412
Available Attributes	412
For More Information.....	412
LUT6_2	413
Introduction.....	413
Logic Table	413
Port Descriptions.....	415
Design Entry Method	415
Available Attributes	415
For More Information.....	415
LUT6_D	416
Introduction.....	416
Logic Table	416
Port Description	418
Design Entry Method	418
Available Attributes	418
For More Information.....	418
LUT6_L.....	419
Introduction.....	419
Logic Table	419
Port Description	421
Design Entry Method	421
Available Attributes	421
For More Information.....	421
M16_1E	422
Introduction.....	422
Logic Table	422
Design Entry Method	423
For More Information.....	423
M2_1.....	424

Introduction.....	424
Logic Table	424
Design Entry Method	424
For More Information.....	424
M2_1B1.....	425
Introduction.....	425
Logic Table	425
Design Entry Method	425
For More Information.....	425
M2_1B2.....	426
Introduction.....	426
Logic Table	426
Design Entry Method	426
For More Information.....	426
M2_1E.....	427
Introduction.....	427
Logic Table	427
Design Entry Method	427
For More Information.....	427
M4_1E.....	428
Introduction.....	428
Logic Table	428
Design Entry Method	428
For More Information.....	428
M8_1E.....	429
Introduction.....	429
Logic Table	429
Design Entry Method	429
For More Information.....	429
MULT18X18	430
Introduction.....	430
Logic Table	430
Design Entry Method	430
For More Information.....	430
MULT18X18S.....	431
Introduction.....	431
Logic Table	431
Design Entry Method	431
For More Information.....	431
MUXCY	432
Introduction.....	432
Logic Table	432
Design Entry Method	432
For More Information.....	432
MUXCY_D.....	433
Introduction.....	433
Logic Table	433
Design Entry Method	433
For More Information.....	433
MUXCY_L.....	434
Introduction.....	434
Logic Table	434
Design Entry Method	434
For More Information.....	434
MUXF7	435
Introduction.....	435
Logic Table	435
Port Descriptions.....	435
Design Entry Method	435

For More Information.....	435
MUXF7_D	436
Introduction.....	436
Logic Table	436
Port Descriptions.....	436
Design Entry Method	436
For More Information.....	436
MUXF7_L.....	437
Introduction.....	437
Logic Table	437
Port Descriptions.....	437
Design Entry Method	437
For More Information.....	437
MUXF8	438
Introduction.....	438
Logic Table	438
Port Descriptions.....	438
Design Entry Method	438
For More Information.....	438
MUXF8_D	439
Introduction.....	439
Logic Table	439
Port Descriptions.....	439
Design Entry Method	439
For More Information.....	439
MUXF8_L.....	440
Introduction.....	440
Logic Table	440
Port Descriptions.....	440
Design Entry Method	440
For More Information.....	440
NAND12.....	441
Introduction.....	441
Design Entry Method	441
For More Information.....	441
NAND16.....	442
Introduction.....	442
Design Entry Method	442
For More Information.....	442
NAND2	443
Introduction.....	443
Design Entry Method	443
For More Information.....	443
NAND2B1.....	444
Introduction.....	444
Design Entry Method	444
For More Information.....	444
NAND2B2.....	445
Introduction.....	445
Design Entry Method	445
For More Information.....	445
NAND3	446
Introduction.....	446
Design Entry Method	446
For More Information.....	446
NAND3B1.....	447
Introduction.....	447
Design Entry Method	447
For More Information.....	447

NAND3B2.....	448
Introduction.....	448
Design Entry Method	448
For More Information.....	448
NAND3B3.....	449
Introduction.....	449
Design Entry Method	449
For More Information.....	449
NAND4	450
Introduction.....	450
Design Entry Method	450
For More Information.....	450
NAND4B1.....	451
Introduction.....	451
Design Entry Method	451
For More Information.....	451
NAND4B2.....	452
Introduction.....	452
Design Entry Method	452
For More Information.....	452
NAND4B3.....	453
Introduction.....	453
Design Entry Method	453
For More Information.....	453
NAND4B4.....	454
Introduction.....	454
Design Entry Method	454
For More Information.....	454
NAND5	455
Introduction.....	455
Design Entry Method	455
For More Information.....	455
NAND5B1.....	456
Introduction.....	456
Design Entry Method	456
For More Information.....	456
NAND5B2.....	457
Introduction.....	457
Design Entry Method	457
For More Information.....	457
NAND5B3.....	458
Introduction.....	458
Design Entry Method	458
For More Information.....	458
NAND5B4.....	459
Introduction.....	459
Design Entry Method	459
For More Information.....	459
NAND5B5.....	460
Introduction.....	460
Design Entry Method	460
For More Information.....	460
NAND6	461
Introduction.....	461
Design Entry Method	461
For More Information.....	461
NAND7	462
Introduction.....	462
Design Entry Method	462

For More Information	462
NAND8	463
Introduction.....	463
Design Entry Method	463
For More Information.....	463
NAND9	464
Introduction.....	464
Design Entry Method	464
For More Information.....	464
NOR12.....	465
Introduction.....	465
Design Entry Method	465
For More Information.....	465
NOR16.....	466
Introduction.....	466
Design Entry Method	466
For More Information.....	466
NOR2.....	467
Introduction.....	467
Design Entry Method	467
For More Information.....	467
NOR2B1.....	468
Introduction.....	468
Design Entry Method	468
For More Information.....	468
NOR2B2.....	469
Introduction.....	469
Design Entry Method	469
For More Information.....	469
NOR3.....	470
Introduction.....	470
Design Entry Method	470
For More Information.....	470
NOR3B1.....	471
Introduction.....	471
Design Entry Method	471
For More Information.....	471
NOR3B2.....	472
Introduction.....	472
Design Entry Method	472
For More Information.....	472
NOR3B3.....	473
Introduction.....	473
Design Entry Method	473
For More Information.....	473
NOR4.....	474
Introduction.....	474
Design Entry Method	474
For More Information.....	474
NOR4B1.....	475
Introduction.....	475
Design Entry Method	475
For More Information.....	475
NOR4B2.....	476
Introduction.....	476
Design Entry Method	476
For More Information.....	476
NOR4B3.....	477
Introduction.....	477

Design Entry Method	477
For More Information	477
NOR4B4	478
Introduction	478
Design Entry Method	478
For More Information	478
NOR5	479
Introduction	479
Design Entry Method	479
For More Information	479
NOR5B1	480
Introduction	480
Design Entry Method	480
For More Information	480
NOR5B2	481
Introduction	481
Design Entry Method	481
For More Information	481
NOR5B3	482
Introduction	482
Design Entry Method	482
For More Information	482
NOR5B4	483
Introduction	483
Design Entry Method	483
For More Information	483
NOR5B5	484
Introduction	484
Design Entry Method	484
For More Information	484
NOR6	485
Introduction	485
Design Entry Method	485
For More Information	485
NOR7	486
Introduction	486
Design Entry Method	486
For More Information	486
NOR8	487
Introduction	487
Design Entry Method	487
For More Information	487
NOR9	488
Introduction	488
Design Entry Method	488
For More Information	488
OBUF	489
Introduction	489
Port Descriptions	489
Design Entry Method	489
Available Attributes	489
For More Information	489
OBUF16	490
Introduction	490
Design Entry Method	490
Available Attributes	490
For More Information	490
OBUF4	491
Introduction	491

Design Entry Method	491
Available Attributes	491
For More Information.....	491
OBUF8	492
Introduction.....	492
Design Entry Method	492
Available Attributes	492
For More Information.....	492
OBUFDS	493
Introduction.....	493
Logic Table	493
Port Descriptions.....	493
Design Entry Method	493
Available Attributes	493
For More Information.....	493
OBUFT.....	494
Introduction.....	494
Logic Table	494
Port Descriptions.....	494
Design Entry Method	494
Available Attributes	494
For More Information.....	495
OBUFT16	496
Introduction.....	496
Logic Table	496
Design Entry Method	496
Available Attributes	496
For More Information.....	496
OBUFT4.....	497
Introduction.....	497
Logic Table	497
Design Entry Method	497
Available Attributes	497
For More Information.....	497
OBUFT8.....	498
Introduction.....	498
Logic Table	498
Design Entry Method	498
Available Attributes	498
For More Information.....	498
OBUFDS	499
Introduction.....	499
Logic Table	499
Port Descriptions.....	499
Design Entry Method	499
Available Attributes	499
For More Information.....	499
ODDR.....	500
Introduction.....	500
Port Descriptions.....	500
Design Entry Method	500
Available Attributes	501
For More Information.....	501
OFD.....	502
Introduction.....	502
Logic Table	502
Design Entry Method	502
For More Information.....	502
OFD_1	503

Introduction.....	503
Logic Table	503
Design Entry Method	503
For More Information.....	503
OFD16	504
Introduction.....	504
Logic Table	504
Design Entry Method	504
For More Information.....	504
OFD4	505
Introduction.....	505
Logic Table	505
Design Entry Method	505
For More Information.....	505
OFD8	506
Introduction.....	506
Logic Table	506
Design Entry Method	506
For More Information.....	506
OFDE.....	507
Introduction.....	507
Logic Table	507
Design Entry Method	507
For More Information.....	507
OFDE_1	508
Introduction.....	508
Logic Table	508
Design Entry Method	508
For More Information.....	508
OFDE16	509
Introduction.....	509
Logic Table	509
Design Entry Method	509
For More Information.....	509
OFDE4	510
Introduction.....	510
Logic Table	510
Design Entry Method	510
For More Information.....	510
OFDE8	511
Introduction.....	511
Logic Table	511
Design Entry Method	511
For More Information.....	511
OFDI.....	512
Introduction.....	512
Logic Table	512
Design Entry Method	512
For More Information.....	512
OFDI_1	513
Introduction.....	513
Logic Table	513
Design Entry Method	513
For More Information.....	513
OFDT.....	514
Introduction.....	514
Logic Table	514
Design Entry Method	514
For More Information.....	514

OFDT_1	515
Introduction.....	515
Logic Table	515
Design Entry Method	515
For More Information.....	515
OFDT16	516
Introduction.....	516
Logic Table	516
Design Entry Method	516
For More Information.....	516
OFDT4.....	517
Introduction.....	517
Logic Table	517
Design Entry Method	517
For More Information.....	517
OFDT8.....	518
Introduction.....	518
Logic Table	518
Design Entry Method	518
For More Information.....	518
OFDX.....	519
Introduction.....	519
Logic Table	519
Design Entry Method	519
For More Information.....	519
OFDX_1	520
Introduction.....	520
Logic Table	520
Design Entry Method	520
For More Information.....	520
OFDX16	521
Introduction.....	521
Logic Table	521
Design Entry Method	521
For More Information.....	521
OFDX4.....	522
Introduction.....	522
Logic Table	522
Design Entry Method	522
For More Information.....	522
OFDX8.....	523
Introduction.....	523
Logic Table	523
Design Entry Method	523
For More Information.....	523
OFDXI	524
Introduction.....	524
Logic Table	524
Design Entry Method	524
For More Information.....	524
OFDXI_1	525
Introduction.....	525
Logic Table	525
Design Entry Method	525
For More Information.....	525
OR12.....	526
Introduction.....	526
Design Entry Method	526
For More Information.....	526

OR16.....	527
Introduction.....	527
Design Entry Method	527
For More Information.....	527
OR2	528
Introduction.....	528
Design Entry Method	528
For More Information.....	528
OR2B1.....	529
Introduction.....	529
Design Entry Method	529
For More Information.....	529
OR2B2.....	530
Introduction.....	530
Design Entry Method	530
For More Information.....	530
OR3	531
Introduction.....	531
Design Entry Method	531
For More Information.....	531
OR3B1.....	532
Introduction.....	532
Design Entry Method	532
For More Information.....	532
OR3B2.....	533
Introduction.....	533
Design Entry Method	533
For More Information.....	533
OR3B3.....	534
Introduction.....	534
Design Entry Method	534
For More Information.....	534
OR4	535
Introduction.....	535
Design Entry Method	535
For More Information.....	535
OR4B1.....	536
Introduction.....	536
Design Entry Method	536
For More Information.....	536
OR4B2.....	537
Introduction.....	537
Design Entry Method	537
For More Information.....	537
OR4B3.....	538
Introduction.....	538
Design Entry Method	538
For More Information.....	538
OR4B4.....	539
Introduction.....	539
Design Entry Method	539
For More Information.....	539
OR5	540
Introduction.....	540
Design Entry Method	540
For More Information.....	540
OR5B1.....	541
Introduction.....	541
Design Entry Method	541

For More Information.....	541
OR5B2.....	542
Introduction.....	542
Design Entry Method	542
For More Information.....	542
OR5B3.....	543
Introduction.....	543
Design Entry Method	543
For More Information.....	543
OR5B4.....	544
Introduction.....	544
Design Entry Method	544
For More Information.....	544
OR5B5.....	545
Introduction.....	545
Design Entry Method	545
For More Information.....	545
OR6	546
Introduction.....	546
Design Entry Method	546
For More Information.....	546
OR7	547
Introduction.....	547
Design Entry Method	547
For More Information.....	547
OR8	548
Introduction.....	548
Design Entry Method	548
For More Information.....	548
OR9	549
Introduction.....	549
Design Entry Method	549
For More Information.....	549
OSERDES.....	550
Introduction.....	550
Port Descriptions.....	550
Design Entry Method	551
Available Attributes	552
For More Information.....	553
PCIE_EP.....	554
Introduction.....	555
Design Entry Method	555
For More Information.....	555
PLL_ADV	556
Introduction.....	556
Port Descriptions.....	556
Design Entry Method	557
Available Attributes	558
For More Information.....	560
PLL_BASE.....	561
Introduction.....	561
Port Descriptions.....	561
Design Entry Method	561
Available Attributes	562
For More Information.....	563
PPC440	564
Introduction.....	568
Design Entry Method	568
For More Information.....	568

PULLDOWN	569
Introduction.....	569
Port Descriptions.....	569
Design Entry Method	569
For More Information.....	569
PULLUP.....	570
Introduction.....	570
Port Descriptions.....	570
Design Entry Method	570
For More Information.....	570
RAM128X1D	571
Introduction.....	571
Port Descriptions.....	571
Design Entry Method	571
Available Attributes	572
For More Information.....	572
RAM16X1D	573
Introduction.....	573
Logic Table	573
Design Entry Method	574
Available Attributes	574
For More Information.....	574
RAM16X1D_1.....	575
Introduction.....	575
Logic Table	575
Port Descriptions.....	576
Design Entry Method	576
Available Attributes	576
For More Information.....	576
RAM16X1S.....	577
Introduction.....	577
Logic Table	577
Design Entry Method	577
Available Attributes	577
For More Information.....	577
RAM16X1S_1.....	578
Introduction.....	578
Logic Table	578
Design Entry Method	578
Available Attributes	578
For More Information.....	579
RAM16X2S.....	580
Introduction.....	580
Logic Table	580
Design Entry Method	580
Available Attributes	581
For More Information.....	581
RAM16X4S.....	582
Introduction.....	582
Logic Table	582
Design Entry Method	582
Available Attributes	582
For More Information.....	583
RAM16X8S.....	584
Introduction.....	584
Logic Table	584
Design Entry Method	584
Available Attributes	584
For More Information.....	585

RAM256X1S	586
Introduction.....	586
Port Descriptions.....	586
Design Entry Method	586
Available Attributes	586
For More Information.....	587
RAM32M	588
Introduction.....	588
Port Descriptions.....	588
Design Entry Method	589
Available Attributes	589
For More Information.....	589
RAM32X1D	590
Introduction.....	590
Logic Table	590
Design Entry Method	590
Available Attributes	591
For More Information.....	591
RAM32X1S.....	592
Introduction.....	592
Logic Table	592
Design Entry Method	592
Available Attributes	592
For More Information.....	592
RAM32X1S_1.....	593
Introduction.....	593
Logic Table	593
Design Entry Method	593
Available Attributes	593
For More Information.....	593
RAM32X2S.....	594
Introduction.....	594
Logic Table	594
Design Entry Method	594
Available Attributes	594
For More Information.....	595
RAM32X4S.....	596
Introduction.....	596
Logic Table	596
Design Entry Method	596
Available Attributes	597
For More Information.....	597
RAM32X8S.....	598
Introduction.....	598
Logic Table	598
Design Entry Method	598
Available Attributes	599
For More Information.....	599
RAM64M	600
Introduction.....	600
Port Descriptions.....	601
Design Entry Method	601
Available Attributes	602
For More Information.....	602
RAM64X1D	603
Introduction.....	603
Logic Table	603
Design Entry Method	603
Available Attributes	604

For More Information.....	604
RAM64X1S.....	605
Introduction.....	605
Logic Table	605
Design Entry Method	605
Available Attributes	605
For More Information.....	606
RAM64X1S_1.....	607
Introduction.....	607
Logic Table	607
Design Entry Method	607
Available Attributes	607
For More Information.....	607
RAM64X2S.....	608
Introduction.....	608
Logic Table	608
Design Entry Method	608
Available Attributes	608
For More Information.....	609
RAMB18	610
Introduction.....	610
Port Descriptions.....	610
Design Entry Method	611
Available Attributes	611
For More Information.....	613
RAMB18SDP	614
Introduction.....	614
Port Descriptions.....	614
Design Entry Method	614
Available Attributes	615
For More Information.....	615
RAMB36	616
Introduction.....	616
Port Descriptions.....	617
Design Entry Method	617
Available Attributes	618
For More Information.....	620
RAMB36SDP	621
Introduction.....	621
Port Descriptions.....	621
Design Entry Method	622
Available Attributes	622
For More Information.....	623
ROM128X1	624
Introduction.....	624
Logic Table	624
Design Entry Method	624
Available Attributes	625
For More Information.....	625
ROM16X1.....	626
Introduction.....	626
Logic Table	626
Design Entry Method	626
Available Attributes	627
For More Information.....	627
ROM256X1	628
Introduction.....	628
Logic Table	628
Design Entry Method	629

Available Attributes	629
For More Information	629
ROM32X1	630
Introduction	630
Logic Table	630
Design Entry Method	630
Available Attributes	631
For More Information	631
ROM64X1	632
Introduction	632
Logic Table	632
Design Entry Method	632
Available Attributes	633
For More Information	633
SOP3	634
Introduction	634
Design Entry Method	634
For More Information	634
SOP3B1A	635
Introduction	635
Design Entry Method	635
For More Information	635
SOP3B1B	636
Introduction	636
Design Entry Method	636
For More Information	636
SOP3B2A	637
Introduction	637
Design Entry Method	637
For More Information	637
SOP3B2B	638
Introduction	638
Design Entry Method	638
For More Information	638
SOP3B3	639
Introduction	639
Design Entry Method	639
For More Information	639
SOP4	640
Introduction	640
Design Entry Method	640
For More Information	640
SOP4B1	641
Introduction	641
Design Entry Method	641
For More Information	641
SOP4B2A	642
Introduction	642
Design Entry Method	642
For More Information	642
SOP4B2B	643
Introduction	643
Design Entry Method	643
For More Information	643
SOP4B3	644
Introduction	644
Design Entry Method	644
For More Information	644
SOP4B4	645

Introduction.....	645
Design Entry Method	645
For More Information.....	645
SR16CE	646
Introduction.....	646
Logic Table	646
Design Entry Method	646
For More Information.....	646
SR16CLE	647
Introduction.....	647
Logic Table	647
Design Entry Method	647
For More Information.....	648
SR16CLED.....	649
Introduction.....	649
Logic Table	649
Design Entry Method	649
For More Information.....	650
SR16RE	651
Introduction.....	651
Logic Table	651
Design Entry Method	651
For More Information.....	651
SR16RLE	652
Introduction.....	652
Logic Table	652
Design Entry Method	652
For More Information.....	653
SR16RLED.....	654
Introduction.....	654
Logic Table	654
Design Entry Method	654
For More Information.....	655
SR4CE.....	656
Introduction.....	656
Logic Table	656
Design Entry Method	656
For More Information.....	656
SR4CLE.....	657
Introduction.....	657
Logic Table	657
Design Entry Method	657
For More Information.....	658
SR4CLED	659
Introduction.....	659
Logic Table	659
Design Entry Method	659
For More Information.....	660
SR4RE	661
Introduction.....	661
Logic Table	661
Design Entry Method	661
For More Information.....	661
SR4RLE	662
Introduction.....	662
Logic Table	662
Design Entry Method	663
For More Information.....	663
SR4RLED	664

Introduction.....	664
Logic Table	664
Design Entry Method	665
For More Information.....	665
SR8CE.....	666
Introduction.....	666
Logic Table	666
Design Entry Method	666
For More Information.....	666
SR8CLE.....	667
Introduction.....	667
Logic Table	667
Design Entry Method	667
For More Information.....	668
SR8CLED	669
Introduction.....	669
Logic Table	669
Design Entry Method	669
For More Information.....	670
SR8RE	671
Introduction.....	671
Logic Table	671
Design Entry Method	671
For More Information.....	671
SR8RLE.....	672
Introduction.....	672
Logic Table	672
Design Entry Method	672
For More Information.....	673
SR8RLED	674
Introduction.....	674
Logic Table	674
Design Entry Method	674
For More Information.....	675
SRL16	676
Introduction.....	676
Logic Table	676
Design Entry Method	676
Available Attributes	676
For More Information.....	677
SRL16_1	678
Introduction.....	678
Logic Table	678
Design Entry Method	678
Available Attributes	678
For More Information.....	679
SRL16E	680
Introduction.....	680
Logic Table	680
Port Descriptions.....	681
Design Entry Method	681
Available Attributes	681
For More Information.....	681
SRL16E_1	682
Introduction.....	682
Logic Table	682
Design Entry Method	682
Available Attributes	682
For More Information.....	683

SRLC16	684
Introduction.....	684
Logic Table	684
Design Entry Method	684
Available Attributes	684
For More Information.....	685
SRLC16_1.....	686
Introduction.....	686
Logic Table	686
Design Entry Method	686
Available Attributes	686
For More Information.....	687
SRLC16E	688
Introduction.....	688
Logic Table	688
Design Entry Method	688
Available Attributes	689
For More Information.....	689
SRLC16E_1.....	690
Introduction.....	690
Logic Table	690
Design Entry Method	690
Available Attributes	691
For More Information.....	691
SRLC32E	692
Introduction.....	692
Port Descriptions.....	692
Design Entry Method	692
Available Attributes	693
For More Information.....	693
STARTUP_VIRTEX5	694
Introduction.....	694
Port Descriptions.....	694
Design Entry Method	694
For More Information.....	695
SYSMON.....	696
Introduction.....	696
Port Descriptions.....	696
Design Entry Method	697
Available Attributes	697
For More Information.....	698
TEMAC.....	699
Introduction.....	700
Design Entry Method	700
For More Information.....	701
USR_ACCESS_VIRTEX5	702
Introduction.....	702
Port Descriptions.....	702
Design Entry Method	702
For More Information.....	702
VCC.....	703
Introduction.....	703
Design Entry Method	703
For More Information.....	703
XNOR2	704
Introduction.....	704
Logic Table	704
Design Entry Method	704
For More Information.....	704

XNOR3	705
Introduction.....	705
Logic Table	705
Design Entry Method	705
For More Information.....	705
XNOR4	706
Introduction.....	706
Logic Table	706
Design Entry Method	706
For More Information.....	706
XNOR5	707
Introduction.....	707
Logic Table	707
Design Entry Method	707
For More Information.....	707
XNOR6	708
Introduction.....	708
Logic Table	708
Design Entry Method	708
For More Information.....	708
XNOR7	709
Introduction.....	709
Logic Table	709
Design Entry Method	709
For More Information.....	709
XNOR8	710
Introduction.....	710
Logic Table	710
Design Entry Method	710
For More Information.....	710
XNOR9	711
Introduction.....	711
Logic Table	711
Design Entry Method	711
For More Information.....	711
XOR2	712
Introduction.....	712
Design Entry Method	712
For More Information.....	712
XOR3	713
Introduction.....	713
Design Entry Method	713
For More Information.....	713
XOR4	714
Introduction.....	714
Design Entry Method	714
For More Information.....	714
XOR5	715
Introduction.....	715
Design Entry Method	715
For More Information.....	715
XOR6	716
Introduction.....	716
Design Entry Method	716
For More Information.....	716
XOR7	717
Introduction.....	717
Design Entry Method	717
For More Information.....	717

XOR8	718
Introduction.....	718
Design Entry Method	718
For More Information.....	718
XOR9	719
Introduction.....	719
Design Entry Method	719
For More Information.....	719
XORCY	720
Introduction.....	720
Logic Table	720
Design Entry Method	720
For More Information.....	720

About this Guide

This schematic guide is part of the ISE documentation collection. A separate version of this guide is available if you prefer to work with HDL.

This guide contains the following:

- Introduction.
- A list of *retargeted elements*.
- A list of design elements supported in this architecture, organized by functional categories.
- Detailed descriptions of each available macro.
- Individual descriptions of each available primitive.

About Design Elements

This version of the Libraries Guide describes design elements available for this architecture. There are several categories of design elements:

- **Retargeted Elements** - These elements are automatically changed by the ISE software tools when they are used in this architecture. Retargeting ensures that your design takes advantage of the latest circuit design advances.
- **Primitives** - The simplest design elements in the Xilinx libraries. Primitives are the design element "atoms." Examples of Xilinx primitives are the simple buffer, BUF, and the D flip-flop with clock enable and clear, FDCE.
- **Macros** - The design element "molecules" of the Xilinx libraries. Macros can be created from the design element primitives or macros. For example, the FD4CE flip-flop macro is a composite of 4 FDCE primitives.

Xilinx maintains software libraries with hundreds of functional design elements (macros and primitives) for different device architectures. New functional elements are assembled with each release of development system software. This guide is one in a series of architecture-specific libraries.

Design Element Retargeting

To ensure that Xilinx® customers are able to take full advantage of the latest circuit design advances, certain design elements are automatically changed by the ISE® Design Suite software tools when they are used in this architecture.

The following table lists these elements and the more advanced elements into which they are transformed.

Original Element	Modern Equivalent
BUFGCE_1	BUFGCE + INV
BUFGMUX	BUFGMUX_CTRL
BUFGMUX_1	BUFGMUX_CTRL + INV
BUFGMUX_VIRTEX4	BUFGMUX_CTRL
BUFGP	BUFG
DCM_BASE	DCM_ADV
DCM_PS	DCM_ADV
DSP48	DSP48E
FD	FDCPE
FD_1	FDCPE + INV
FDC	FDCPE
FDC_1	FDCPE + INV
FDCE	FDCPE
FDCE_1	FDCPE + INV
FDCP	FDCPE
FDCP_1	FDCPE + INV
FDE	FDCPE
FDE_1	FDCPE + INV
FDPE	FDCPE
FDPE_1	FDCPE + INV
FDR	FDRSE
FDR_1	FDRSE + INV
FDRE	FDRSE
FDRE_1	FDRSE + INV
FDRS	FDRSE
FDRS_1	FDRSE + INV

Original Element	Modern Equivalent
FDS	FDRSE
FDS_1	FDRSE + INV
FDSE	FDRSE
FDSE_1	FDRSE + INV
FIFO16	FIFO18
ISERDES	ISERDES_NODELAY
JTAGPPC	JTAG_PPC440
LD	LDCPE
LD_1	LDCPE + INV
LDC	LDCPE
LDC_1	LDCPE + INV
LDCE	LDCPE
LDCE_1	LDCPE + INV
LDCP	LDCPE
LDCP_1	LDCPE + INV
LDE	LDCPE
LDE_1	LDCPE + INV
LDP	LDCPE
LDP_1	LDCPE + INV
LDPE	LDCPE
LDPE_1	LDCPE + INV
LUT1	LUT5
LUT1_L	LUT5_L
LUT1_D	LUT5_D
LUT2	LUT5
LUT2_L	LUT5_L
LUT2_D	LUT5_D
LUT3	LUT5
LUT3_L	LUT5_L
LUT3_D	LUT5_D
LUT4	LUT5
LUT4_L	LUT5_L
LUT4_D	LUT5_D
MULT_AND	LUT6
MULT18X18	DSP48E
MULT18X18S	DSP48E
MUXCY	CARRY4
MUXCY_D	CARRY4

Original Element	Modern Equivalent
MUXCY_L	CARRY4
MUXF5	LUT5
MUXF5_D	LUT5_D
MUXF5_L	LUT5_L
MUXF6	LUT6
MUXF6_D	LUT6_D
MUXF6_L	LUT6_L
PMCD	PLL_ADV
RAM16X1D	RAM64X1D
RAM16X1S	RAM64X1S
RAM32X1S	RAM64X1S
RAMB16	RAMB18
RAMB16BWE	RAMB18
ROM128X1	2 LUT6'S + MUXF7
ROM16X1	LUT5
ROM256X1	4 LUT6'S + MUXF6/7
ROM32X1	LUT5
ROM64X1	LUT6
SRLC16	SRLC32E
SRLC16_1	SRLC32E + INV
SRLC16E	SRLC32E
SRLC16E_1	SRLC32E + INV
XORCY	CARRY4
XORCY_D	CARRY4
XORCY_L	CARRY4

Functional Categories

This section categorizes, by function, the circuit design elements described in detail later in this guide. The elements (*primitives* and *macros*) are listed in alphanumeric order under each functional category.

Advanced	Flip Flop	Logic
Arithmetic	General	LUT
Buffer	GigaBit IO/Processor	Memory
Carry Logic	Input/Output Functions	MUX
Clocking Resources	IO	Shift Register
Comparator	IO FlipFlop	Shifter
Counter	IO Latch	
Decoder	Latch	

Advanced

Design Element	Description
CRC32	Primitive: Cyclic Redundancy Check Calculator for 32 bits
CRC64	Primitive: Cyclic Redundancy Check Calculator for 64 bits
GTP_DUAL	Primitive: Dual Gigabit Transceiver
GTX_DUAL	Primitive: Dual Gigabit Transceiver
PCIE_EP	Primitive: PCI Express
TEMAC	Primitive: Tri-mode Ethernet Media Access Controller (MAC)

Arithmetic

Design Element	Description
ACC16	Macro: 16-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset
ACC4	Macro: 4-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset
ACC8	Macro: 8-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset
ADD16	Macro: 16-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow
ADD4	Macro: 4-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow
ADD8	Macro: 8-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow
ADSU16	Macro: 16-Bit Cascadable Adder/Subtractor with Carry-In, Carry-Out, and Overflow
ADSU4	Macro: 4-Bit Cascadable Adder/Subtractor with Carry-In, Carry-Out, and Overflow
ADSU8	Macro: 8-Bit Cascadable Adder/Subtractor with Carry-In, Carry-Out, and Overflow
DSP48E	Primitive: 25x18 Two's Complement Multiplier with Integrated 48-Bit, 3-Input Adder/Subtractor/Accumulator or 2-Input Logic Unit
MULT18X18	Primitive: 18 x 18 Signed Multiplier
MULT18X18S	Primitive: 18 x 18 Signed Multiplier -- Registered Version

Buffer

Design Element	Description
BUF	Primitive: General Purpose Buffer
BUFCF	Primitive: Fast Connect Buffer
BUFG	Primitive: Global Clock Buffer
BUFGCE	Primitive: Global Clock Buffer with Clock Enable
BUFGCE_1	Primitive: Global Clock Buffer with Clock Enable and Output State 1
BUFGMUX_CTRL	Primitive: 2-to-1 Global Clock MUX Buffer

Carry Logic

Design Element	Description
CARRY4	Primitive: Fast Carry Logic with Look Ahead
MUXCY	Primitive: 2-to-1 Multiplexer for Carry Logic with General Output
MUXCY_D	Primitive: 2-to-1 Multiplexer for Carry Logic with Dual Output
MUXCY_L	Primitive: 2-to-1 Multiplexer for Carry Logic with Local Output
XORCY	Primitive: XOR for Carry Logic with General Output

Clocking Resources

Design Element	Description
BUFGCTRL	Primitive: Global Clock MUX Buffer
BUFIO	Primitive: Local Clock Buffer for I/O
BUFR	Primitive: Regional Clock Buffer for I/O and Logic Resources
DCM_ADV	Primitive: Advanced Digital Clock Manager Circuit
DCM_BASE	Primitive: Base Digital Clock Manager Circuit
DCM_PS	Primitive: Digital Clock Manager with Basic and Phase Shift Features
PLL_ADV	Primitive: Advanced Phase Locked Loop Clock Circuit
PLL_BASE	Primitive: Basic Phase Locked Loop Clock Circuit
SYSMON	Primitive: System Monitor

Comparator

Design Element	Description
COMP16	Macro: 16-Bit Identity Comparator
COMP2	Macro: 2-Bit Identity Comparator
COMP4	Macro: 4-Bit Identity Comparator
COMP8	Macro: 8-Bit Identity Comparator
COMPM16	Macro: 16-Bit Magnitude Comparator
COMPM2	Macro: 2-Bit Magnitude Comparator
COMPM4	Macro: 4-Bit Magnitude Comparator
COMPM8	Macro: 8-Bit Magnitude Comparator
COMPMC16	Macro: 16-Bit Magnitude Comparator
COMPMC8	Macro: 8-Bit Magnitude Comparator

Counter

Design Element	Description
CB16CE	Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear
CB16CLE	Macro: 16-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear
CB16CLED	Macro: 16-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear
CB16RE	Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset
CB2CE	Macro: 2-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear
CB2CLE	Macro: 2-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear
CB2CLED	Macro: 2-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear
CB2RE	Macro: 2-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset

Design Element	Description
CB4CE	Macro: 4-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear
CB4CLE	Macro: 4-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear
CB4CLED	Macro: 4-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear
CB4RE	Macro: 4-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset
CB8CE	Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear
CB8CLE	Macro: 8-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear
CB8CLED	Macro: 8-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear
CB8RE	Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset
CC16CE	Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear
CC16CLE	Macro: 16-Bit Loadable Cascadable Binary Counter with Clock Enable and Asynchronous Clear
CC16CLED	Macro: 16-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear
CC16RE	Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset
CC8CE	Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear
CC8CLE	Macro: 8-Bit Loadable Cascadable Binary Counter with Clock Enable and Asynchronous Clear
CC8CLED	Macro: 8-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear
CC8RE	Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset
CD4CE	Macro: 4-Bit Cascadable BCD Counter with Clock Enable and Asynchronous Clear
CD4CLE	Macro: 4-Bit Loadable Cascadable BCD Counter with Clock Enable and Asynchronous Clear
CD4RE	Macro: 4-Bit Cascadable BCD Counter with Clock Enable and Synchronous Reset
CD4RLE	Macro: 4-Bit Loadable Cascadable BCD Counter with Clock Enable and Synchronous Reset
CJ4CE	4-Bit Johnson Counter with Clock Enable and Asynchronous Clear
CJ4RE	Macro: 4-Bit Johnson Counter with Clock Enable and Synchronous Reset
CJ5CE	Macro: 5-Bit Johnson Counter with Clock Enable and Asynchronous Clear
CJ5RE	Macro: 5-Bit Johnson Counter with Clock Enable and Synchronous Reset
CJ8CE	Macro: 8-Bit Johnson Counter with Clock Enable and Asynchronous Clear
CJ8RE	Macro: 8-Bit Johnson Counter with Clock Enable and Synchronous Reset

Decoder

Design Element	Description
D2_4E	Macro: 2- to 4-Line Decoder/Demultiplexer with Enable
D3_8E	Macro: 3- to 8-Line Decoder/Demultiplexer with Enable
D4_16E	Macro: 4- to 16-Line Decoder/Demultiplexer with Enable
DEC_CC16	Macro: 16-Bit Active Low Decoder
DEC_CC4	Macro: 4-Bit Active Low Decoder
DEC_CC8	Macro: 8-Bit Active Low Decoder

Flip Flop

Design Element	Description
FD	Primitive: D Flip-Flop
FD_1	Primitive: D Flip-Flop with Negative-Edge Clock
FD16CE	Macro: 16-Bit Data Register with Clock Enable and Asynchronous Clear
FD16RE	Macro: 16-Bit Data Register with Clock Enable and Synchronous Reset
FD4CE	Macro: 4-Bit Data Register with Clock Enable and Asynchronous Clear
FD4RE	Macro: 4-Bit Data Register with Clock Enable and Synchronous Reset
FD8CE	Macro: 8-Bit Data Register with Clock Enable and Asynchronous Clear
FD8RE	Macro: 8-Bit Data Register with Clock Enable and Synchronous Reset
FDC	Primitive: D Flip-Flop with Asynchronous Clear
FDC_1	Primitive: D Flip-Flop with Negative-Edge Clock and Asynchronous Clear
FDCE	Primitive: D Flip-Flop with Clock Enable and Asynchronous Clear
FDCE_1	Primitive: D Flip-Flop with Negative-Edge Clock, Clock Enable, and Asynchronous Clear
FDCP	Primitive: D Flip-Flop with Asynchronous Preset and Clear
FDCP_1	Primitive: D Flip-Flop with Negative-Edge Clock and Asynchronous Preset and Clear
FDCPE	Primitive: D Flip-Flop with Clock Enable and Asynchronous Preset and Clear
FDCPE_1	Primitive: D Flip-Flop with Negative-Edge Clock, Clock Enable, and Asynchronous Preset and Clear
FDE	Primitive: D Flip-Flop with Clock Enable
FDE_1	Primitive: D Flip-Flop with Negative-Edge Clock and Clock Enable
FDP	Primitive: D Flip-Flop with Asynchronous Preset
FDP_1	Primitive: D Flip-Flop with Negative-Edge Clock and Asynchronous Preset
FDPE	Primitive: D Flip-Flop with Clock Enable and Asynchronous Preset
FDPE_1	Primitive: D Flip-Flop with Negative-Edge Clock, Clock Enable, and Asynchronous Preset
FDR	Primitive: D Flip-Flop with Synchronous Reset
FDR_1	Primitive: D Flip-Flop with Negative-Edge Clock and Synchronous Reset
FDRE	Primitive: D Flip-Flop with Clock Enable and Synchronous Reset

Design Element	Description
FDRE_1	Primitive: D Flip-Flop with Negative-Clock Edge, Clock Enable, and Synchronous Reset
FDRS	Primitive: D Flip-Flop with Synchronous Reset and Set
FDRS_1	Primitive: D Flip-Flop with Negative-Clock Edge and Synchronous Reset and Set
FDRSE	Primitive: D Flip-Flop with Synchronous Reset and Set and Clock Enable
FDRSE_1	Primitive: D Flip-Flop with Negative-Clock Edge, Synchronous Reset and Set, and Clock Enable
FDS	Primitive: D Flip-Flop with Synchronous Set
FDS_1	Primitive: D Flip-Flop with Negative-Edge Clock and Synchronous Set
FDSE	Primitive: D Flip-Flop with Clock Enable and Synchronous Set
FDSE_1	Primitive: D Flip-Flop with Negative-Edge Clock, Clock Enable, and Synchronous Set
FJKC	Macro: J-K Flip-Flop with Asynchronous Clear
FJKCE	Macro: J-K Flip-Flop with Clock Enable and Asynchronous Clear
FJKP	Macro: J-K Flip-Flop with Asynchronous Preset
FJKPE	Macro: J-K Flip-Flop with Clock Enable and Asynchronous Preset
FJKRSE	Macro: J-K Flip-Flop with Clock Enable and Synchronous Reset and Set
FJKSRE	Macro: J-K Flip-Flop with Clock Enable and Synchronous Set and Reset
FTC	Macro: Toggle Flip-Flop with Asynchronous Clear
FTCE	Macro: Toggle Flip-Flop with Clock Enable and Asynchronous Clear
FTCLE	Macro: Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Clear
FTCLEX	Macro: Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Clear
FTP	Macro: Toggle Flip-Flop with Asynchronous Preset
FTPE	Macro: Toggle Flip-Flop with Clock Enable and Asynchronous Preset
FTPLE	Macro: Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Preset
FTRSE	Macro: Toggle Flip-Flop with Clock Enable and Synchronous Reset and Set
FTRSLE	Macro: Toggle/Loadable Flip-Flop with Clock Enable and Synchronous Reset and Set
FTSRE	Macro: Toggle Flip-Flop with Clock Enable and Synchronous Set and Reset
FTSRLE	Macro: Toggle/Loadable Flip-Flop with Clock Enable and Synchronous Set and Reset

General

Design Element	Description
BSCAN_VIRTEX5	Primitive: Virtex®-5 JTAG Boundary-Scan Logic Access Circuit
CAPTURE_VIRTEX5	Primitive: Virtex®-5 Readback Register Capture Control
FRAME_ECC_VIRTEX5	Primitive: Virtex®-5 Configuration Frame Error Detection and Correction Circuitry
GND	Primitive: Ground-Connection Signal Tag
ICAP_VIRTEX5	Primitive: Internal Configuration Access Port
KEEPER	Primitive: KEEPER Symbol
KEY_CLEAR	Primitive: Virtex-5 Configuration Encryption Key Erase
PULLDOWN	Primitive: Resistor to GND for Input Pads, Open-Drain, and 3-State Outputs
PULLUP	Primitive: Resistor to VCC for Input PADS, Open-Drain, and 3-State Outputs
STARTUP_VIRTEX5	Primitive: Virtex®-5 Configuration Start-Up Sequence Interface
USR_ACCESS_VIRTEX5	Primitive: Virtex-5 User Access Register
VCC	Primitive: VCC-Connection Signal Tag

GigaBit IO/Processor

Design Element	Description
JTAGPPC440	Primitive: JTAG Primitive for the Power PC
PPC440	Primitive: Power PC 440 CPU Core

Input/Output Functions

Design Element	Description
DCIRESET	Primitive: DCI State Machine Reset (After Configuration Has Been Completed)
IDDR	Primitive: Input Dual Data-Rate Register
IDDR_2CLK	Primitive: Input Dual Data-Rate Register with Dual Clock Inputs
IDELAY	Primitive: Input Delay Element
IDELAYCTRL	Primitive: IDELAY Tap Delay Value Control
IODELAY	Primitive: Input and Output Fixed or Variable Delay Element
ISERDES_NODELAY	Primitive: Input SERIAL/DESerializer
ODDR	Primitive: Dedicated Dual Data Rate (DDR) Output Register
OSERDES	Primitive: Dedicated IOB Output Serializer

IO

Design Element	Description
IBUF	Primitive: Input Buffer
IBUF16	Macro: 16-Bit Input Buffer
IBUF4	Macro: 4-Bit Input Buffer
IBUF8	Macro: 8-Bit Input Buffer
IBUFDS	Primitive: Differential Signaling Input Buffer
IBUFG	Primitive: Dedicated Input Clock Buffer
IBUFGDS	Primitive: Differential Signaling Dedicated Input Clock Buffer and Optional Delay
IOBUF	Primitive: Bi-Directional Buffer
IOBUFDS	Primitive: 3-State Differential Signaling I/O Buffer with Active Low Output Enable
OBUF	Primitive: Output Buffer
OBUF16	Macro: 16-Bit Output Buffer
OBUF4	Macro: 4-Bit Output Buffer
OBUF8	Macro: 8-Bit Output Buffer
OBUFDS	Primitive: Differential Signaling Output Buffer
OBUFFT	Primitive: 3-State Output Buffer with Active Low Output Enable
OBUFFT16	Macro: 16-Bit 3-State Output Buffer with Active Low Output Enable
OBUFFT4	Macro: 4-Bit 3-State Output Buffers with Active-Low Output Enable
OBUFFT8	Macro: 8-Bit 3-State Output Buffers with Active-Low Output Enable
OBUFFTDS	Primitive: 3-State Output Buffer with Differential Signaling, Active-Low Output Enable

IO FlipFlop

Design Element	Description
IFD	Macro: Input D Flip-Flop
IFD_1	Macro: Input D Flip-Flop with Inverted Clock (Asynchronous Preset)
IFD16	Macro: 16-Bit Input D Flip-Flop
IFD4	Macro: 4-Bit Input D Flip-Flop
IFD8	Macro: 8-Bit Input D Flip-Flop
IFDI	Macro: Input D Flip-Flop (Asynchronous Preset)
IFDI_1	Macro: Input D Flip-Flop with Inverted Clock (Asynchronous Preset)
IFDX	Macro: Input D Flip-Flop with Clock Enable
IFDX_1	Macro: Input D Flip-Flop with Inverted Clock and Clock Enable
IFDX16	Macro: 16-Bit Input D Flip-Flops with Clock Enable
IFDX4	Macro: 4-Bit Input D Flip-Flop with Clock Enable
IFDX8	Macro: 8-Bit Input D Flip-Flop with Clock Enable
OFD	Macro: Output D Flip-Flop
OFD_1	Macro: Output D Flip-Flop with Inverted Clock

Design Element	Description
OFD16	Macro: 16-Bit Output D Flip-Flop
OFD4	Macro: 4-Bit Output D Flip-Flop
OFD8	Macro: 8-Bit Output D Flip-Flop
OFDE	Macro: D Flip-Flop with Active-High Enable Output Buffers
OFDE_1	Macro: D Flip-Flop with Active-High Enable Output Buffer and Inverted Clock
OFDE16	Macro: 16-Bit D Flip-Flop with Active-High Enable Output Buffers
OFDE4	Macro: 4-Bit D Flip-Flop with Active-High Enable Output Buffers
OFDE8	Macro: 8-Bit D Flip-Flop with Active-High Enable Output Buffers
OFDI	Macro: Output D Flip-Flop (Asynchronous Preset)
OFDI_1	Macro: Output D Flip-Flop with Inverted Clock (Asynchronous Preset)
OFDT	Macro: D Flip-Flop with Active-Low 3-State Output Buffer
OFDT_1	Macro: D Flip-Flop with Active-Low 3-State Output Buffer and Inverted Clock
OFDT16	Macro: 16-Bit D Flip-Flop with Active-Low 3-State Output Buffers
OFDT4	Macro: 4-Bit D Flip-Flop with Active-Low 3-State Output Buffers
OFDT8	Macro: 8-Bit D Flip-Flop with Active-Low 3-State Output Buffers
OFDX	Macro: Output D Flip-Flop with Clock Enable
OFDX_1	Macro: Output D Flip-Flop with Inverted Clock and Clock Enable
OFDX16	Macro: 16-Bit Output D Flip-Flop with Clock Enable
OFDX4	Macro: 4-Bit Output D Flip-Flop with Clock Enable
OFDX8	Macro: 8-Bit Output D Flip-Flop with Clock Enable
OFDXI	Macro: Output D Flip-Flop with Clock Enable (Asynchronous Preset)
OFDXI_1	Macro: Output D Flip-Flop with Inverted Clock and Clock Enable (Asynchronous Preset)

IO Latch

Design Element	Description
ILD	Macro: Transparent Input Data Latch
ILD_1	Macro: Transparent Input Data Latch with Inverted Gate
ILD16	Macro: Transparent Input Data Latch
ILD4	Macro: Transparent Input Data Latch
ILD8	Macro: Transparent Input Data Latch
ILDI	Macro: Transparent Input Data Latch (Asynchronous Preset)
ILDI_1	Macro: Transparent Input Data Latch with Inverted Gate (Asynchronous Preset)
ILDXI	Macro: Transparent Input Data Latch (Asynchronous Preset)
ILDXI_1	Macro: Transparent Input Data Latch with Inverted Gate (Asynchronous Preset)

Latch

Design Element	Description
LD	Primitive: Transparent Data Latch
LD_1	Primitive: Transparent Data Latch with Inverted Gate
LD16	Macro: Multiple Transparent Data Latch
LD16CE	Macro: Transparent Data Latch with Asynchronous Clear and Gate Enable
LD4	Macro: Multiple Transparent Data Latch
LD4CE	Macro: Transparent Data Latch with Asynchronous Clear and Gate Enable
LD8	Macro: Multiple Transparent Data Latch
LD8CE	Macro: Transparent Data Latch with Asynchronous Clear and Gate Enable
LDC	Primitive: Macro: Transparent Data Latch with Asynchronous Clear
LDC_1	Primitive: Transparent Data Latch with Asynchronous Clear and Inverted Gate
LDCE	Primitive: Transparent Data Latch with Asynchronous Clear and Gate Enable
LDCE_1	Primitive: Transparent Data Latch with Asynchronous Clear, Gate Enable, and Inverted Gate
LDCP	Primitive: Transparent Data Latch with Asynchronous Clear and Preset
LDCP_1	Primitive: Transparent Data Latch with Asynchronous Clear and Preset and Inverted Gate
LDCPE	Primitive: Transparent Data Latch with Asynchronous Clear and Preset and Gate Enable
LDCPE_1	Primitive: Transparent Data Latch with Asynchronous Clear and Preset, Gate Enable, and Inverted Gate
LDE	Primitive: Transparent Data Latch with Gate Enable
LDE_1	Primitive: Transparent Data Latch with Gate Enable and Inverted Gate
LDP	Primitive: Macro: Transparent Data Latch with Asynchronous Preset
LDP_1	Primitive: Transparent Data Latch with Asynchronous Preset and Inverted Gate
LDPE	Primitive: Transparent Data Latch with Asynchronous Preset and Gate Enable
LDPE_1	Primitive: Transparent Data Latch with Asynchronous Preset, Gate Enable, and Inverted Gate

Logic

Design Element	Description
AND12	Macro: 12- Input AND Gate with Non-Inverted Inputs
AND16	Macro: 16- Input AND Gate with Non-Inverted Inputs
AND2	Primitive: 2-Input AND Gate with Non-Inverted Inputs
AND2B1	Primitive: 2-Input AND Gate with 1 Inverted and 1 Non-Inverted Inputs
AND2B2	Primitive: 2-Input AND Gate with Inverted Inputs
AND3	Primitive: 3-Input AND Gate with Non-Inverted Inputs
AND3B1	Primitive: 3-Input AND Gate with 1 Inverted and 2 Non-Inverted Inputs
AND3B2	Primitive: 3-Input AND Gate with 2 Inverted and 1 Non-Inverted Inputs

Design Element	Description
AND3B3	Primitive: 3-Input AND Gate with Inverted Inputs
AND4	Primitive: 4-Input AND Gate with Non-Inverted Inputs
AND4B1	Primitive: 4-Input AND Gate with 1 Inverted and 3 Non-Inverted Inputs
AND4B2	Primitive: 4-Input AND Gate with 2 Inverted and 2 Non-Inverted Inputs
AND4B3	Primitive: 4-Input AND Gate with 3 Inverted and 1 Non-Inverted Inputs
AND4B4	Primitive: 4-Input AND Gate with Inverted Inputs
AND5	Primitive: 5-Input AND Gate with Non-Inverted Inputs
AND5B1	Primitive: 5-Input AND Gate with 1 Inverted and 4 Non-Inverted Inputs
AND5B2	Primitive: 5-Input AND Gate with 2 Inverted and 3 Non-Inverted Inputs
AND5B3	Primitive: 5-Input AND Gate with 3 Inverted and 2 Non-Inverted Inputs
AND5B4	Primitive: 5-Input AND Gate with 4 Inverted and 1 Non-Inverted Inputs
AND5B5	Primitive: 5-Input AND Gate with Inverted Inputs
AND6	Macro: 6-Input AND Gate with Non-Inverted Inputs
AND7	Macro: 7-Input AND Gate with Non-Inverted Inputs
AND8	Macro: 8-Input AND Gate with Non-Inverted Inputs
AND9	Macro: 9-Input AND Gate with Non-Inverted Inputs
INV	Primitive: Inverter
INV16	Macro: 16 Inverters
INV4	Macro: Four Inverters
INV8	Macro: Eight Inverters
NAND12	Macro: 12- Input NAND Gate with Non-Inverted Inputs
NAND16	Macro: 16- Input NAND Gate with Non-Inverted Inputs
NAND2	Primitive: 2-Input NAND Gate with Non-Inverted Inputs
NAND2B1	Primitive: 2-Input NAND Gate with 1 Inverted and 1 Non-Inverted Inputs
NAND2B2	Primitive: 2-Input NAND Gate with Inverted Inputs
NAND3	Primitive: 3-Input NAND Gate with Non-Inverted Inputs
NAND3B1	Primitive: 3-Input NAND Gate with 1 Inverted and 2 Non-Inverted Inputs
NAND3B2	Primitive: 3-Input NAND Gate with 2 Inverted and 1 Non-Inverted Inputs
NAND3B3	Primitive: 3-Input NAND Gate with Inverted Inputs
NAND4	Primitive: 4-Input NAND Gate with Non-Inverted Inputs
NAND4B1	Primitive: 4-Input NAND Gate with 1 Inverted and 3 Non-Inverted Inputs
NAND4B2	Primitive: 4-Input NAND Gate with 2 Inverted and 2 Non-Inverted Inputs
NAND4B3	Primitive: 4-Input NAND Gate with 3 Inverted and 1 Non-Inverted Inputs
NAND4B4	Primitive: 4-Input NAND Gate with Inverted Inputs
NAND5	Primitive: 5-Input NAND Gate with Non-Inverted Inputs
NAND5B1	Primitive: 5-Input NAND Gate with 1 Inverted and 4 Non-Inverted Inputs
NAND5B2	Primitive: 5-Input NAND Gate with 2 Inverted and 3 Non-Inverted Inputs
NAND5B3	Primitive: 5-Input NAND Gate with 3 Inverted and 2 Non-Inverted Inputs

Design Element	Description
NAND5B4	Primitive: 5-Input NAND Gate with 4 Inverted and 1 Non-Inverted Inputs
NAND5B5	Primitive: 5-Input NAND Gate with Inverted Inputs
NAND6	Macro: 6-Input NAND Gate with Non-Inverted Inputs
NAND7	Macro: 7-Input NAND Gate with Non-Inverted Inputs
NAND8	Macro: 8-Input NAND Gate with Non-Inverted Inputs
NAND9	Macro: 9-Input NAND Gate with Non-Inverted Inputs
NOR12	Macro: 12-Input NOR Gate with Non-Inverted Inputs
NOR16	Macro: 16-Input NOR Gate with Non-Inverted Inputs
NOR2	Primitive: 2-Input NOR Gate with Non-Inverted Inputs
NOR2B1	Primitive: 2-Input NOR Gate with 1 Inverted and 1 Non-Inverted Inputs
NOR2B2	Primitive: 2-Input NOR Gate with Inverted Inputs
NOR3	Primitive: 3-Input NOR Gate with Non-Inverted Inputs
NOR3B1	Primitive: 3-Input NOR Gate with 1 Inverted and 2 Non-Inverted Inputs
NOR3B2	Primitive: 3-Input NOR Gate with 2 Inverted and 1 Non-Inverted Inputs
NOR3B3	Primitive: 3-Input NOR Gate with Inverted Inputs
NOR4	Primitive: 4-Input NOR Gate with Non-Inverted Inputs
NOR4B1	Primitive: 4-Input NOR Gate with 1 Inverted and 3 Non-Inverted Inputs
NOR4B2	Primitive: 4-Input NOR Gate with 2 Inverted and 2 Non-Inverted Inputs
NOR4B3	Primitive: 4-Input NOR Gate with 3 Inverted and 1 Non-Inverted Inputs
NOR4B4	Primitive: 4-Input NOR Gate with Inverted Inputs
NOR5	Primitive: 5-Input NOR Gate with Non-Inverted Inputs
NOR5B1	Primitive: 5-Input NOR Gate with 1 Inverted and 4 Non-Inverted Inputs
NOR5B2	Primitive: 5-Input NOR Gate with 2 Inverted and 3 Non-Inverted Inputs
NOR5B3	Primitive: 5-Input NOR Gate with 3 Inverted and 2 Non-Inverted Inputs
NOR5B4	Primitive: 5-Input NOR Gate with 4 Inverted and 1 Non-Inverted Inputs
NOR5B5	Primitive: 5-Input NOR Gate with Inverted Inputs
NOR6	Macro: 6-Input NOR Gate with Non-Inverted Inputs
NOR7	Macro: 7-Input NOR Gate with Non-Inverted Inputs
NOR8	Macro: 8-Input NOR Gate with Non-Inverted Inputs
NOR9	Macro: 9-Input NOR Gate with Non-Inverted Inputs
OR12	Macro: 12-Input OR Gate with Non-Inverted Inputs
OR16	Macro: 16-Input OR Gate with Non-Inverted Inputs
OR2	Primitive: 2-Input OR Gate with Non-Inverted Inputs
OR2B1	Primitive: 2-Input OR Gate with 1 Inverted and 1 Non-Inverted Inputs
OR2B2	Primitive: 2-Input OR Gate with Inverted Inputs
OR3	Primitive: 3-Input OR Gate with Non-Inverted Inputs
OR3B1	Primitive: 3-Input OR Gate with 1 Inverted and 2 Non-Inverted Inputs
OR3B2	Primitive: 3-Input OR Gate with 2 Inverted and 1 Non-Inverted Inputs

Design Element	Description
OR3B3	Primitive: 3-Input OR Gate with Inverted Inputs
OR4	Primitive: 4-Input OR Gate with Non-Inverted Inputs
OR4B1	Primitive: 4-Input OR Gate with 1 Inverted and 3 Non-Inverted Inputs
OR4B2	Primitive: 4-Input OR Gate with 2 Inverted and 2 Non-Inverted Inputs
OR4B3	Primitive: 4-Input OR Gate with 3 Inverted and 1 Non-Inverted Inputs
OR4B4	Primitive: 4-Input OR Gate with Inverted Inputs
OR5	Primitive: 5-Input OR Gate with Non-Inverted Inputs
OR5B1	Primitive: 5-Input OR Gate with 1 Inverted and 4 Non-Inverted Inputs
OR5B2	Primitive: 5-Input OR Gate with 2 Inverted and 3 Non-Inverted Inputs
OR5B3	Primitive: 5-Input OR Gate with 3 Inverted and 2 Non-Inverted Inputs
OR5B4	Primitive: 5-Input OR Gate with 4 Inverted and 1 Non-Inverted Inputs
OR5B5	Primitive: 5-Input OR Gate with Inverted Inputs
OR6	Macro: 6-Input OR Gate with Non-Inverted Inputs
OR7	Macro: 7-Input OR Gate with Non-Inverted Inputs
OR8	Macro: 8-Input OR Gate with Non-Inverted Inputs
OR9	Macro: 9-Input OR Gate with Non-Inverted Inputs
SOP3	Macro: 3-Input Sum of Products
SOP3B1A	Macro: 3-Input Sum of Products with One Inverted Input (Option A)
SOP3B1B	Macro: 3-Input Sum of Products with One Inverted Input (Option B)
SOP3B2A	Macro: 3-Input Sum of Products with Two Inverted Inputs (Option A)
SOP3B2B	Macro: 3-Input Sum of Products with Two Inverted Inputs (Option B)
SOP3B3	Macro: 3-Input Sum of Products with Inverted Inputs
SOP4	Macro: 4-Input Sum of Products
SOP4B1	Macro: 4-Input Sum of Products with One Inverted Input
SOP4B2A	Macro: 4-Input Sum of Products with Two Inverted Inputs (Option A)
SOP4B2B	Macro: 4-Input Sum of Products with Two Inverted Inputs (Option B)
SOP4B3	Macro: 4-Input Sum of Products with Three Inverted Inputs
SOP4B4	Macro: 4-Input Sum of Products with Inverted Inputs
XNOR2	Primitive: 2-Input XNOR Gate with Non-Inverted Inputs
XNOR3	Primitive: 3-Input XNOR Gate with Non-Inverted Inputs
XNOR4	Primitive: 4-Input XNOR Gate with Non-Inverted Inputs
XNOR5	Primitive: 5-Input XNOR Gate with Non-Inverted Inputs
XNOR6	Macro: 6-Input XNOR Gate with Non-Inverted Inputs
XNOR7	Macro: 7-Input XNOR Gate with Non-Inverted Inputs
XNOR8	Macro: 8-Input XNOR Gate with Non-Inverted Inputs
XNOR9	Macro: 9-Input XNOR Gate with Non-Inverted Inputs
XOR2	Primitive: 2-Input XOR Gate with Non-Inverted Inputs
XOR3	Primitive: 3-Input XOR Gate with Non-Inverted Inputs

Design Element	Description
XOR4	Primitive: 4-Input XOR Gate with Non-Inverted Inputs
XOR5	Primitive: 5-Input XOR Gate with Non-Inverted Inputs
XOR6	Macro: 6-Input XOR Gate with Non-Inverted Inputs
XOR7	Macro: 7-Input XOR Gate with Non-Inverted Inputs
XOR8	Macro: 8-Input XOR Gate with Non-Inverted Inputs
XOR9	Macro: 9-Input XOR Gate with Non-Inverted Inputs

LUT

Design Element	Description
CFGLUT5	Primitive: 5-input Dynamically Reconfigurable Look-Up Table (LUT)
LUT1	Macro: 1-Bit Look-Up Table with General Output
LUT1_D	Macro: 1-Bit Look-Up Table with Dual Output
LUT1_L	Macro: 1-Bit Look-Up Table with Local Output
LUT2	Macro: 2-Bit Look-Up Table with General Output
LUT2_D	Macro: 2-Bit Look-Up Table with Dual Output
LUT2_L	Macro: 2-Bit Look-Up Table with Local Output
LUT3	Macro: 3-Bit Look-Up Table with General Output
LUT3_D	Macro: 3-Bit Look-Up Table with Dual Output
LUT3_L	Macro: 3-Bit Look-Up Table with Local Output
LUT4	Macro: 4-Bit Look-Up-Table with General Output
LUT4_D	Macro: 4-Bit Look-Up Table with Dual Output
LUT4_L	Macro: 4-Bit Look-Up Table with Local Output
LUT5	Primitive: 5-Input Lookup Table with General Output
LUT5_D	Primitive: 5-Input Lookup Table with General and Local Outputs
LUT5_L	Primitive: 5-Input Lookup Table with Local Output
LUT6	Primitive: 6-Input Lookup Table with General Output
LUT6_2	Primitive: Six-input, 2-output, Look-Up Table
LUT6_D	Primitive: 6-Input Lookup Table with General and Local Outputs
LUT6_L	Primitive: 6-Input Lookup Table with Local Output

Memory

Design Element	Description
FIFO18	Primitive: 18kb FIFO (First In, First Out) Block RAM Memory
FIFO18_36	Primitive: 36-bit Wide by 512 Deep 18kb FIFO (First In, First Out) Block RAM Memory
FIFO36	Primitive: 36kb FIFO (First In, First Out) Block RAM Memory
FIFO36_72	Primitive: 72-Bit Wide by 512 Deep 36kb FIFO (First In, First Out) Block RAM Memory with ECC (Error Detection and Correction Circuitry)
RAM128X1D	Primitive: 128-Deep by 1-Wide Dual Port Random Access Memory (Select RAM)
RAM16X1D	Primitive: 16-Deep by 1-Wide Static Dual Port Synchronous RAM
RAM16X1D_1	Primitive: 16-Deep by 1-Wide Static Dual Port Synchronous RAM with Negative-Edge Clock
RAM16X1S	Primitive: 16-Deep by 1-Wide Static Synchronous RAM
RAM16X1S_1	Primitive: 16-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock
RAM16X2S	Primitive: 16-Deep by 2-Wide Static Synchronous RAM
RAM16X4S	Primitive: 16-Deep by 4-Wide Static Synchronous RAM
RAM16X8S	Primitive: 16-Deep by 8-Wide Static Synchronous RAM
RAM256X1S	Primitive: 256-Deep by 1-Wide Random Access Memory (Select RAM)
RAM32M	Primitive: 32-Deep by 8-bit Wide Multi Port Random Access Memory (Select RAM)
RAM32X1D	Primitive: 32-Deep by 1-Wide Static Dual Port Synchronous RAM
RAM32X1S	Primitive: 32-Deep by 1-Wide Static Synchronous RAM
RAM32X1S_1	Primitive: 32-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock
RAM32X2S	Primitive: 32-Deep by 2-Wide Static Synchronous RAM
RAM32X4S	Primitive: 32-Deep by 4-Wide Static Synchronous RAM
RAM32X8S	Primitive: 32-Deep by 8-Wide Static Synchronous RAM
RAM64M	Primitive: 64-Deep by 4-bit Wide Multi Port Random Access Memory (Select RAM)
RAM64X1D	Primitive: 64-Deep by 1-Wide Dual Port Static Synchronous RAM
RAM64X1S	Primitive: 64-Deep by 1-Wide Static Synchronous RAM
RAM64X1S_1	Primitive: 64-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock
RAM64X2S	Primitive: 64-Deep by 2-Wide Static Synchronous RAM
RAMB18	Primitive: 18K-bit Configurable Synchronous True Dual Port Block RAM
RAMB18SDP	Primitive: 36-bit by 512 Deep, 18kb Synchronous Simple Dual Port Block RAM
RAMB36	Primitive: 36kb Configurable Synchronous True Dual Port Block RAM
RAMB36SDP	Primitive: 72-bit by 512 Deep, 36kb Synchronous Simple Dual Port Block RAM with ECC (Error Correction Circuitry)
ROM128X1	Primitive: 128-Deep by 1-Wide ROM
ROM16X1	Primitive: 16-Deep by 1-Wide ROM
ROM256X1	Primitive: 256-Deep by 1-Wide ROM
ROM32X1	Primitive: 32-Deep by 1-Wide ROM
ROM64X1	Primitive: 64-Deep by 1-Wide ROM

MUX

Design Element	Description
M16_1E	Macro: 16-to-1 Multiplexer with Enable
M2_1	Macro: 2-to-1 Multiplexer
M2_1B1	Macro: 2-to-1 Multiplexer with D0 Inverted
M2_1B2	Macro: 2-to-1 Multiplexer with D0 and D1 Inverted
M2_1E	Macro: 2-to-1 Multiplexer with Enable
M4_1E	Macro: 4-to-1 Multiplexer with Enable
M8_1E	Macro: 8-to-1 Multiplexer with Enable
MUXF7	Primitive: 2-to-1 Look-Up Table Multiplexer with General Output
MUXF7_D	Primitive: 2-to-1 Look-Up Table Multiplexer with Dual Output
MUXF7_L	Primitive: 2-to-1 look-up table Multiplexer with Local Output
MUXF8	Primitive: 2-to-1 Look-Up Table Multiplexer with General Output
MUXF8_D	Primitive: 2-to-1 Look-Up Table Multiplexer with Dual Output
MUXF8_L	Primitive: 2-to-1 Look-Up Table Multiplexer with Local Output

Shift Register

Design Element	Description
SR16CE	Macro: 16-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear
SR16CLE	Macro: 16-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear
SR16CLED	Macro: 16-Bit Shift Register with Clock Enable and Asynchronous Clear
SR16RE	Macro: 16-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset
SR16RLE	Macro: 16-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset
SR16RLED	Macro: 16-Bit Shift Register with Clock Enable and Synchronous Reset
SR4CE	Macro: 4-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear
SR4CLE	Macro: 4-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear
SR4CLED	Macro: 4-Bit Shift Register with Clock Enable and Asynchronous Clear
SR4RE	Macro: 4-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset
SR4RLE	Macro: 4-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset
SR4RLED	Macro: 4-Bit Shift Register with Clock Enable and Synchronous Reset
SR8CE	Macro: 8-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear
SR8CLE	Macro: 8-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear

Design Element	Description
SR8CLED	Macro: 8-Bit Shift Register with Clock Enable and Asynchronous Clear
SR8RE	Macro: 8-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset
SR8RLE	Macro: 8-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset
SR8RLED	Macro: 8-Bit Shift Register with Clock Enable and Synchronous Reset
SRL16	Primitive: 16-Bit Shift Register Look-Up Table (LUT)
SRL16_1	Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Negative-Edge Clock
SRL16E	Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Clock Enable
SRL16E_1	Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Negative-Edge Clock and Clock Enable
SRLC16	Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Carry
SRLC16_1	Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Carry and Negative-Edge Clock
SRLC16E	Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Carry and Clock Enable
SRLC16E_1	Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Carry, Negative-Edge Clock, and Clock Enable
SRLC32E	Primitive: 32 Clock Cycle, Variable Length Shift Register Look-Up Table (LUT) with Clock Enable

Shifter

Design Element	Description
BRLSHFT4	Macro: 4-Bit Barrel Shifter
BRLSHFT8	Macro: 8-Bit Barrel Shifter

About Design Elements

This section describes the design elements that can be used with this architecture. The design elements are organized alphabetically.

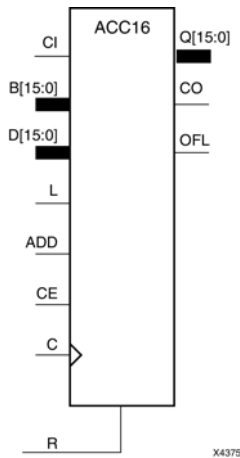
The following information is provided for each design element, where applicable:

- Name of element
- Brief description
- Schematic symbol (if any)
- Logic Table (if any)
- Port Descriptions (if any)
- Design Entry Method
- Available Attributes (if any)
- For more information

You can find examples of VHDL and Verilog instantiation code in the ISE software (in the main menu, select **Edit > Language Templates** or in the *Libraries Guide for HDL Designs* for this architecture.

ACC16

Macro: 16-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset



Introduction

This design element can add or subtract a 16-bit unsigned-binary, respectively or two's-complement word to or from the contents of a 16-bit data register and store the results in the register. The register can be loaded with the 16-bit word.

When the load input (L) is High, CE is ignored and the data on the D inputs is loaded into the register during the Low-to-High clock (C) transition. ACC16 loads the data on inputs D15 : D0 into the 16-bit register.

This design element operates on either 16-bit unsigned binary numbers or 16-bit two's-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is how they determine when "overflow" occurs. Unsigned binary uses carry-out (CO), while two's complement uses OFL to determine when "overflow" occurs.

- For unsigned binary operation, ACC16 can represent numbers between 0 and 15, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtractor. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds. The carry-out (CO) is not registered synchronously with the data outputs. CO always reflects the accumulation of the B inputs (B15 : B0 for ACC16). This allows the cascading of ACC16s by connecting CO of one stage to CI of the next stage. An unsigned binary "overflow" that is always active-High can be generated by gating the ADD signal and CO as follows:

$\text{unsigned overflow} = \text{CO} \text{ XOR } \text{ADD}$

Ignore OFL in unsigned binary operation.

- For two's-complement operation, ACC16 represents numbers between -8 and +7, inclusive. If an addition or subtraction operation result exceeds this range, the OFL output goes High. The overflow (OFL) is not registered synchronously with the data outputs. OFL always reflects the accumulation of the B inputs (B15 : B0 for ACC16) and the contents of the register, which allows cascading of ACC16s by connecting OFL of one stage to CI of the next stage.

Ignore CO in two's-complement operation.

The synchronous reset (R) has priority over all other inputs, and when set to High, causes all outputs to go to logic level zero during the Low-to-High clock (C) transition. Clock (C) transitions are ignored when clock enable (CE) is Low.

This design element is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Input						Output
R	L	CE	ADD	D	C	Q
1	x	x	x	x	↑	0
0	1	x	x	Dn	↑	Dn
0	0	1	1	x	↑	$Q0+Bn+CI$
0	0	1	0	x	↑	$Q0-Bn-CI$
0	0	0	x	x	↑	No Change
Q0: Previous value of Q Bn: Value of Data input B CI: Value of input CI						

Design Entry Method

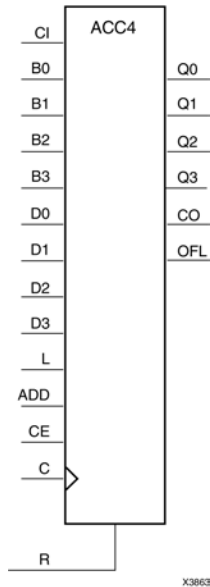
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

ACC4

Macro: 4-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset



Introduction

This design element can add or subtract a 4-bit unsigned-binary, respectively or two's-complement word to or from the contents of a 4-bit data register and store the results in the register. The register can be loaded with the 4-bit word.

When the load input (L) is High, CE is ignored and the data on the D inputs is loaded into the register during the Low-to-High clock (C) transition. ACC4 loads the data on inputs D3 : D0 into the 4-bit register.

This design element operates on either 4-bit unsigned binary numbers or 4-bit two's-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is how they determine when "overflow" occurs. Unsigned binary uses carry-out (CO), while two's complement uses OFL to determine when "overflow" occurs.

- For unsigned binary operation, ACC4 can represent numbers between 0 and 15, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtractor. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds. The carry-out (CO) is not registered synchronously with the data outputs. CO always reflects the accumulation of the B inputs (B3 : B0 for ACC4). This allows the cascading of ACC4s by connecting CO of one stage to CI of the next stage. An unsigned binary "overflow" that is always active-High can be generated by gating the ADD signal and CO as follows:

`unsigned overflow = CO XOR ADD`

Ignore OFL in unsigned binary operation.

- For two's-complement operation, ACC4 represents numbers between -8 and +7, inclusive. If an addition or subtraction operation result exceeds this range, the OFL output goes High. The overflow (OFL) is not registered synchronously with the data outputs. OFL always reflects the accumulation of the B inputs (B3 : B0 for ACC4) and the contents of the register, which allows cascading of ACC4s by connecting OFL of one stage to CI of the next stage.

Ignore CO in two's-complement operation.

The synchronous reset (R) has priority over all other inputs, and when set to High, causes all outputs to go to logic level zero during the Low-to-High clock (C) transition. Clock (C) transitions are ignored when clock enable (CE) is Low.

This design element is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Input						Output
R	L	CE	ADD	D	C	Q
1	x	x	x	x	↑	0
0	1	x	x	Dn	↑	Dn
0	0	1	1	x	↑	Q0+Bn+CI
0	0	1	0	x	↑	Q0-Bn-CI
0	0	0	x	x	↑	No Change
Q0: Previous value of Q Bn: Value of Data input B CI: Value of input CI						

Design Entry Method

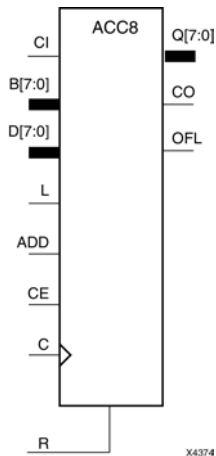
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

ACC8

Macro: 8-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset



Introduction

This design element can add or subtract a 8-bit unsigned-binary, respectively or two's-complement word to or from the contents of a 8-bit data register and store the results in the register. The register can be loaded with the 8-bit word.

When the load input (L) is High, CE is ignored and the data on the D inputs is loaded into the register during the Low-to-High clock (C) transition. ACC8 loads the data on inputs D7 : D0 into the 8-bit register.

This design element operates on either 8-bit unsigned binary numbers or 8-bit two's-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is how they determine when "overflow" occurs. Unsigned binary uses carry-out (CO), while two's complement uses OFL to determine when "overflow" occurs.

- For unsigned binary operation, ACC8 can represent numbers between 0 and 255, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtractor. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds. The carry-out (CO) is not registered synchronously with the data outputs. CO always reflects the accumulation of the B inputs (B3 : B0 for ACC4). This allows the cascading of ACC8s by connecting CO of one stage to CI of the next stage. An unsigned binary "overflow" that is always active-High can be generated by gating the ADD signal and CO as follows:

$\text{unsigned overflow} = \text{CO} \text{ XOR } \text{ADD}$

Ignore OFL in unsigned binary operation.

- For two's-complement operation, ACC8 represents numbers between -128 and +127, inclusive. If an addition or subtraction operation result exceeds this range, the OFL output goes High. The overflow (OFL) is not registered synchronously with the data outputs. OFL always reflects the accumulation of the B inputs (B3 : B0 for ACC8) and the contents of the register, which allows cascading of ACC8s by connecting OFL of one stage to CI of the next stage.

Ignore CO in two's-complement operation.

The synchronous reset (R) has priority over all other inputs, and when set to High, causes all outputs to go to logic level zero during the Low-to-High clock (C) transition. Clock (C) transitions are ignored when clock enable (CE) is Low.

This design element is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Input						Output
R	L	CE	ADD	D	C	Q
1	x	x	x	x	↑	0
0	1	x	x	Dn	↑	Dn
0	0	1	1	x	↑	Q0+Bn+CI
0	0	1	0	x	↑	Q0-Bn-CI
0	0	0	x	x	↑	No Change
Q0: Previous value of Q Bn: Value of Data input B CI: Value of input CI						

Design Entry Method

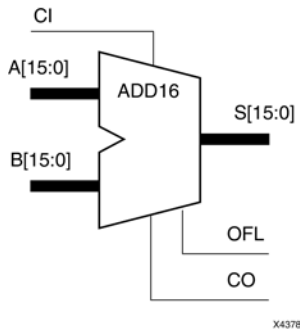
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

ADD16

Macro: 16-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow



Introduction

This design element adds two words and a carry-in (CI), producing a sum output and carry-out (CO) or overflow (OFL). The factors added are A15:A0, B15:B0 and CI, producing the sum output S15:S0 and CO (or OFL).

Logic Table

Input		Output
A	B	S
A _n	B _n	A _n +B _n +CI
CI: Value of input CI.		

Unsigned Binary Versus Two's Complement

This design element can operate on either 16-bit unsigned binary numbers or 16-bit two's-complement numbers, respectively. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is the way they determine when "overflow" occurs. Unsigned binary uses CO, while two's-complement uses OFL to determine when "overflow" occurs. To interpret the inputs as unsigned binary, follow the CO output. To interpret the inputs as two's complement, follow the OFL output.

Unsigned Binary Operation

For unsigned binary operation, this element represents numbers between 0 and 65535, inclusive. OFL is ignored in unsigned binary operation.

Two's-Complement Operation

For two's-complement operation, this element can represent numbers between -32768 and +32767, inclusive. OFL is active (High) when the sum exceeds the bounds of the adder. CO is ignored in two's-complement operation.

Design Entry Method

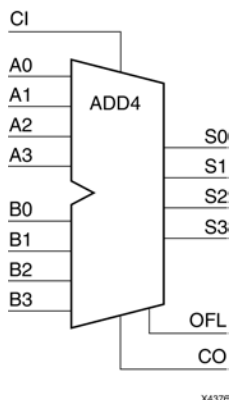
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

ADD4

Macro: 4-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow



Introduction

This design element adds two words and a carry-in (CI), producing a sum output and carry-out (CO) or overflow (OFL). The factors added are A3:A0, B3:B0, and CI producing the sum output S3:S0 and CO (or OFL).

Logic Table

Input		Output
A	B	S
A _n	B _n	A _n +B _n +CI
CI: Value of input CI.		

Unsigned Binary Versus Two's Complement

This design element can operate on either 4-bit unsigned binary numbers or 4-bit two's-complement numbers, respectively. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is the way they determine when "overflow" occurs. Unsigned binary uses CO, while two's-complement uses OFL to determine when "overflow" occurs. To interpret the inputs as unsigned binary, follow the CO output. To interpret the inputs as two's complement, follow the OFL output.

Unsigned Binary Operation

For unsigned binary operation, this element represents numbers from 0 to 15, inclusive. OFL is ignored in unsigned binary operation.

Two's-Complement Operation

For two's-complement operation, this element can represent numbers between -8 and +7, inclusive. OFL is active (High) when the sum exceeds the bounds of the adder. CO is ignored in two's-complement operation.

Design Entry Method

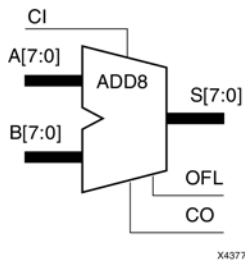
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

ADD8

Macro: 8-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow



Introduction

This design element adds two words and a carry-in (CI), producing a sum output and carry-out (CO) or overflow (OFL). The factors added are A7:A0, B7:B0, and CI, producing the sum output S7:S0 and CO (or OFL).

Logic Table

Input		Output
A	B	S
A _n	B _n	A _n +B _n +CI
CI: Value of input CI.		

Unsigned Binary Versus Two's Complement

This design element can operate on either 8-bit unsigned binary numbers or 8-bit two's-complement numbers, respectively. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is the way they determine when "overflow" occurs. Unsigned binary uses CO, while two's-complement uses OFL to determine when "overflow" occurs. To interpret the inputs as unsigned binary, follow the CO output. To interpret the inputs as two's complement, follow the OFL output.

Unsigned Binary Operation

For unsigned binary operation, this element represents numbers between 0 and 255, inclusive. OFL is ignored in unsigned binary operation.

Two's-Complement Operation

For two's-complement operation, this element can represent numbers between -128 and +127, inclusive. OFL is active (High) when the sum exceeds the bounds of the adder. CO is ignored in two's-complement operation.

Design Entry Method

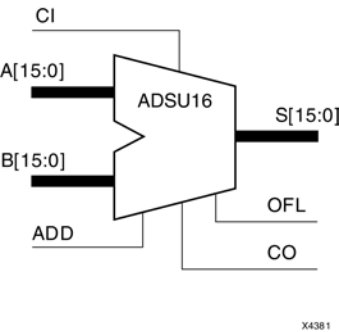
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

ADSU16

Macro: 16-Bit Cascadable Adder/Subtractor with Carry-In, Carry-Out, and Overflow



Introduction

When the ADD input is High, this element adds two 16-bit words (A15:A0 and B15:B0) and a carry-in (CI), producing a 16-bit sum output (S15:S0) and carry-out (CO) or overflow (OFL).

When the ADD input is Low, this element subtracts B15:B0 from A15:A0, producing a difference output and a carry-out (CO) or an overflow (OFL).

In add mode, CO and CI are active-High. In subtract mode, CO and CI are active-Low. OFL is active-High in add and subtract modes.

Logic Table

Input			Output
ADD	A	B	S
1	An	Bn	An+Bn+CI*
0	An	Bn	An-Bn-CI*
CI*: ADD = 0, CI, CO active LOW			
CI*: ADD = 1, CI, CO active HIGH			

Unsigned Binary Versus Two's Complement

This design element can operate on either 16-bit unsigned binary numbers or 16-bit two's-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is the way they determine when "overflow" occurs. Unsigned binary uses CO, while two's complement uses OFL to determine when "overflow" occurs.

With adder/subtractors, either unsigned binary or two's-complement operations cause an overflow. If the result crosses the overflow boundary, an overflow is generated. Similarly, when the result crosses the carry-out boundary, a carry-out is generated.

Unsigned Binary Operation

For unsigned binary operation, this element can represent numbers between 0 and 65535, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtractor. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds.

An unsigned binary "overflow" that is always active-High can be generated by gating the ADD signal and CO as follows:

`unsigned overflow = CO XOR ADD`

OFL is ignored in unsigned binary operation.

Two's-Complement Operation

For two's-complement operation, this element can represent numbers between -32768 and +32767, inclusive.

If an addition or subtraction operation result exceeds this range, the OFL output goes High. CO is ignored in two's-complement operation.

Design Entry Method

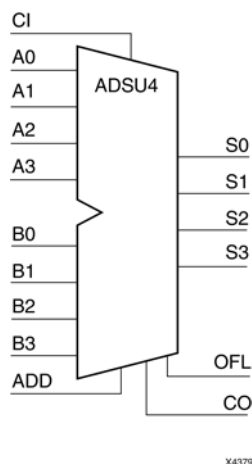
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

ADSU4

Macro: 4-Bit Cascadable Adder/Subtractor with Carry-In, Carry-Out, and Overflow



Introduction

When the ADD input is High, this element adds two 4-bit words (A3:A0 and B3:B0) and a carry-in (CI), producing a 4-bit sum output (S3:S0) and a carry-out (CO) or an overflow (OFL).

When the ADD input is Low, this element subtracts B3:B0 from A3:A0, producing a 4-bit difference output (S3:S0) and a carry-out (CO) or an overflow (OFL).

In add mode, CO and CI are active-High. In subtract mode, CO and CI are active-Low. OFL is active-High in add and subtract modes.

Logic Table

Input			Output
ADD	A	B	S
1	A _n	B _n	A _n +B _n +CI*
0	A _n	B _n	A _n -B _n -CI*
CI*: ADD = 0, CI, CO active LOW			
CI*: ADD = 1, CI, CO active HIGH			

Unsigned Binary Versus Two's Complement

This design element can operate on either 4-bit unsigned binary numbers or 4-bit two's-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is the way they determine when "overflow" occurs. Unsigned binary uses CO, while two's complement uses OFL to determine when "overflow" occurs.

With adder/subtractors, either unsigned binary or two's-complement operations cause an overflow. If the result crosses the overflow boundary, an overflow is generated. Similarly, when the result crosses the carry-out boundary, a carry-out is generated.

Unsigned Binary Operation

For unsigned binary operation, ADSU4 can represent numbers between 0 and 15, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtractor. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds.

An unsigned binary “overflow” that is always active-High can be generated by gating the ADD signal and CO as follows:

`unsigned overflow = CO XOR ADD`

OFL is ignored in unsigned binary operation.

Two's-Complement Operation

For two's-complement operation, this element can represent numbers between -8 and +7, inclusive.

If an addition or subtraction operation result exceeds this range, the OFL output goes High. CO is ignored in two's-complement operation.

Design Entry Method

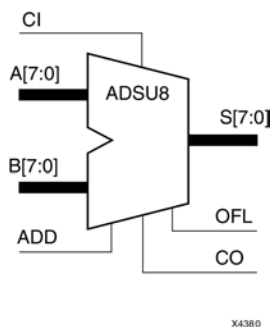
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

ADSU8

Macro: 8-Bit Cascadable Adder/Subtractor with Carry-In, Carry-Out, and Overflow



Introduction

When the ADD input is High, this element adds two 8-bit words (A7:A0 and B7:B0) and a carry-in (CI), producing an 8-bit sum output (S7:S0) and carry-out (CO) or an overflow (OFL).

When the ADD input is Low, this element subtracts B7:B0 from A7:A0, producing an 8-bit difference output (S7:S0) and a carry-out (CO) or an overflow (OFL).

In add mode, CO and CI are active-High. In subtract mode, CO and CI are active-Low. OFL is active-High in add and subtract modes.

Logic Table

Input			Output
ADD	A	B	S
1	A _n	B _n	A _n +B _n +CI*
0	A _n	B _n	A _n -B _n -CI*
CI*: ADD = 0, CI, CO active LOW			
CI*: ADD = 1, CI, CO active HIGH			

Unsigned Binary Versus Two's Complement

This design element can operate on either 8-bit unsigned binary numbers or 8-bit two's-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is the way they determine when "overflow" occurs. Unsigned binary uses CO, while two's complement uses OFL to determine when "overflow" occurs.

With adder/subtractors, either unsigned binary or two's-complement operations cause an overflow. If the result crosses the overflow boundary, an overflow is generated. Similarly, when the result crosses the carry-out boundary, a carry-out is generated.

Unsigned Binary Operation

For unsigned binary operation, this element can represent numbers between 0 and 255, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtractor. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds.

An unsigned binary "overflow" that is always active-High can be generated by gating the ADD signal and CO as follows:

unsigned overflow = CO XOR ADD

OFL is ignored in unsigned binary operation.

Two's-Complement Operation

For two's-complement operation, this element can represent numbers between -128 and +127, inclusive.

If an addition or subtraction operation result exceeds this range, the OFL output goes High. CO is ignored in two's-complement operation.

Design Entry Method

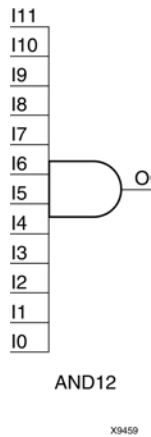
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

AND12

Macro: 12- Input AND Gate with Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

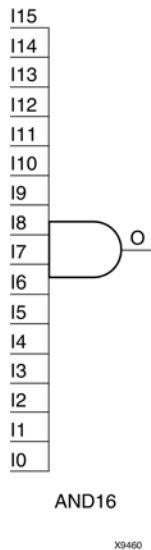
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

AND16

Macro: 16- Input AND Gate with Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

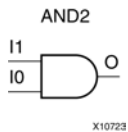
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

AND2

Primitive: 2-Input AND Gate with Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

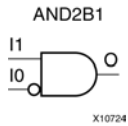
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

AND2B1

Primitive: 2-Input AND Gate with 1 Inverted and 1 Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

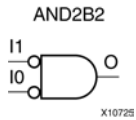
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

AND2B2

Primitive: 2-Input AND Gate with Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

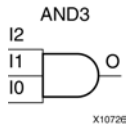
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

AND3

Primitive: 3-Input AND Gate with Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

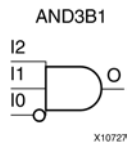
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

AND3B1

Primitive: 3-Input AND Gate with 1 Inverted and 2 Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

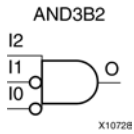
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

AND3B2

Primitive: 3-Input AND Gate with 2 Inverted and 1 Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

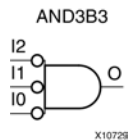
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

AND3B3

Primitive: 3-Input AND Gate with Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

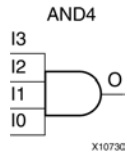
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

AND4

Primitive: 4-Input AND Gate with Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

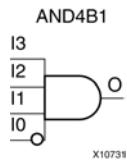
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

AND4B1

Primitive: 4-Input AND Gate with 1 Inverted and 3 Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

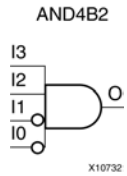
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

AND4B2

Primitive: 4-Input AND Gate with 2 Inverted and 2 Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

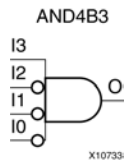
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

AND4B3

Primitive: 4-Input AND Gate with 3 Inverted and 1 Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

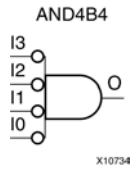
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

AND4B4

Primitive: 4-Input AND Gate with Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

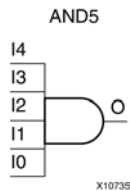
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

AND5

Primitive: 5-Input AND Gate with Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

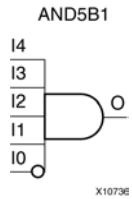
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

AND5B1

Primitive: 5-Input AND Gate with 1 Inverted and 4 Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

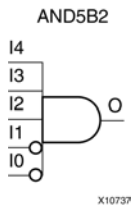
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

AND5B2

Primitive: 5-Input AND Gate with 2 Inverted and 3 Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

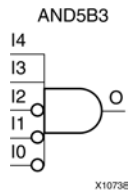
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

AND5B3

Primitive: 5-Input AND Gate with 3 Inverted and 2 Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

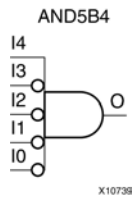
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

AND5B4

Primitive: 5-Input AND Gate with 4 Inverted and 1 Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

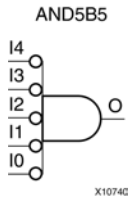
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

AND5B5

Primitive: 5-Input AND Gate with Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

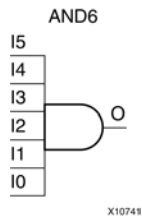
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

AND6

Macro: 6-Input AND Gate with Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

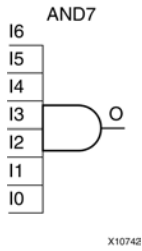
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

AND7

Macro: 7-Input AND Gate with Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

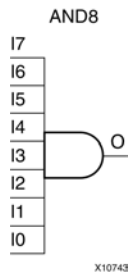
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

AND8

Macro: 8-Input AND Gate with Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

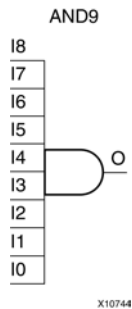
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

AND9

Macro: 9-Input AND Gate with Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

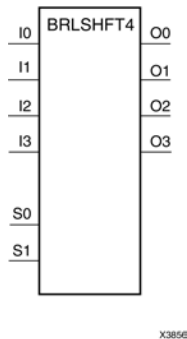
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

BRLSHFT4

Macro: 4-Bit Barrel Shifter



Introduction

This design element is a 4-bit barrel shifter that can rotate four inputs (I3 : I0) up to four places. The control inputs (S1 and S0) determine the number of positions, from one to four, that the data is rotated. The four outputs (O3 : O0) reflect the shifted data inputs.

Logic Table

Inputs						Outputs			
S1	S0	I0	I1	I2	I3	O0	O1	O2	O3
0	0	a	b	c	d	a	b	c	d
0	1	a	b	c	d	b	c	d	a
1	0	a	b	c	d	c	d	a	b
1	1	a	b	c	d	d	a	b	c

Design Entry Method

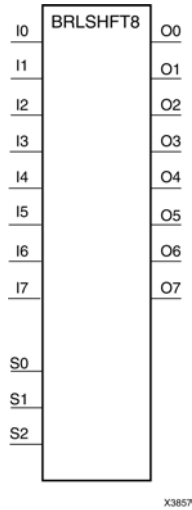
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

BRLSHFT8

Macro: 8-Bit Barrel Shifter



Introduction

This design element is an 8-bit barrel shifter, can rotate the eight inputs (I7 : I0) up to eight places. The control inputs (S2 : S0) determine the number of positions, from one to eight, that the data is rotated. The eight outputs (O7 : O0) reflect the shifted data inputs.

Logic Table

Inputs											Outputs							
S2	S1	S0	I0	I1	I2	I3	I4	I5	I6	I7	O0	O1	O2	O3	O4	O5	O6	O7
0	0	0	a	b	c	d	e	f	g	h	a	b	c	d	e	f	g	h
0	0	1	a	b	c	d	e	f	g	h	b	c	d	e	f	g	h	a
0	1	0	a	b	c	d	e	f	g	h	c	d	e	f	g	h	a	b
0	1	1	a	b	c	d	e	f	g	h	d	e	f	g	h	a	b	c
1	0	0	a	b	c	d	e	f	g	h	e	f	g	h	a	b	c	d
1	0	1	a	b	c	d	e	f	g	h	f	g	h	a	b	c	d	e
1	1	0	a	b	c	d	e	f	g	h	g	h	a	b	c	d	e	f
1	1	1	a	b	c	d	e	f	g	h	h	a	b	c	d	e	f	g

Design Entry Method

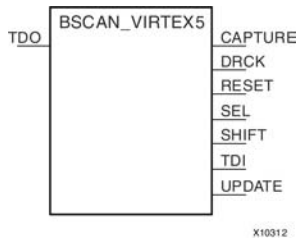
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

BSCAN_VIRTEX5

Primitive: Virtex®-5 JTAG Boundary-Scan Logic Access Circuit



Introduction

This design element allows access to and from internal logic by the JTAG Boundary Scan logic controller. This allows for communication between the internal running design and the dedicated JTAG pins of the FPGA.

Each instance of this design element will handle one JTAG USER instruction (USER1 through USER4) as set with the JTAG_CHAIN attribute. To handle all four USER instructions, instantiate four of these elements and set the JTAG_CHAIN attribute appropriately.

Note For specific information on boundary scan for an architecture, see the Programmable Logic Data Sheet for this element.

Port Descriptions

Port	Type	Width	Function
CAPTURE	Output	1	Active upon the loading of the USER instruction. Asserts High when the JTAG TAP controller is in the CAPTURE-DR state.
DRCK	Output	1	A mirror of the TCK input pin to the FPGA when the JTAG USER instruction assigned by JTAG_CHAIN is loaded and the JTAG TAP controller is in the SHIFT-DR state or in the CAPTURE-DR state.
RESET	Output	1	Active upon the loading of the USER instruction. It asserts High when the JTAG TAP controller is in the TEST-LOGIC-RESET state.
SEL	Output	1	Indicates when the USER instruction has been loaded into the JTAG Instruction Register. Becomes active in the UPDATE-IR state, and stays active until a new instruction is loaded.
SHIFT	Output	1	Active upon the loading of the USER instruction. It asserts High when the JTAG TAP controller is in the SHIFT-DR state.
TDI	Output	1	A mirror of the TDI pin.
UPDATE	Output	1	Active upon the loading of the USER instruction. It asserts High when the JTAG TAP controller is in the UPDATE-DR state.
TDO	Input	1	Active upon the loading of the USER instruction. External JTAG TDO pin will reflect data input to the macro's TDO1 pin.

Design Entry Method

This design element can be used in schematics.

Available Attributes

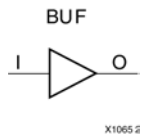
Attribute	Type	Allowed Values	Default	Description
JTAG_CHAIN	Integer	1, 2, 3, 4	1	Sets the JTAG USER instruction number that this instance of the element will handle.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

BUF

Primitive: General Purpose Buffer



Introduction

This is a general-purpose, non-inverting buffer.

This element is not necessary and is removed by the partitioning software (MAP).

Design Entry Method

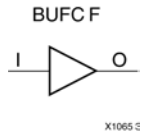
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

BUFCF

Primitive: Fast Connect Buffer



Introduction

This design element is a single fast connect buffer used to connect the outputs of the LUTs and some dedicated logic directly to the input of another LUT. Using this buffer implies CLB packing. No more than four LUTs may be connected together as a group.

Design Entry Method

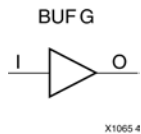
This design element can be used in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

BUFG

Primitive: Global Clock Buffer



Introduction

This design element is a high-fanout buffer that connects signals to the global routing resources for low skew distribution of the signal. BUFs are typically used on clock nets.

Port Descriptions

Port	Type	Width	Function
I	Input	1	Clock buffer output
O	Output	1	Clock buffer input

Design Entry Method

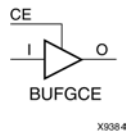
This design element can be used in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

BUFGCE

Primitive: Global Clock Buffer with Clock Enable



Introduction

This design element is a global clock buffer with a single gated input. Its O output is "0" when clock enable (CE) is Low (inactive). When clock enable (CE) is High, the I input is transferred to the O output.

Logic Table

Inputs		Outputs
I	CE	O
X	0	0
I	1	I

Design Entry Method

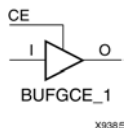
This design element can be used in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

BUFGCE_1

Primitive: Global Clock Buffer with Clock Enable and Output State 1



Introduction

This design element is a multiplexed global clock buffer with a single gated input. Its O output is High (1) when clock enable (CE) is Low (inactive). When clock enable (CE) is High, the I input is transferred to the O output.

Logic Table

Inputs		Outputs
I	CE	O
X	0	1
I	1	I

Design Entry Method

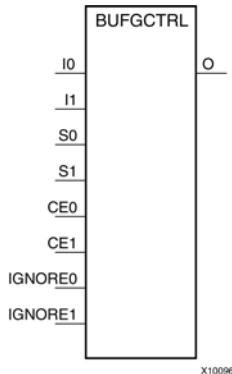
This design element can be used in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

BUFGCTRL

Primitive: Global Clock MUX Buffer



Introduction

BUFGCTRL primitive is global clock buffer that is designed as a synchronous/asynchronous "glitch free" 2:1 multiplexer with two clock inputs. Unlike global clock buffers that are found in previous generation of FPGAs, these clock buffers are designed with more control pins to provide a wider range of functionality and more robust input switching. BUFGCTRL is not limited to clocking applications.

Port Descriptions

Port	Type	Width	Function
O	Output	1	Clock Output pin
I	Input	1	Clock Input: I0 - Clock Input Pin I1 - Clock Input Pin
CE0, CE1	Input	1 (each)	Clock Enable Input. The CE pins represent the clock enable pin for each clock inputs and are used to select the clock inputs. A setup/hold time must be specified when you are using the CE pin to select inputs. Failure to meet this requirement could result in a clock glitch.
S0, S1	Input	1 (each)	Clock Select Input. The S pins represent the clock select pin for each clock inputs. When using the S pin as input select, there is a setup/hold time requirement. Unlike CE pins, failure to meet this requirement won't result in a clock glitch. However, it can cause the output clock to appear one clock cycle later.
IGNORE0, IGNORE1	Input	1 (each)	Clock Ignore Input. IGNORE pins are used whenever a designer wants to bypass the switching algorithm executed by the BUFGCTRL.

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT_OUT	Integer	0, 1	0	Initializes the BUFGCTRL output to the specified value after configuration.
PRESELECT_I0	Boolean	FALSE, TRUE	FALSE	If TRUE, BUFGCTRL output uses I0 input after configuration.
PRESELECT_I1	Boolean	FALSE, TRUE	FALSE	If TRUE, BUFGCTRL output uses I1 input after configuration.

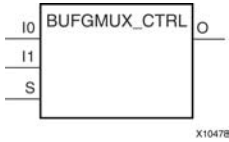
Note Both PRESELECT attributes might not be TRUE at the same time.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

BUFGMUX_CTRL

Primitive: 2-to-1 Global Clock MUX Buffer



Introduction

This design element is a global clock buffer with two clock inputs, one clock output, and a select line used to cleanly select between one of two clocks driving the global clocking resource. This component is based on BUFGCTRL, with some pins connected to logic High or Low. This element uses the S pin as the select pin for the 2-to-1 MUX. S can switch anytime without causing a glitch on the output clock of the buffer.

Port Descriptions

Port	Direction	Width	Function
O	Output	1 bit	Clock Output
I0	Input	1 bit	One of two Clock Inputs
I1	Input	1 bit	One of two Clock Inputs
S	Input	1 bit	Select for I0 (S=0) or I1 (S=1) Clock Output

Design Entry Method

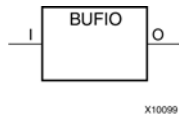
This design element can be used in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

BUFIO

Primitive: Local Clock Buffer for I/O



Introduction

This design element is a clock buffer. It is simply a clock-in, clock-out buffer. It drives a dedicated clock net within the I/O column, independent of the global clock resources. Thus, these elements are ideally suited for source-synchronous data capture (forwarded/receiver clock distribution). They can only be driven by clock capable I/Os located in the same clock region. They drive the two adjacent I/O clock nets (for a total of up to three clock regions), as well as the regional clock buffers (BUFR). These elements cannot drive logic resources (CLB, block RAM, etc.) because the I/O clock network only reaches the I/O column.

Port Descriptions

Port	Type	Width	Function
O	Output	1	Clock output
I	Input	1	Clock input

Design Entry Method

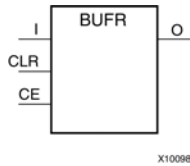
This design element can be used in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

BUFR

Primitive: Regional Clock Buffer for I/O and Logic Resources



Introduction

The BUFR is a clock buffer. BUFRs drive clock signals to a dedicated clock net within a clock region, independent from the global clock tree. BUFRs can drive the I/O logic and logic resources (CLB, block RAM, etc.) in the existing and adjacent clock regions. BUFRs can be driven by clock capable pins or local interconnect. In addition, BUFRs are capable of generating divided clock outputs with respect to the clock input. The divide value is an Integer between one and eight. BUFRs are ideal for source-synchronous applications requiring clock domain crossing or serial-to-parallel conversion. There are two BUFRs in a typical clock region (two regional clock networks). The center column does not have BUFRs.

Port Descriptions

Port	Type	Width	Function
CE	Input	1	Clock enable port. When asserted Low, this port \ndisables the output clock at port O. When asserted \nHigh, this port resets the counter used to produce \nthe divided clock output.
CLR	Input	1	Counter reset for divided clock output. When asserted \nHigh, this port resets the counter used to produce \nthe divided clock output.
I	Input	1	Clock input port. This port is the clock source port \nfor BUFR. It can be driven by BUFIO output or local \ninterconnect.
O	Output	1	Clock output port. This port drives the clock tracks \nin the clock region of the BUFR and the two adjacent \nclock regions. This port drives FPGA fabric, and \nIOBs.

Design Entry Method

This design element can be used in schematics.

Available Attributes

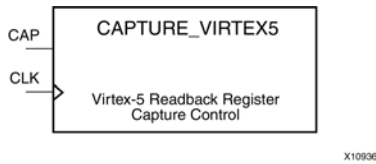
Attribute	Type	Allowed_Values	Default	Description
BUFR_DIVIDE	STRING	"BYPASS", "1", "2", "3", "4", "5", "6", "7", "8"	"BYPASS"	Defines whether the output clock is a divided version \nof input clock.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CAPTURE_VIRTEX5

Primitive: Virtex®-5 Readback Register Capture Control



Introduction

This element provides user control and synchronization over when and how the capture register (flip-flop and latch) information task is requested. The readback function is provided through dedicated configuration port instructions. However, without this element, the readback data is synchronized to the configuration clock. Only register (flip-flop and latch) states can be captured. Although LUT RAM, SRL, and block RAM states are readback, they cannot be captured.

An asserted high CAP signal indicates that the registers in the device are to be captured at the next Low-to-High clock transition. By default, data is captured after every trigger when transition on CLK while CAP is asserted. To limit the readback operation to a single data capture, add the ONESHOT=TRUE attribute to this element.

Port Descriptions

Port	Direction	Width	Function
CAP	Input	1	Readback capture trigger
CLK	Input	1	Readback capture clock

Design Entry Method

This design element can be used in schematics.

Connect all inputs and outputs to the design in order to ensure proper operation.

Available Attributes

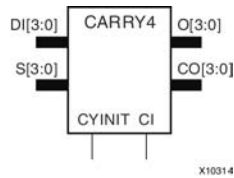
Attribute	Type	Allowed Values	Default	Description
ONESHOT	Boolean	TRUE, FALSE	TRUE	Specifies the procedure for performing single readback per CAP trigger.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CARRY4

Primitive: Fast Carry Logic with Look Ahead



Introduction

This circuit design represents the fast carry logic for a slice. The carry chain consists of a series of four MUXes and four XORs that connect to the other logic (LUTs) in the slice via dedicated routes to form more complex functions. The fast carry logic is useful for building arithmetic functions like adders, counters, subtractors and add/subs, as well as such other logic functions as wide comparators, address decoders, and some logic gates (specifically, AND and OR).

Port Descriptions

Port	Direction	Width	Function
O	Output	4	Carry chain XOR general data out
CO	Output	4	Carry-out of each stage of the carry chain
DI	Input	4	Carry-MUX data input
S	Input	4	Carry-MUX select line
CYINIT	Input	1	Carry-in initialization input
CI	Input	1	Carry cascade input

Design Entry Method

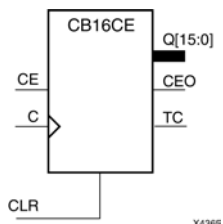
This design element can be used in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CB16CE

Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is an asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs		
CLR	CE	C	Qz-Q0	TC	CEO
1	X	X	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1 $TC = Q_z \cdot Q_{(z-1)} \cdot Q_{(z-2)} \cdot \dots \cdot Q_0$ $CEO = TC \cdot CE$					

Design Entry Method

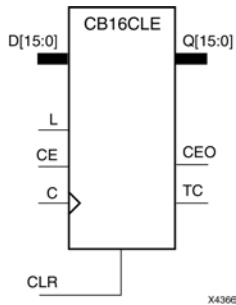
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CB16CLE

Macro: 16-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear



Introduction

This element is a synchronously loadable, asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs					Outputs		
CLR	L	CE	C	Dz-D0	Qz-Q0	TC	CEO
1	X	X	X	X	0	0	0
0	1	X	↑	Dn	Dn	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO
z = bit width - 1 $TC = Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \dots \cdot Q0$ $CEO = TC \cdot CE$							

Design Entry Method

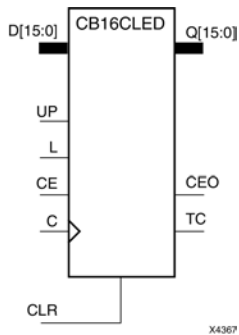
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CB16CLED

Macro: 16-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear



Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to-High clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

For CPLD parts, see “CB2X1”, “CB4X1”, “CB8X1”, “CB16X1” for high-performance cascadable, bidirectional counters.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs						Outputs		
CLR	L	CE	C	UP	Dz-D0	Qz-Q0	TC	CEO
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	Dn	TC	CEO
0	0	0	X	X	X	No change	No change	0
0	0	1	↑	1	X	Inc	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO
$z = \text{bit width} - 1$ $TC = (Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \dots \cdot Q0 \cdot UP) + (Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \dots \cdot Q0 \cdot \overline{UP})$								

Inputs						Outputs		
CLR	L	CE	C	UP	Dz-D0	Qz-Q0	TC	CEO
CEO = TC • CE								

Design Entry Method

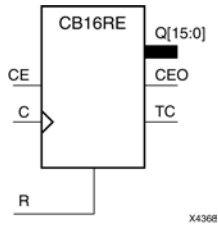
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CB16RE

Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset



Introduction

This design element is a synchronous, resettable, cascadable binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to zero on the Low-to-High clock transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when both Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n \cdot (t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs		
R	CE	C	Qz-Q0	TC	CEO
1	X	↑	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
$z = \text{bit width} - 1$ $TC = Q_z \cdot Q_{(z-1)} \cdot Q_{(z-2)} \cdot \dots \cdot Q_0$ $CEO = TC \cdot CE$					

Design Entry Method

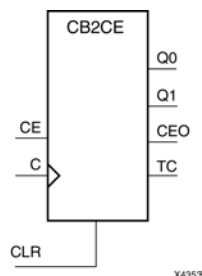
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CB2CE

Macro: 2-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is an asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs		
CLR	CE	C	Qz-Q0	TC	CEO
1	X	X	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
$z = \text{bit width} - 1$ $TC = Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \dots \cdot Q0$ $CEO = TC \cdot CE$					

Design Entry Method

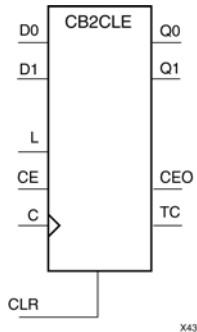
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CB2CLE

Macro: 2-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear



Introduction

This element is a synchronously loadable, asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs					Outputs		
CLR	L	CE	C	Dz-D0	Qz-Q0	TC	CEO
1	X	X	X	X	0	0	0
0	1	X	↑	Dn	Dn	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO
z = bit width - 1 $TC = Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \dots \cdot Q0$ $CEO = TC \cdot CE$							

Design Entry Method

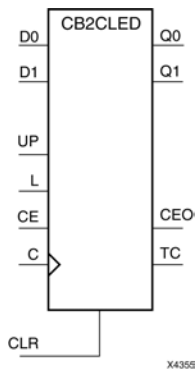
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CB2CLED

Macro: 2-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear



Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to-High clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

For CPLD parts, see “CB2X1”, “CB4X1”, “CB8X1”, “CB16X1” for high-performance cascadable, bidirectional counters.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs						Outputs		
CLR	L	CE	C	UP	Dz-D0	Qz-Q0	TC	CEO
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	Dn	TC	CEO
0	0	0	X	X	X	No change	No change	0
0	0	1	↑	1	X	Inc	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO

Inputs						Outputs		
CLR	L	CE	C	UP	Dz-D0	Qz-Q0	TC	CEO
$z = \text{bit width} - 1$ $TC = (Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \dots \cdot Q0 \cdot UP) + (Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \dots \cdot Q0 \cdot UP)$ $CEO = TC \cdot CE$								

Design Entry Method

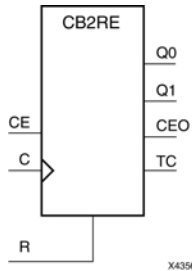
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CB2RE

Macro: 2-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset



Introduction

This design element is a synchronous, resettable, cascadable binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to zero on the Low-to-High clock transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when both Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs		
R	CE	C	Qz-Q0	TC	CEO
1	X	↑	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
$z = \text{bit width} - 1$ $TC = Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \dots \cdot Q0$ $CEO = TC \cdot CE$					

Design Entry Method

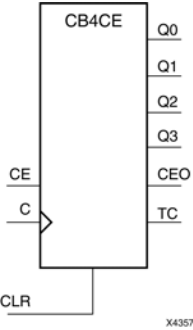
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CB4CE

Macro: 4-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is an asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs		
CLR	CE	C	Qz-Q0	TC	CEO
1	X	X	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1					
$TC = Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \dots \cdot Q0$					
$CEO = TC \cdot CE$					

Design Entry Method

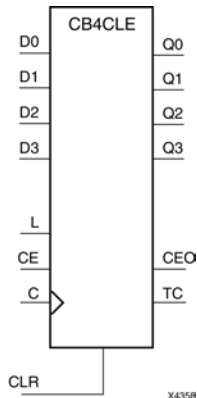
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CB4CLE

Macro: 4-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear



Introduction

This element is a synchronously loadable, asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs					Outputs		
CLR	L	CE	C	Dz-D0	Qz-Q0	TC	CEO
1	X	X	X	X	0	0	0
0	1	X	↑	Dn	Dn	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO
z = bit width - 1 $TC = Q_z \cdot Q_{(z-1)} \cdot Q_{(z-2)} \cdot \dots \cdot Q_0$ $CEO = TC \cdot CE$							

Design Entry Method

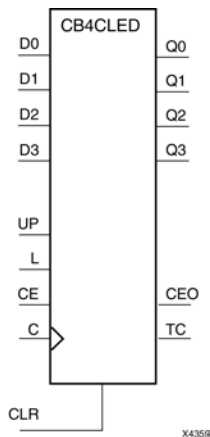
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CB4CLED

Macro: 4-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear



Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to-High clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

For CPLD parts, see “CB2X1”, “CB4X1”, “CB8X1”, “CB16X1” for high-performance cascadable, bidirectional counters.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs						Outputs		
CLR	L	CE	C	UP	Dz-D0	Qz-Q0	TC	CEO
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	Dn	TC	CEO
0	0	0	X	X	X	No change	No change	0
0	0	1	↑	1	X	Inc	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO
z = bit width - 1 $TC = (Qz \bullet Q(z-1) \bullet Q(z-2) \bullet \dots \bullet Q0 \bullet UP) + (Qz \bullet Q(z-1) \bullet Q(z-2) \bullet \dots \bullet Q0 \bullet UP)$ $CEO = TC \bullet CE$								

Design Entry Method

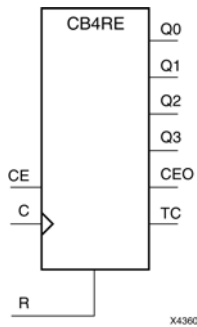
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CB4RE

Macro: 4-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset



Introduction

This design element is a synchronous, resettable, cascadable binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to zero on the Low-to-High clock transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when both Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs		
R	CE	C	Qz-Q0	TC	CEO
1	X	↑	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
$z = \text{bit width} - 1$ $TC = Q_z \cdot Q(z-1) \cdot Q(z-2) \cdot \dots \cdot Q_0$ $CEO = TC \cdot CE$					

Design Entry Method

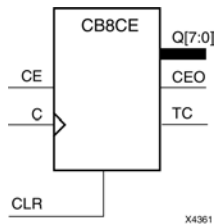
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CB8CE

Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is an asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs		
CLR	CE	C	Qz-Q0	TC	CEO
1	X	X	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1 $TC = Q_z \cdot Q_{(z-1)} \cdot Q_{(z-2)} \cdot \dots \cdot Q_0$ $CEO = TC \cdot CE$					

Design Entry Method

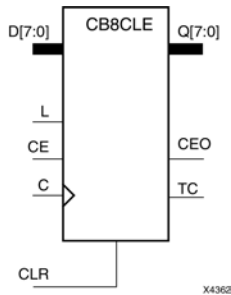
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CB8CLE

Macro: 8-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear



Introduction

This element is a synchronously loadable, asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs					Outputs		
CLR	L	CE	C	Dz-D0	Qz-Q0	TC	CEO
1	X	X	X	X	0	0	0
0	1	X	↑	Dn	Dn	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO
z = bit width - 1 $TC = Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \dots \cdot Q0$ $CEO = TC \cdot CE$							

Design Entry Method

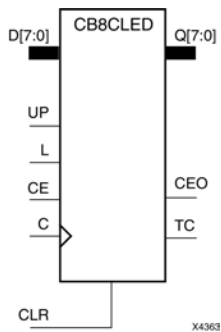
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CB8CLED

Macro: 8-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear



Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to-High clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

For CPLD parts, see “CB2X1”, “CB4X1”, “CB8X1”, “CB16X1” for high-performance cascadable, bidirectional counters.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs						Outputs		
CLR	L	CE	C	UP	Dz-D0	Qz-Q0	TC	CEO
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	Dn	TC	CEO
0	0	0	X	X	X	No change	No change	0
0	0	1	↑	1	X	Inc	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO

z = bit width - 1

$$TC = (Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \dots \cdot Q0 \cdot UP) + (Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \dots \cdot Q0 \cdot \overline{UP})$$

Inputs						Outputs		
CLR	L	CE	C	UP	Dz-D0	Qz-Q0	TC	CEO
CEO = TC • CE								

Design Entry Method

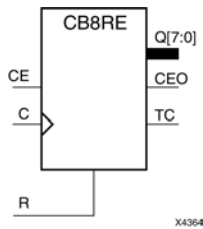
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CB8RE

Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset



Introduction

This design element is a synchronous, resettable, cascadable binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to zero on the Low-to-High clock transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when both Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs		
R	CE	C	Qz-Q0	TC	CEO
1	X	↑	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1 $TC = Q_z \cdot Q_{(z-1)} \cdot Q_{(z-2)} \cdot \dots \cdot Q_0$ $CEO = TC \cdot CE$					

Design Entry Method

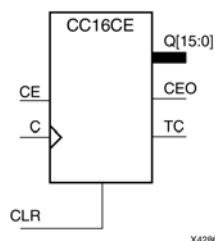
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CC16CE

Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is an asynchronously clearable, cascadable binary counter. It is implemented using carry logic with relative location constraints to ensure efficient logic placement. The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs		
CLR	CE	C	Qz-Q0	TC	CEO
1	X	X	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1 $TC = Q_z \cdot Q_{(z-1)} \cdot Q_{(z-2)} \cdot \dots \cdot Q_0$ $CEO = TC \cdot CE$					

Design Entry Method

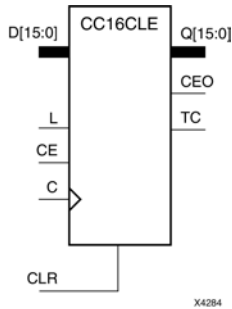
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CC16CLE

Macro: 16-Bit Loadable Cascadable Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable binary counter. It is implemented using carry logic with relative location constraints to ensure efficient logic placement. The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs					Outputs		
CLR	L	CE	C	Dz-D0	Qz-Q0	TC	CEO
1	X	X	X	X	0	0	0
0	1	X	↑	Dn	Dn	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO
z = bit width - 1 $TC = Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \dots \cdot Q0$ $CEO = TC \cdot CE$							

Design Entry Method

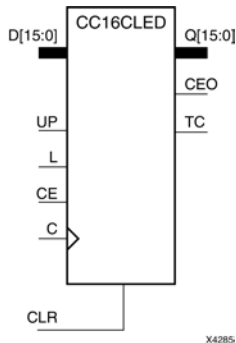
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CC16CLED

Macro: 16-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional binary counter. It is implemented using carry logic with relative location constraints, which assures most efficient logic placement. The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to-High clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs						Outputs		
CLR	L	CE	C	UP	Dz-D0	Qz-Q0	TC	CEO
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	Dn	TC	CEO
0	0	0	X	X	X	No change	No change	0
0	0	1	↑	1	X	Inc	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO
z = bit width - 1 $TC = (Q_z \cdot Q_{(z-1)} \cdot Q_{(z-2)} \cdot \dots \cdot Q_0 \cdot UP) + (Q_z \cdot Q_{(z-1)} \cdot Q_{(z-2)} \cdot \dots \cdot Q_0 \cdot \overline{UP})$ $CEO = TC \cdot CE$								

Design Entry Method

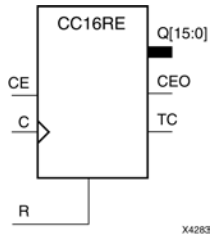
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CC16RE

Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset



Introduction

This design element is a synchronous resettable, cascadable binary counter. These counters are implemented using carry logic with relative location constraints to ensure efficient logic placement. The synchronous reset (R) is the highest priority input. When R is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero on the Low-to-High clock (C) transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs and CE are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n (t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs			Outputs		
R	CE	C	Qz-Q0	TC	CEO
1	X	↑	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1 $TC = Q_z \cdot Q(z-1) \cdot Q(z-2) \cdot \dots \cdot Q_0$ $CEO = TC \cdot CE$					

Design Entry Method

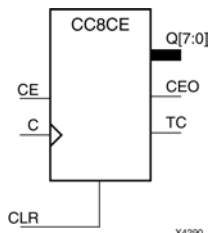
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CC8CE

Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is an asynchronously clearable, cascadable binary counter. It is implemented using carry logic with relative location constraints to ensure efficient logic placement. The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs			Outputs		
CLR	CE	C	Q _z -Q ₀	TC	CEO
1	X	X	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO

$z = \text{bit width} - 1$
 $TC = Q_z \cdot Q(z-1) \cdot Q(z-2) \cdot \dots \cdot Q_0$
 $CEO = TC \cdot CE$

Design Entry Method

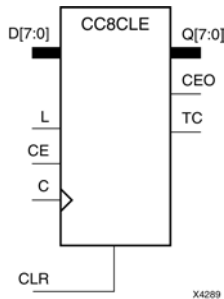
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CC8CLE

Macro: 8-Bit Loadable Cascadable Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable binary counter. It is implemented using carry logic with relative location constraints to ensure efficient logic placement. The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs					Outputs		
CLR	L	CE	C	Dz-D0	Qz-Q0	TC	CEO
1	X	X	X	X	0	0	0
0	1	X	↑	Dn	Dn	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO
z = bit width - 1 $TC = Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \dots \cdot Q0$ $CEO = TC \cdot CE$							

Design Entry Method

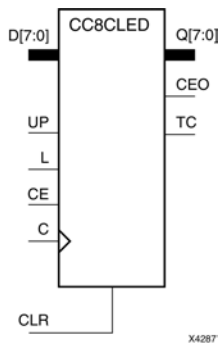
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CC8CLED

Macro: 8-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional binary counter. It is implemented using carry logic with relative location constraints, which assures most efficient logic placement. The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to-High clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs						Outputs		
CLR	L	CE	C	UP	Dz-D0	Qz-Q0	TC	CEO
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	Dn	TC	CEO
0	0	0	X	X	X	No change	No change	0
0	0	1	↑	1	X	Inc	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO
z = bit width - 1 $TC = (Q_z \cdot Q_{(z-1)} \cdot Q_{(z-2)} \cdot \dots \cdot Q_0 \cdot UP) + (Q_z \cdot Q_{(z-1)} \cdot Q_{(z-2)} \cdot \dots \cdot Q_0 \cdot \overline{UP})$ $CEO = TC \cdot CE$								

Design Entry Method

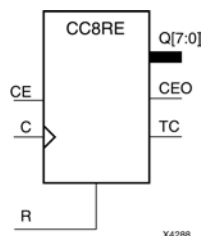
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CC8RE

Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset



Introduction

This design element is a synchronous resettable, cascadable binary counter. These counters are implemented using carry logic with relative location constraints to ensure efficient logic placement. The synchronous reset (R) is the highest priority input. When R is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero on the Low-to-High clock (C) transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs and CE are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n (t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs			Outputs		
R	CE	C	Q _z -Q ₀	TC	CEO
1	X	↑	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
$z = \text{bit width} - 1$ $TC = Q_z \cdot Q(z-1) \cdot Q(z-2) \cdot \dots \cdot Q_0$ $CEO = TC \cdot CE$					

Design Entry Method

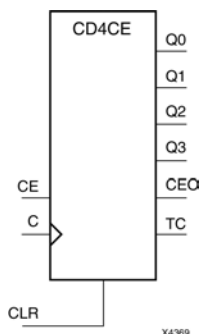
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CD4CE

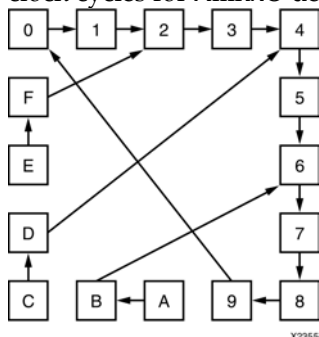
Macro: 4-Bit Cascadable BCD Counter with Clock Enable and Asynchronous Clear



Introduction

CD4CE is a 4-bit (stage), asynchronous clearable, cascadable binary-coded-decimal (BCD) counter. The asynchronous clear input (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The Q outputs increment when clock enable (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when Q3 and Q0 are High and Q2 and Q1 are Low.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for Xilinx® devices, as shown in the following state diagram:



Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs			Outputs					
CLR	CE	C	Q3	Q2	Q1	Q0	TC	CEO
1	X	X	0	0	0	0	0	0
0	1	↑	Inc	Inc	Inc	Inc	TC	CEO
0	0	X	No Change	No Change	No Change	No Change	TC	0
0	1	X	1	0	0	1	1	1
$TC = Q3 \cdot !Q2 \cdot !Q1 \cdot Q0$ $CEO = TC \cdot CE$								

Design Entry Method

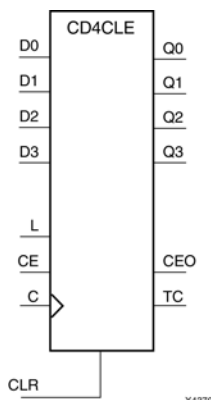
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CD4CLE

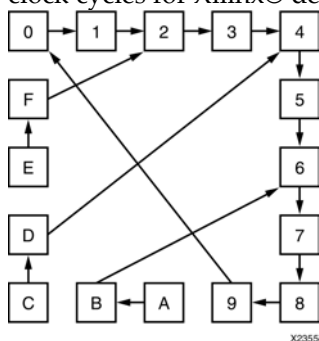
Macro: 4-Bit Loadable Cascadable BCD Counter with Clock Enable and Asynchronous Clear



Introduction

CD4CLE is a 4-bit (stage), synchronously loadable, asynchronously clearable, binary-coded-decimal (BCD) counter. The asynchronous clear input (CLR) is the highest priority input. When (CLR) is High, all other inputs are ignored; the (Q) outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the (D) inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition. The (Q) outputs increment when clock enable input (CE) is High during the Low-to-High clock transition. The counter ignores clock transitions when (CE) is Low. The (TC) output is High when Q3 and Q0 are High and Q2 and Q1 are Low.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for Xilinx® devices, as shown in the following state diagram:



Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs					Outputs					
CLR	L	CE	D3 : D0	C	Q3	Q2	Q1	Q0	TC	CEO
1	X	X	X	X	0	0	0	0	0	0
0	1	X	D3 : D0	↑	D3	D2	D1	D0	TC	CEO
0	0	1	X	↑	Inc	Inc	Inc	Inc	TC	CEO
0	0	0	X	X	No Change	No Change	No Change	No Change	TC	0
0	0	1	X	X	1	0	0	1	1	1
TC = $Q3 \cdot !Q2 \cdot !Q1 \cdot Q0$ CEO = $TC \cdot CE$										

Design Entry Method

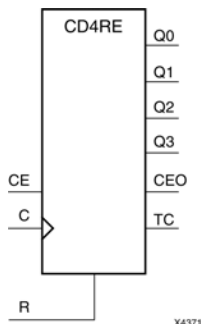
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CD4RE

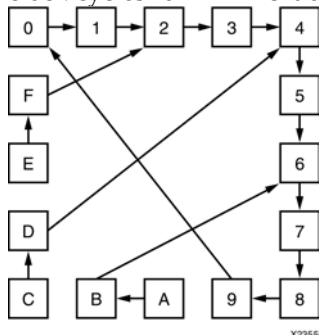
Macro: 4-Bit Cascadable BCD Counter with Clock Enable and Synchronous Reset



Introduction

CD4RE is a 4-bit (stage), synchronous resettable, cascadable binary-coded-decimal (BCD) counter. The synchronous reset input (R) is the highest priority input. When (R) is High, all other inputs are ignored; the (Q) outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero on the Low-to-High clock (C) transition. The (Q) outputs increment when the clock enable input (CE) is High during the Low-to-High clock transition. The counter ignores clock transitions when (CE) is Low. The (TC) output is High when Q3 and Q0 are High and Q2 and Q1 are Low.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for Xilinx® devices, as shown in the following state diagram:



Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs			Outputs					
R	CE	C	Q3	Q2	Q1	Q0	TC	CEO
1	X	↑	0	0	0	0	0	0
0	1	↑	Inc	Inc	Inc	Inc	TC	CEO
0	0	X	No Change	No Change	No Change	No Change	TC	0
0	1	X	1	0	0	1	1	1
TC = $Q3 \cdot !Q2 \cdot !Q1 \cdot Q0$								
CEO = $TC \cdot CE$								

Design Entry Method

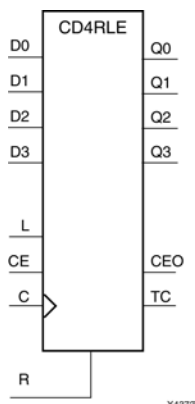
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CD4RLE

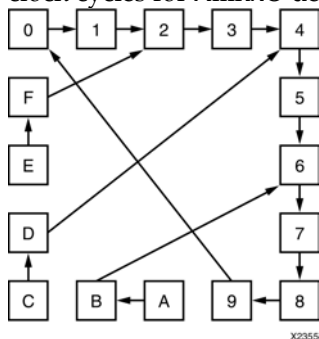
Macro: 4-Bit Loadable Cascadable BCD Counter with Clock Enable and Synchronous Reset



Introduction

CD4RLE is a 4-bit (stage), synchronous loadable, resettable, binary-coded-decimal (BCD) counter. The synchronous reset input (R) is the highest priority input. When R is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero on the Low-to-High clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when Q3 and Q0 are High and Q2 and Q1 are Low.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for Xilinx® devices, as shown in the following state diagram:



Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs					Outputs					
R	L	CE	D3 : D0	C	Q3	Q2	Q1	Q0	TC	CEO
1	X	X	X	↑	0	0	0	0	0	0
0	1	X	D3 : D0	↑	D3	D	D	D0	TC	CEO
0	0	1	X	↑	Inc	Inc	Inc	Inc	TC	CEO
0	0	0	X	X	No Change	No Change	No Change	No Change	TC	0
0	0	1	X	X	1	0	0	1	1	1
TC = Q3•!Q2•!Q1•Q0										
CEO = TC•CE										

Design Entry Method

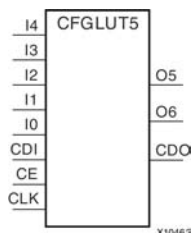
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CFGLUT5

Primitive: 5-input Dynamically Reconfigurable Look-Up Table (LUT)



Introduction

This element is a runtime, dynamically reconfigurable, 5-input look-up table (LUT) that enables the changing of the logical function of the LUT during circuit operation. Using the CDI pin, a new INIT value can be synchronously shifted in serially to change the logical function. The O6 output pin produces the logical output function, based on the current INIT value loaded into the LUT and the currently selected I0-I4 input pins. Optionally, you can use the O5 output in combination with the O6 output to create two individual 4-input functions sharing the same inputs or a 5-input function and a 4-input function that uses a subset of the 5-input logic (see tables below). This component occupies one of the four 6-LUT components within a slice.

To cascade this element, connect the CDO pin from each element to the CDI input of the next element. This will allow a single serial chain of data (32-bits per LUT) to reconfigure multiple LUTs.

Port Descriptions

Port	Direction	Width	Function
O6	Output	1	5-LUT output
O5	Output	1	4-LUT output
I0, I1, I2, I3, I4	Input	1	LUT inputs
CDO	Output	1	Reconfiguration data cascaded output (optionally connect to the CDI input of a subsequent LUT)
CDI	Input	1	Reconfiguration data serial input
CLK	Input	1	Reconfiguration clock
CE	Input	1	Active high reconfiguration clock enable

Design Entry Method

This design element can be used in schematics.

- Connect the CLK input to the clock source used to supply the reconfiguration data.
- Connect the CDI input to the source of the reconfiguration data.
- Connect the CE pin to the active high logic if you need to enable/disable LUT reconfiguration.
- Connect the I4-I0 pins to the source inputs to the logic equation. The logic function is output on O6 and O5.
- To cascade this element, connect the CDO pin from each element to the CDI input of the next element to allow a single serial chain of data to reconfigure multiple LUTs.

The INIT attribute should be placed on this design element to specify the initial logical function of the LUT. A new INIT can be loaded into the LUT any time during circuit operation by shifting in 32-bits per LUT in the chain, representing the new INIT value. Disregard the O6 and O5 output data until all 32-bits of new INIT data has been clocked into the LUT. The logical function of the LUT changes as new INIT data is shifted into it. Data should be shifted in MSB (INIT[31]) first and LSB (INIT[0]) last.

In order to understand the O6 and O5 logical value based on the current INIT, see the table below:

I4 I3 I2 I1 I0	O6 Value	O5 Value
1 1 1 1 1	INIT[31]	INIT[15]
1 1 1 1 0	INIT[30]	INIT[14]
...
1 0 0 0 1	INIT[17]	INIT[1]
1 0 0 0 0	INIT[16]	INIT[0]
0 1 1 1 1	INIT[15]	INIT[15]
0 1 1 1 0	INIT[14]	INIT[14]
...
0 0 0 0 1	INIT[1]	INIT[1]
0 0 0 0 0	INIT[0]	INIT[0]

For instance, the INIT value of FFFF8000 would represent the following logical equations:

- $O6 = I4 \text{ or } (I3 \text{ and } I2 \text{ and } I1 \text{ and } I0)$
- $O5 = I3 \text{ and } I2 \text{ and } I1 \text{ and } I0$

To use these elements as two, 4-input LUTs with the same inputs but different functions, tie the I4 signal to a logical one. The INIT[31:16] values apply to the logical values of the O6 output and INIT [15:0] apply to the logical values of the O5 output.

Available Attributes

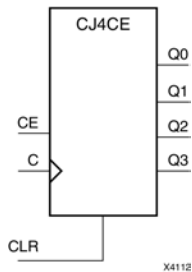
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 32-bit Value	All zeros	Specifies the initial logical expression of this element.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CJ4CE

4-Bit Johnson Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is a clearable Johnson/shift counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the data (Q) outputs to logic level zero, independent of clock (C) transitions. The counter increments (shifts Q0 to Q1, Q1 to Q2, and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when (CE) is Low.

The Q3 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs	
CLR	CE	C	Q0	Q1 through Q3
1	X	X	0	0
0	0	X	No change	No change
0	1	↑	!q3	q0 through q2
q = state of referenced output one setup time prior to active clock transition				

Design Entry Method

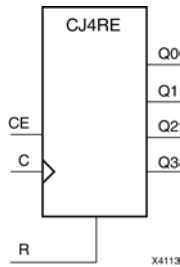
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CJ4RE

Macro: 4-Bit Johnson Counter with Clock Enable and Synchronous Reset



Introduction

This design element is a resettable Johnson/shift counter. The synchronous reset (R) input, when High, overrides all other inputs and forces the data (Q) outputs to logic level zero during the Low-to-High clock (C) transition. The counter increments (shifts Q0 to Q1, Q1 to Q2, and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when CE is Low.

The Q3 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs	
R	CE	C	Q0	Q1 through Q3
1	X	↑	0	0
0	0	X	No change	No change
0	1	↑	!q3	q0 through q2
q = state of referenced output one setup time prior to active clock transition				

Design Entry Method

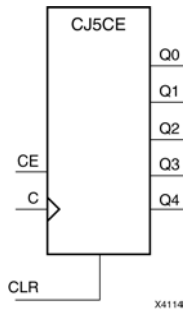
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CJ5CE

Macro: 5-Bit Johnson Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is a clearable Johnson/shift counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the data (Q) outputs to logic level zero, independent of clock (C) transitions. The counter increments (shifts Q0 to Q1, Q1 to Q2, and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when (CE) is Low.

The Q4 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs	
CLR	CE	C	Q0	Q1 through Q4
1	X	X	0	0
0	0	X	No change	No change
0	1	↑	!q4	q0 through q3
q = state of referenced output one setup time prior to active clock transition				

Design Entry Method

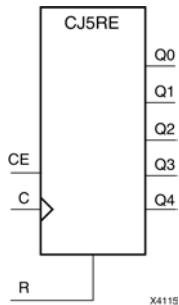
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CJ5RE

Macro: 5-Bit Johnson Counter with Clock Enable and Synchronous Reset



Introduction

This design element is a resettable Johnson/shift counter. The synchronous reset (R) input, when High, overrides all other inputs and forces the data (Q) outputs to logic level zero during the Low-to-High clock (C) transition. The counter increments (shifts Q0 to Q1, Q1 to Q2, and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when CE is Low.

The Q4 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs	
R	CE	C	Q0	Q1 through Q4
1	X	↑	0	0
0	0	X	No change	No change
0	1	↑	!q4	q0 through q3
q = state of referenced output one setup time prior to active clock transition				

Design Entry Method

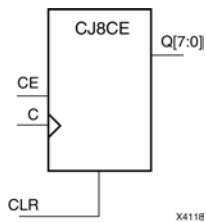
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CJ8CE

Macro: 8-Bit Johnson Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is a clearable Johnson/shift counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the data (Q) outputs to logic level zero, independent of clock (C) transitions. The counter increments (shifts Q0 to Q1, Q1 to Q2, and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when (CE) is Low.

The Q7 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs	
CLR	CE	C	Q0	Q1 through Q8
1	X	X	0	0
0	0	X	No change	No change
0	1	↑	!q7	q0 through q7

q = state of referenced output one setup time prior to active clock transition

Design Entry Method

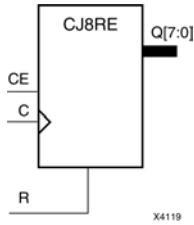
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CJ8RE

Macro: 8-Bit Johnson Counter with Clock Enable and Synchronous Reset



Introduction

This design element is a resettable Johnson/shift counter. The synchronous reset (R) input, when High, overrides all other inputs and forces the data (Q) outputs to logic level zero during the Low-to-High clock (C) transition. The counter increments (shifts Q0 to Q1, Q1 to Q2, and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when CE is Low.

The Q7 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs	
R	CE	C	Q0	Q1 through Q7
1	X	↑	0	0
0	0	X	No change	No change
0	1	↑	!q7	q0 through q6
q = state of referenced output one setup time prior to active clock transition				

Design Entry Method

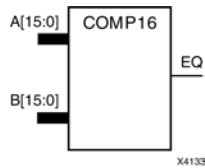
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

COMP16

Macro: 16-Bit Identity Comparator



Introduction

This design element is a 16-bit identity comparator. The equal output (EQ) is high when A15 : A0 and B15 : B0 are equal.

Equality is determined by a bit comparison of the two words. When any two of the corresponding bits from each word are not the same, the EQ output is Low.

Design Entry Method

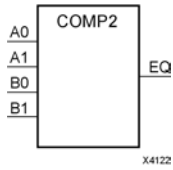
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

COMP2

Macro: 2-Bit Identity Comparator



Introduction

This design element is a 2-bit identity comparator. The equal output (EQ) is High when the two words A1 : A0 and B1 : B0 are equal.

Equality is determined by a bit comparison of the two words. When any two of the corresponding bits from each word are not the same, the EQ output is Low.

Design Entry Method

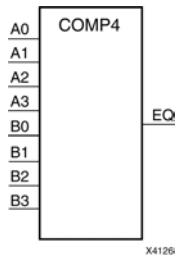
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

COMP4

Macro: 4-Bit Identity Comparator



Introduction

This design element is a 4-bit identity comparator. The equal output (EQ) is high when A3 : A0 and B3 : B0 are equal.

Equality is determined by a bit comparison of the two words. When any two of the corresponding bits from each word are not the same, the EQ output is Low.

Design Entry Method

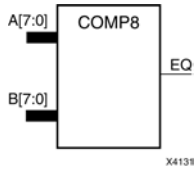
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

COMP8

Macro: 8-Bit Identity Comparator



Introduction

This design element is an 8-bit identity comparator. The equal output (EQ) is high when A7 : A0 and B7 : B0 are equal.

Equality is determined by a bit comparison of the two words. When any two of the corresponding bits from each word are not the same, the EQ output is Low.

Design Entry Method

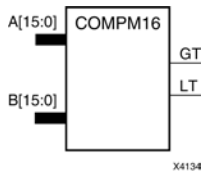
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

COMPM16

Macro: 16-Bit Magnitude Comparator



Introduction

This design element is a 16-bit magnitude comparator that compare two positive Binary-weighted words. It compares A15 : A0 and B15 : B0, where A15 and B15 are the most significant bits.

The greater-than output (GT) is High when $A > B$, and the less-than output (LT) is High when $A < B$. When the two words are equal, both GT and LT are Low. Equality can be measured with this macro by comparing both outputs with a NOR gate.

Logic Table

Inputs								Outputs	
A7, B7	A6, B6	A5, B5	A4, B4	A3, B3	A2, B2	A1, B1	A0, B0	GT	LT
A7>B7	X	X	X	X	X	X	X	1	0
A7<B7	X	X	X	X	X	X	X	0	1
A7=B7	A6>B6	X	X	X	X	X	X	1	0
A7=B7	A6<B6	X	X	X	X	X	X	0	1
A7=B7	A6=B6	A5>B5	X	X	X	X	X	1	0
A7=B7	A6=B6	A5<B5	X	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4>B4	X	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4<B4	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3>B3	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3<B3	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2>B2	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2<B2	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1>B1	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1<B1	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0>B0	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0<B0	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0=B0	0	0

Design Entry Method

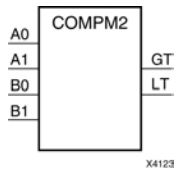
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

COMPM2

Macro: 2-Bit Magnitude Comparator



Introduction

This design element is a 2-bit magnitude comparator that compare two positive binary-weighted words. It compares A1 : A0 and B1 : B0, where A1 and B1 are the most significant bits.

The greater-than output (GT) is High when $A > B$, and the less-than output (LT) is High when $A < B$. When the two words are equal, both GT and LT are Low. Equality can be measured with this macro by comparing both outputs with a NOR gate.

Logic Table

Inputs				Outputs	
A1	B1	A0	B0	GT	LT
0	0	0	0	0	0
0	0	1	0	1	0
0	0	0	1	0	1
0	0	1	1	0	0
1	1	0	0	0	0
1	1	1	0	1	0
1	1	0	1	0	1
1	1	1	1	0	0
1	0	X	X	1	0
0	1	X	X	0	1

Design Entry Method

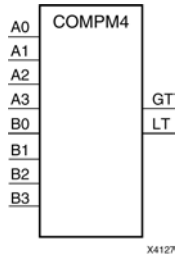
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

COMPM4

Macro: 4-Bit Magnitude Comparator



Introduction

This design element is a 4-bit magnitude comparator that compare two positive Binary-weighted words. It compares A3 : A0 and B3 : B0, where A3 and B3 are the most significant bits.

The greater-than output (GT) is High when $A > B$, and the less-than output (LT) is High when $A < B$. When the two words are equal, both GT and LT are Low. Equality can be measured with this macro by comparing both outputs with a NOR gate.

Logic Table

Inputs				Outputs	
A3, B3	A2, B2	A1, B1	A0, B0	GT	LT
$A3 > B3$	X	X	X	1	0
$A3 < B3$	X	X	X	0	1
$A3 = B3$	$A2 > B2$	X	X	1	0
$A3 = B3$	$A2 < B2$	X	X	0	1
$A3 = B3$	$A2 = B2$	$A1 > B1$	X	1	0
$A3 = B3$	$A2 = B2$	$A1 < B1$	X	0	1
$A3 = B3$	$A2 = A2$	$A1 = B1$	$A0 > B0$	1	0
$A3 = B3$	$A2 = B2$	$A1 = B1$	$A0 < B0$	0	1
$A3 = B3$	$A2 = B2$	$A1 = B1$	$A0 = B0$	0	0

Design Entry Method

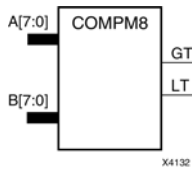
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

COMPM8

Macro: 8-Bit Magnitude Comparator



Introduction

This design element is an 8-bit magnitude comparator that compare two positive Binary-weighted words. It compares A7 : A0 and B7 : B0, where A7 and B7 are the most significant bits.

The greater-than output (GT) is High when $A > B$, and the less-than output (LT) is High when $A < B$. When the two words are equal, both GT and LT are Low. Equality can be measured with this macro by comparing both outputs with a NOR gate.

Logic Table

Inputs								Outputs	
A7, B7	A6, B6	A5, B5	A4, B4	A3, B3	A2, B2	A1, B1	A0, B0	GT	LT
$A7 > B7$	X	X	X	X	X	X	X	1	0
$A7 < B7$	X	X	X	X	X	X	X	0	1
$A7 = B7$	$A6 > B6$	X	X	X	X	X	X	1	0
$A7 = B7$	$A6 < B6$	X	X	X	X	X	X	0	1
$A7 = B7$	$A6 = B6$	$A5 > B5$	X	X	X	X	X	1	0
$A7 = B7$	$A6 = B6$	$A5 < B5$	X	X	X	X	X	0	1
$A7 = B7$	$A6 = B6$	$A5 = B5$	$A4 > B4$	X	X	X	X	1	0
$A7 = B7$	$A6 = B6$	$A5 = B5$	$A4 < B4$	X	X	X	X	0	1
$A7 = B7$	$A6 = B6$	$A5 = B5$	$A4 = B4$	$A3 > B3$	X	X	X	1	0
$A7 = B7$	$A6 = B6$	$A5 = B5$	$A4 = B4$	$A3 < B3$	X	X	X	0	1
$A7 = B7$	$A6 = B6$	$A5 = B5$	$A4 = B4$	$A3 = B3$	$A2 > B2$	X	X	1	0
$A7 = B7$	$A6 = B6$	$A5 = B5$	$A4 = B4$	$A3 = B3$	$A2 < B2$	X	X	0	1
$A7 = B7$	$A6 = B6$	$A5 = B5$	$A4 = B4$	$A3 = B3$	$A2 = B2$	$A1 > B1$	X	1	0
$A7 = B7$	$A6 = B6$	$A5 = B5$	$A4 = B4$	$A3 = B3$	$A2 = B2$	$A1 < B1$	X	0	1
$A7 = B7$	$A6 = B6$	$A5 = B5$	$A4 = B4$	$A3 = B3$	$A2 = B2$	$A1 = B1$	$A0 > B0$	1	0
$A7 = B7$	$A6 = B6$	$A5 = B5$	$A4 = B4$	$A3 = B3$	$A2 = B2$	$A1 = B1$	$A0 < B0$	0	1
$A7 = B7$	$A6 = B6$	$A5 = B5$	$A4 = B4$	$A3 = B3$	$A2 = B2$	$A1 = B1$	$A0 = B0$	0	0

Design Entry Method

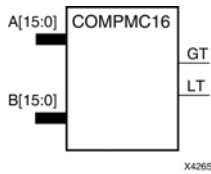
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

COMPMC16

Macro: 16-Bit Magnitude Comparator



Introduction

This design element is a 16-bit, magnitude comparator that compares two positive Binary weighted words A15 : A0 and B15 : B0, where A15 and B15 are the most significant bits.

This comparator is implemented using carry logic with relative location constraints to ensure efficient logic placement.

The greater-than output (GT) is High when $A > B$, and the less-than output (LT) is High when $A < B$. When the two words are equal, both GT and LT are Low. Equality can be flagged with this macro by connecting both outputs to a NOR gate.

Logic Table

Inputs								Outputs	
A7, B7	A6, B6	A5, B5	A4, B4	A3, B3	A2, B2	A1, B1	A0, B0	GT	LT
A7>B7	X	X	X	X	X	X	X	1	0
A7<B7	X	X	X	X	X	X	X	0	1
A7=B7	A6>B6	X	X	X	X	X	X	1	0
A7=B7	A6<B6	X	X	X	X	X	X	0	1
A7=B7	A6=B6	A5>B5	X	X	X	X	X	1	0
A7=B7	A6=B6	A5<B5	X	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4>B4	X	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4<B4	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3>B3	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3<B3	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2>B2	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2<B2	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1>B1	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1<B1	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0>B0	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0<B0	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0=B0	0	0

Design Entry Method

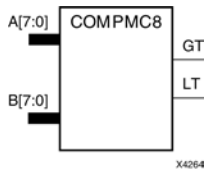
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

COMPMC8

Macro: 8-Bit Magnitude Comparator



Introduction

This design element is an 8-bit, magnitude comparator that compares two positive Binaryweighted words A7 : A0 and B7 : B0, where A7 and B7 are the most significant bits.

This comparator is implemented using carry logic with relative location constraints to ensure efficient logic placement.

The greater-than output (GT) is High when $A > B$, and the less-than output (LT) is High when $A < B$. When the two words are equal, both GT and LT are Low. Equality can be flagged with this macro by connecting both outputs to a NOR gate.

Logic Table

Inputs								Outputs	
A7, B7	A6, B6	A5, B5	A4, B4	A3, B3	A2, B2	A1, B1	A0, B0	GT	LT
A7>B7	X	X	X	X	X	X	X	1	0
A7<B7	X	X	X	X	X	X	X	0	1
A7=B7	A6>B6	X	X	X	X	X	X	1	0
A7=B7	A6<B6	X	X	X	X	X	X	0	1
A7=B7	A6=B6	A5>B5	X	X	X	X	X	1	0
A7=B7	A6=B6	A5<B5	X	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4>B4	X	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4<B4	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3>B3	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3<B3	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2>B2	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2<B2	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1>B1	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1<B1	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0>B0	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0<B0	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0=B0	0	0

Design Entry Method

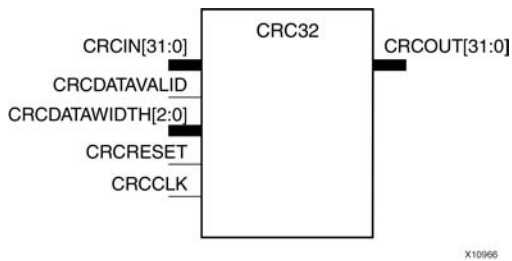
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CRC32

Primitive: Cyclic Redundancy Check Calculator for 32 bits



Introduction

This design element is computed for the contents of a frame and appended to the end of the frame before transmission or storage. Each CRC block computes a 32-bit CRC using the CRC-32 polynomial specified for PCI EXPRESS®, Gigabit Ethernet, and other common protocols. The 32-bit CRC primitive, CRC32, can process 8, 16, 24 or 32-bit input data and generates a 32-bit CRC.

Port Descriptions

Port	Direction	Width	Function		
CRCIN[31:0]	Input	32	CRC input data, max datapath width is 4 bytes		
CRCDATAVALID	Input	1	Indicates valid data on CRCIN inputs.		
			1'b1: data valid		
			1'b0: data invalid		
			De-asserting this signal will cause the CRC value to be held for the number of cycles that the signal is de-asserted		
CRCDATAWIDTH[2:0]	Input	3	Indicates how many input data bytes are valid.		
			CRCDATAWIDTH[2:0]	Data Width	CRC Data Bus bits
			0	8-bit	CRCIN[31:24]
			1	16-bit	CRCIN[31:16]
			10	24-bit	CRCIN[31:8]
			11	32-bit	CRCIN[31:0]
CRCRESET	Input	1	Synchronous reset of CRC registers. When CRCRESET is asserted, the CRC block is initialized to the CRC_INIT value		
CRCCLK	Input	1	CRC Clock		
CRCOUT[31:0]	Output	32	32-bit CRC output. CRCOUT is the byte-reversed, bit inverted CRC value corresponding to the CRC calculation on valid bytes from the previous clock cycle and the previous CRC value. Note that input CRCDATAVALID must be set to "1".		

Design Entry Method

This design element can be used in schematics.

Available Attributes

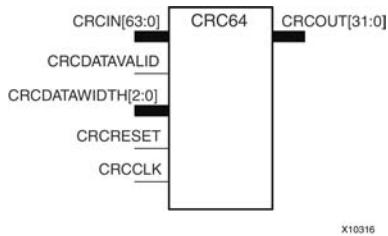
Attribute	Type	Allowed values	Default	Description
CRC_INIT[31:0]	Hexadecimal	Any 32-Bit Value	0xFFFFFFFF	Sets the initial value of CRC internal registers. For LX30T & LX50T ES silicon the value is fixed as 0xFFFFFFFF.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

CRC64

Primitive: Cyclic Redundancy Check Calculator for 64 bits



Introduction

This design element is computed for the contents of a frame, and appended to the end of the frame before transmission or storage. Each CRC block computes a 32-bit CRC using the CRC-32 polynomial specified for PCI EXPRESS®, Gigabit Ethernet, and other common protocols. The 64-bit CRC primitive, CRC64, can process 8, 16, 24, 32, 40, 56 or 64-bit input data and generates a 32-bit CRC. Using the CRC64 primitive consumes both CRC hard blocks paired with a given transceiver tile.

Port Descriptions

Port	Direction	Width	Function		
CRCIN[63:0]	Input	64	CRC input data, max datapath width is 8 bytes		
CRCDATAVALID	Input	1	Indicates valid data on CRCIN inputs.		
			1'b1: data valid		
			1'b0: data invalid		
			De-asserting this signal will cause the CRC value to be held for the number of cycles that the signal is de-asserted.		
CRCDATAWIDTH[2:0]	Input	3	Indicates how many input data bytes are valid.		
			CRCDATAWIDTH [2:0]	Data Width	CRC Data Bus bits
			0	8-bit	CRCIN[63:56]
			1	16-bit	CRCIN[63:48]
			10	24-bit	CRCIN[63:40]
			11	32-bit	CRCIN[63:32]
			100	40-bit	CRCIN[63:24]
			101	48-bit	CRCIN[63:16]
			110	56-bit	CRCIN[63:8]
			111	64-bit	CRCIN[63:0]
CRCRESET	Input	1	Synchronous reset of CRC registers. When CRCRESET is asserted, the CRC block is initialized to the CRC_INIT value.		
CRCCLK	Input	1	CRC Clock		
CRCOUT[31:0]	Output	32	32-bit CRC output. CRCOUT is the byte-reversed, bit inverted CRC value corresponding to the CRC calculation on valid bytes from the previous clock cycle and the previous CRC value. Note that CRCDATAVALID must be set to "1".		

Design Entry Method

This design element can be used in schematics.

Available Attributes

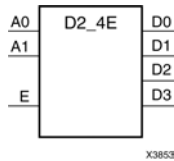
Attribute	Type	Allowed values	Default	Description
CRC_INIT[31:0]	Hexadecimal	Any 32-Bit Value	0xFFFFFFFF	Sets the initial value of CRC internal registers. For LX30T & LX50T ES silicon the value is fixed as 0xFFFFFFFF.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

D2_4E

Macro: 2- to 4-Line Decoder/Demultiplexer with Enable



Introduction

This design element is a decoder/demultiplexer. When the enable (E) input of this element is High, one of four active-High outputs (D3 : D0) is selected with a 2-bit binary address (A1 : A0) input. The non-selected outputs are Low. Also, when the E input is Low, all outputs are Low. In demultiplexer applications, the E input is the data input.

Logic Table

Inputs			Outputs			
A1	A0	E	D3	D2	D1	D0
X	X	0	0	0	0	0
0	0	1	0	0	0	1
0	1	1	0	0	1	0
1	0	1	0	1	0	0
1	1	1	1	0	0	0

Design Entry Method

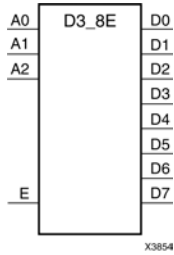
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

D3_8E

Macro: 3- to 8-Line Decoder/Demultiplexer with Enable



Introduction

When the enable (E) input of the D3_8E decoder/demultiplexer is High, one of eight active-High outputs (D7 : D0) is selected with a 3-bit binary address (A2 : A0) input. The non-selected outputs are Low. Also, when the E input is Low, all outputs are Low. In demultiplexer applications, the E input is the data input.

Logic Table

Inputs				Outputs							
A2	A1	A0	E	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	1
0	0	1	1	0	0	0	0	0	0	1	0
0	1	0	1	0	0	0	0	0	1	0	0
0	1	1	1	0	0	0	0	1	0	0	0
1	0	0	1	0	0	0	1	0	0	0	0
1	0	1	1	0	0	1	0	0	0	0	0
1	1	0	1	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0

Design Entry Method

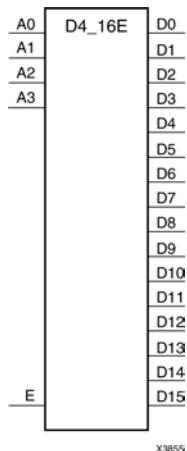
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

D4_16E

Macro: 4- to 16-Line Decoder/Demultiplexer with Enable



Introduction

This design element is a decoder/demultiplexer. When the enable (E) input of this design element is High, one of 16 active-High outputs (D15 : D0) is selected with a 4-bit binary address (A3 : A0) input. The non-selected outputs are Low. Also, when the E input is Low, all outputs are Low. In demultiplexer applications, the E input is the data input.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

DCIRESET

Primitive: DCI State Machine Reset (After Configuration Has Been Completed)



Introduction

This design element is used to reset the DCI state machine after configuration has been completed.

Port Descriptions

Port	Type	Width	Function
LOCKED	Output	1	Indicates that DCI state machine has achieved a stable state after reset.
RST	Input	1	Invokes the DCI state machine to start from initial state.

Design Entry Method

This design element can be used in schematics.

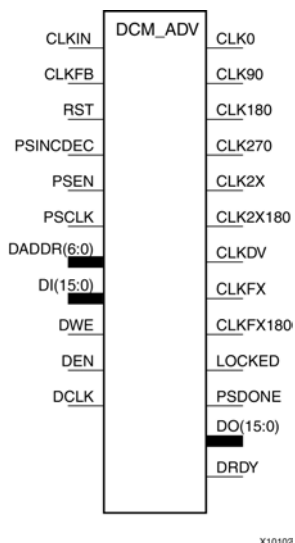
Available Attributes

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

DCM_ADV

Primitive: Advanced Digital Clock Manager Circuit



Introduction

This design element is a configurable/reconfigurable DLL with additional phase and frequency synthesis control capabilities. This component is commonly used for many FPGA applications in order to derive and control the various clocks needed within the system. If dynamic reconfiguration is not necessary, use either the DCM_BASE or DCM_PS components.

Port Descriptions

Port	Direction	Width	Function
Clock Outputs/Inputs			
CLK0	Output	1	The CLK0 output clock provides a clock with the same frequency as the DCM's effective CLKIN frequency. By default, the effective CLKIN frequency is equal to the CLKIN frequency, except when the CLKIN_DIVIDE_BY_2 attribute is set to TRUE. When CLKFB is connected, CLK0 is phase aligned to CLKIN.
CLK90	Output	1	The CLK90 output clock provides a clock with the same frequency as the DCM's CLK0, only phase-shifted by 90°.
CLK180	Output	1	The CLK180 output clock provides a clock with the same frequency as the DCM's CLK0, only phase-shifted by 180°.
CLK270	Output	1	The CLK270 output clock provides a clock with the same frequency as the DCM's CLK0, only phase-shifted by 270°.
CLK2X	Output	1	The CLK2X output clock provides a clock that is phase aligned to CLK0, with twice the CLK0 frequency, and with an automatic 50/50 duty-cycle correction. Until the DCM is locked, the CLK2X output appears as a 1x version of the input clock with a 25/75 duty cycle. This behavior allows the DCM to lock on the correct edge with respect to the source clock.
CLK2X180	Output	1	The CLK2X180 output clock provides a clock with the same frequency as the DCM's CLK2X, only phase-shifted by 180°.

Port	Direction	Width	Function
CLKDV	Output	1	The frequency divide (CLKDV) output clock provides a clock that is phase aligned to CLK0 with a frequency that is a fraction of the effective CLKIN frequency. The fraction is determined by the CLKDV_DIVIDE attribute. By default, the effective CLKIN frequency is equal to the CLKIN frequency, except when the CLKIN_DIVIDE_BY_2 attribute is set to TRUE.
CLKFX	Output	1	<p>The frequency (CLKFX) output clock provides a clock with the following frequency definition:</p> $\text{CLKFX Frequency} = (M/D) \times (\text{Effective CLKIN Frequency}).$ <p>In this equation, M is the multiplier (numerator), with a value defined by the CLKFX_MULTIPLY attribute. D is the divisor (denominator), with a value defined by the CLKFX_DIVIDE attribute. Specifications for M and D, as well as input and output frequency ranges for the frequency synthesizer, are provided in the Data Sheet for this architecture. The rising edge of CLKFX output is phase aligned to the rising edges of CLK0, CLK2X, and CLKDV when the feedback path (CLKFB) is used. When M and D do have no common factor, the alignment occurs only once every D cycles of CLK0. By default, the effective CLKIN frequency is equal to the CLKIN frequency, except when the CLKIN_DIVIDE_BY_2 attribute is set to TRUE.</p>
CLKFX180	Output	1	The CLKFX180 output clock provides a clock with the same frequency as the DCM's CLKFX only phase-shifted by 180°.
CLKIN	Input	1	<p>The source clock (CLKIN) input pin provides the source clock to the DCM. The CLKIN frequency must fall in the ranges specified in the Data Sheet for this architecture. The clock input signal comes from one of the following buffers:</p> <ul style="list-style-type: none"> IBUFG - Global Clock Input Buffer. The DCM compensates for the clock input path when an IBUFG, on the same edge (top or bottom) of the device, such as the DCM, is used. BUFG/BUFGCTRL - Internal Global Clock Buffer. Any BUFGCTRL can drive any DCM in the device using the dedicated global routing. A BUFGCTRL can drive the DCM CLKIN pin when used to connect two DCM in series. IBUF - Input Buffer. When IBUF drives CLKIN input, the PAD to DCM input skew is not compensated and increased jitter can occur. This configuration is generally not recommended.
CLKFB	Input	1	The feedback clock (CLKFB) input pin provides a reference or feedback signal to the DCM to delay-compensate the clock outputs and align it with the clock input. To provide the necessary feedback to the DCM, connect only the CLK0 output to the CLKFB input via a BUFG component in the case of internal feedback or an OBUF ' IBUFG to the case of external feedback. Set the CLK_FEEDBACK attribute to 1X. When the CLKFB pin is connected, CLK0, CLKDV, and CLKFX are phase aligned to CLKIN. When the CLKFB pin is not connected, set CLK_FEEDBACK to NONE and only the CLKFX and CLKFX180 outputs are valid, however, not phase aligned to CLKIN.
Status Outputs/Control Inputs			
LOCKED	Output	1	Synchronous output from the PLL that provides you with an indication that the PLL has achieved phase alignment and is ready for operation.
PSDONE	Output	1	Dynamic CLKIN select input. When high, '1' CLKIN1 is selected and while low, '0' CLKIN2 is selected. If dual clock selection is not necessary, connect this input to a logic 1.

Port	Direction	Width	Function
RST	Input	1	The reset (RST) input pin resets the DCM circuitry. The RST signal is an active High asynchronous reset. Asserting the RST signal asynchronously forces all DCM outputs Low (the LOCKED signal, all status signals, and all output clocks within four source clock cycles). Because the reset is asynchronous, the last cycle of the clocks can exhibit an unintended short pulse, severely distorted duty-cycle, and no longer phase adjust with respect to one another while deasserting. The RST pin must be used when reconfiguring the device or changing the input frequency. Deasserting the RST signal synchronously starts the locking process at the next CLKIN cycle. To ensure a proper DCM reset and locking process, the RST signal must be deasserted after the CLKIN signal has been present and stable for at least three clock cycles. In all designs, the DCM must be held in reset until the clock is stable. During configuration, the DCM is automatically held in reset until GSR is released. If the clock is stable when GSR is released.
PSCLK	Input	1	The phase-shift clock (PSCLK) input pin provides the source clock for the DCM phase shift. The phase-shift clock signal can be driven by any clock source (external or internal). The frequency range of PSCLK is defined by PSCLK_FREQ_LF/HF (see the Data Sheet for this architecture). This input must be tied to ground when the CLKOUT_PHASE_SHIFT attribute is set to NONE or FIXED.
PSINCDEC	Input	1	The PSINCDEC input signal is synchronous with PSCLK. The PSINCDEC input signal is used to increment or decrement the phase-shift factor when CLKOUT_PHASE_SHIFT is set to one of the variable modes. As a result, the output clock is phase shifted. the PSINCDEC signal is asserted High for increment, or deasserted Low for decrement. This input must be tied to ground when the CLKOUT_PHASE_SHIFT attribute is set to NONE or FIXED.
PSEN	Input	1	The PSEN input signal is synchronous with PSCLK. A variable phase-shift operation is initiated by the PSEN input signal when CLKOUT_PHASE_SHIFT is set to a variable mode. It must be activated for one period of PSCLK. After PSEN is initiated, the phase change is effective for up to 100 CLKIN pulse cycles, plus three PSCLK cycles, and is indicated by a High pulse on PSDONE. There are no sporadic changes or glitches on any output during the phase transition. From the time PSEN is enabled until PSDONE is flagged, the DCM output clock moves bit-by-bit from its original phase shift to the target phase shift. The phase-shift is complete when PSDONE is flagged. PSEN must be tied to ground when the CLKOUT_PHASE_SHIFT attribute is set to NONE or FIXED.
Dynamic Reconfiguration/DCM Status			
For more information on Dynamic Configuration, please see the Configuration User Guide.			
DO	Output	16	The DO output bus provides DCM status when not using the dynamic reconfiguration feature, and a data output when using the dynamic reconfiguration. When showing DCM status, the following mapping applies: <ul style="list-style-type: none"> DO[0] - Phase-shift overflow DO[1] - CLKIN stopped DO[2] - CLKFX stopped DO[3] - CLKFB stopped DO[15:4] - Not assigned
DRDY	Output	1	The DRDY output pin provides ready status for the DCM's dynamic reconfiguration feature
DI	Input	16	The DI input bus provides reconfiguration data for dynamic reconfiguration. When not used, all bits must be assigned zeros.
DADDR	Input	7	The DADDR input bus provides a reconfiguration address for dynamic reconfiguration. When not used, all bits must be assigned zeros.

Port	Direction	Width	Function
DWE	Input	1	The DWE input pin provides the write enable control signal to write the DI data into the DADDR address. When not used, it must be tied Low.
DEN	Input	1	The DEN input pin provides the enable control signal to access the dynamic reconfiguration feature. To reflect the DCM status signals on the DO output bus when the dynamic reconfiguration feature is not used, DEN should be tied low.
DCLK	Input	1	The DCLK input pin provides the source clock for the DCM's dynamic reconfiguration circuit. The frequency of DCLK can be asynchronous (in phase and frequency) to CLKIN. The dynamic reconfiguration clock signal is driven by any clock source. The frequency range of DCLK is described in the Data Sheet for this architecture. When dynamic reconfiguration is not used, this input must be tied to ground.

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
CLK_FEEDBACK	String	"1X" , or "NONE"	"1X"	Specifies the clock feedback of the allowed value.
CLKDV_DIVIDE	Float	1.5, 2.0, 2.5, 3.0, 3.5, 4.0, 4.5, 5.0, 5.5, 6.0, 6.5, 7.0, 7.5, 8.0, 9.0, 10.0, 11.0, 12.0, 13.0, 14.0, 15.0, 16.0	2.0	Specifies the extent to which the CLKDLL, CLKDLLE, CLKDLLHF, or DCM clock divider (CLKDV output) is to be frequency divided.
CLKFX_DIVIDE	Integer	1 to 32	1	Specifies the frequency divider value for the CLKFX output.
CLKFX_MULTIPLY	Integer	2 to 32	4	Specifies the frequency multiplier value for the CLKFX output.
CLKIN_DIVIDE_BY_2	Boolean	FALSE, TRUE	FALSE	Allows for the input clock frequency to be divided in half when such a reduction is necessary to meet the DCM input clock frequency requirements.
CLKIN_PERIOD	Float	1.25 to 1000.00	10.0	Specifies period of input clock in ns from 1.25 to 1000.00.
CLKOUT_PHASE_SHIFT	String	"NONE", "FIXED", "VARIABLE_POSITIVE", "VARIABLE_CENTER" or "DIRECT"	"NONE"	Specifies the phase shift mode of allowed value.
DCM_PERFORMANCE_MODE	String	"MAX_SPEED" or "MAX_RANGE"	"MAX_SPEED"	Allows selection between maximum frequency and minimum jitter for low frequency and maximum phase shift range.

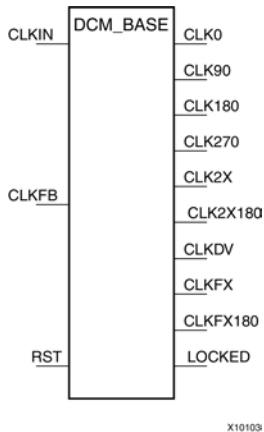
Attribute	Type	Allowed Values	Default	Description
DESKEW_ADJUST	String	"SOURCE_SYNCHRONOUS", "SYSTEM_SYNCHRONOUS" or "0" to "15"	"SYSTEM_SYNCHRONOUS"	Affects the amount of delay in the feedback path, and should be used for source-synchronous interfaces.
DFS_FREQUENCY_MODE	String	"LOW" or "HIGH"	"LOW"	Specifies the frequency mode of the frequency synthesizer.
DLL_FREQUENCY_MODE	String	"LOW" or "HIGH"	"LOW"	Specifies the DLL's frequency mode.
DUTY_CYCLE_CORRECTION	Boolean	TRUE, FALSE	TRUE	Corrects the duty cycle of the CLK0, CLK90, CLK180, and CLK270 outputs.
FACTORY_JF	Hexa-decimal	Any 16-Bit value.	F0F0	The FACTORY_JF attribute affects the DCMs jitter filter characteristic. The default value should not be modified unless otherwise instructed by Xilinx.
PHASE_SHIFT	Integer	-255 to 1023	0	Specifies the phase shift numerator. The range depends on CLKOUT_PHASE_SHIFT.
SIM_DEVICE	String	"VIRTEX4" or "VIRTEX5"	"VIRTEX5"	Device selection.
STARTUP_WAIT	Boolean	FALSE, TRUE	FALSE	When TRUE, the configuration startup sequence waits in the specified cycle until the DCM locks.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

DCM_BASE

Primitive: Base Digital Clock Manager Circuit



Introduction

This design element is a configurable DLL with additional phase and frequency synthesis control capabilities. This component is commonly used for many FPGA applications in order to derive and control the various clocks needed within the system. If dynamic reconfiguration is necessary, use the DCM_ADV component. If dynamic phase shift is required, use the DCM_PS component.

Port Descriptions

Port	Direction	Width	Function
Clock Outputs/Inputs			
CLK0	Output	1	The CLK0 output clock provides a clock with the same frequency as the DCM's effective CLKIN frequency. By default, the effective CLKIN frequency is equal to the CLKIN frequency, except when the CLKIN_DIVIDE_BY_2 attribute is set to TRUE. When CLKFB is connected, CLK0 is phase aligned to CLKIN.
CLK90	Output	1	The CLK90 output clock provides a clock with the same frequency as the DCM's CLK0 only phase-shifted by 90°.
CLK180	Output	1	The CLK180 output clock provides a clock with the same frequency as the DCM's CLK0 only phase-shifted by 180°.
CLK270	Output	1	The CLK270 output clock provides a clock with the same frequency as the DCM's CLK0 only phase-shifted by 270°.
CLK2X	Output	1	The CLK2X output clock provides a clock that is phase aligned to CLK0, with twice the CLK0 frequency, and with an automatic 50/50 duty-cycle correction. Until the DCM is locked, the CLK2X output appears as a 1x version of the input clock with a 25/75 duty cycle. This behavior allows the DCM to lock on the correct edge with respect to the source clock.
CLK2X180	Output	1	The CLK2X180 output clock provides a clock with the same frequency as the DCM's CLK2X only phase-shifted by 180°.
CLKDV	Output	1	The frequency divide (CLKDV) output clock provides a clock that is phase aligned to CLK0 with a frequency that is a fraction of the effective CLKIN frequency. The fraction is determined by the CLKDV_DIVIDE attribute. By default, the effective CLKIN frequency is equal to the CLKIN frequency, except when the CLKIN_DIVIDE_BY_2 attribute is set to TRUE.

Port	Direction	Width	Function
CLKFX	Output	1	<p>The frequency (CLKFX) output clock provides a clock with the following frequency definition:</p> $\text{CLKFX Frequency} = (M/D) \times (\text{Effective CLKIN Frequency})$ <p>In this equation, M is the multiplier (numerator) with a value defined by the CLKFX_MULTIPLY attribute. D is the divisor (denominator) with a value defined by the CLKFX_DIVIDE attribute. Specifications for M and D, as well as input and output frequency ranges for the frequency synthesizer, are provided in the Data Sheet for this architecture. The rising edge of CLKFX output is phase aligned to the rising edges of CLK0, CLK2X, and CLKDV when the feedback path (CLKFB) is used. When M and D have no common factor, the alignment occurs only once every D cycles of CLK0. By default, the effective CLKIN frequency is equal to the CLKIN frequency, except when the CLKIN_DIVIDE_BY_2 attribute is set to TRUE.</p>
CLKFX180	Output	1	The CLKFX180 output clock provides a clock with the same frequency as the DCM's CLKFX only phase-shifted by 180°.
CLKIN	Input	1	<p>The source clock (CLKIN) input pin provides the source clock to the DCM. The CLKIN frequency must fall in the ranges specified in the Data Sheet for this architecture. The clock input signal comes from one of the following buffers:</p> <ul style="list-style-type: none"> • IBUFG - Global Clock Input Buffer. The DCM compensates for the clock input path when an IBUFG on the same edge (top or bottom) of the device as the DCM is used. • BUFG/BUFGCTRL - Internal Global Clock Buffer. Any BUFGCTRL can drive any DCM in the device using the dedicated global routing. A BUFGCTRL can drive the DCM CLKIN pin when used to connect two DCM in series. • IBUF - Input Buffer. When IBUF drives CLKIN input, the PAD to DCM input skew is not compensated and increased jitter can occur. This configuration is generally not recommended.
CLKFB	Input	1	<p>The feedback clock (CLKFB) input pin provides a reference or feedback signal to the DCM to delay-compensate the clock outputs, and align it with the clock input. To provide the necessary feedback to the DCM, connect only the CLK0 output to the CLKFB input via a BUFG component in the case of internal feedback or an OBUF ' IBUFG to the case of external feedback. Set the CLK_FEEDBACK attribute to 1X. When the CLKFB pin is connected, CLK0, CLKDV, and CLKFX are phase aligned to CLKIN. When the CLKFB pin is not connected, set CLK_FEEDBACK to NONE and only the CLKFX and CLKFX180 outputs are valid. However, they are not phase aligned to CLKIN.</p>
Status Outputs/Control Inputs			
LOCKED	Output	1	Synchronous output from the PLL that provides you with an indication the PLL has achieved phase alignment and is ready for operation.
RST	Input	1	<p>The reset (RST) input pin resets the DCM circuitry. The RST signal is an active High asynchronous reset. Asserting the RST signal asynchronously forces all DCM outputs Low (the LOCKED signal, all status signals, and all output clocks within four source clock cycles). Because the reset is asynchronous, the last cycle of the clocks can exhibit an unintended short pulse, severely distorted duty-cycle, and no longer phase adjust with respect to one another while deasserting. The RST pin must be used when reconfiguring the device or changing the input frequency. Deasserting the RST signal synchronously starts the locking process at the next CLKIN cycle. To ensure a proper DCM reset and locking process, the RST signal must be deasserted after the CLKIN signal has been present and stable for at least three clock cycles. In all designs, the DCM must be held in reset until the clock is stable. During configuration, the DCM is automatically held in reset until GSR is released. If the clock is stable when GSR is released.</p>

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
CLK_FEEDBACK	String	"1X", "2X", or "NONE"	"1X"	Specifies the feedback input to the DCM (CLK0, or CLK2X).
CLKDV_DIVIDE	Float	1.5, 2.0, 2.5, 3.0, 3.5, 4.0, 4.5, 5.0, 5.5, 6.0, 6.5, 7.0, 7.5, 8.0, 9.0, 10.0, 11.0, 12.0, 13.0, 14.0, 15.0, 16.0	2.0	Specifies the extent to which the CLKDLL, CLKDLLE, CLKDLLHF, or DCM clock divider (CLKDV output) is to be frequency divided.
CLKFX_DIVIDE	Integer	1 to 32	1	Specifies the frequency divider value for the CLKFX output.
CLKFX_MULTIPLY	Integer	2 to 32	4	Specifies the frequency multiplier value for the CLKFX output.
CLKIN_DIVIDE_BY_2	Boolean	FALSE, TRUE	FALSE	Allows for the input clock frequency to be divided in half when such a reduction is necessary to meet the DCM input clock frequency requirements.
CLKIN_PERIOD	Float	1.25 to 1000.00	10.0	Specifies the period of input clock in ns from 1.25 to 1000.00.
CLKOUT_PHASE_SHIFT	String	"NONE", "FIXED", "VARIABLE_POSITIVE", "VARIABLE_CENTER" or "DIRECT"	"NONE"	Specifies the phase shift mode of allowed value.
DCM_PERFORMANCE_MODE	String	"MAX_SPEED" or "MAX_RANGE"	"MAX_SPEED"	Allows selection between maximum frequency and minimum jitter for low frequency and maximum phase shift range.
DESKEW_ADJUST	String	"SOURCE_SYNCHRONOUS", "SYSTEM_SYNCHRONOUS" or "0" to "15"	"SYSTEM_SYNCHRONOUS"	Affects the amount of delay in the feedback path, and should be used for source-synchronous interfaces.
DFS_FREQUENCY_MODE	String	"LOW" or "HIGH"	"LOW"	Specifies the frequency mode of the frequency synthesizer.
DLL_FREQUENCY_MODE	String	"LOW" or "HIGH"	"LOW"	This specifies the DLL's frequency mode
DUTY_CYCLE_CORRECTION	Boolean	TRUE, FALSE	TRUE	Corrects the duty cycle of the CLK0, CLK90, CLK180, and CLK270 outputs.
FACTORY_JF	Hexa-decimal	Any 16-Bit Value	F0F0	The FACTORY_JF attribute affects the DCMs jitter filter characteristic. This attribute is set the default value should not be modified unless otherwise instructed by Xilinx.
PHASE_SHIFT	Integer	-255 to 1023	0	Specifies the phase shift numerator. The range depends on CLKOUT_PHASE_SHIFT.

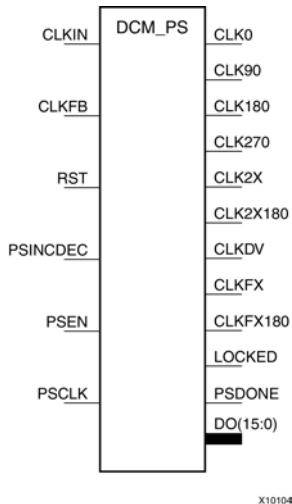
Attribute	Type	Allowed Values	Default	Description
STARTUP_WAIT	Boolean	FALSE, TRUE	FALSE	When set to TRUE, the configuration startup sequence waits in the specified cycle until the DCM locks.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

DCM_PS

Primitive: Digital Clock Manager with Basic and Phase Shift Features



Introduction

This design element is a configurable DLL with additional phase and frequency synthesis control capabilities. This component is commonly used for many FPGA applications in order to derive and control the various clocks needed within the system. If dynamic reconfiguration is necessary, use the DCM_ADV. If Dynamic Phase shift is not necessary, use the DCM_BASE component.

Port Descriptions

Port	Direction	Width	Function
Clock Outputs/Inputs			
CLK0	Output	1	The CLK0 output clock provides a clock with the same frequency as the DCM's effective CLKIN frequency. By default, the effective CLKIN frequency is equal to the CLKIN frequency, except when the CLKIN_DIVIDE_BY_2 attribute is set to TRUE. When CLKFB is connected, CLK0 is phase aligned to CLKIN.
CLK90	Output	1	The CLK90 output clock provides a clock with the same frequency as the DCM's CLK0 only phase-shifted by 90°.
CLK180	Output	1	The CLK180 output clock provides a clock with the same frequency as the DCM's CLK0 only phase-shifted by 180°.
CLK270	Output	1	The CLK270 output clock provides a clock with the same frequency as the DCM's CLK0 only phase-shifted by 270°.
CLK2X	Output	1	The CLK2X output clock provides a clock that is phase aligned to CLK0, with twice the CLK0 frequency, and with an automatic 50/50 duty-cycle correction. Until the DCM is locked, the CLK2X output appears as a 1x version of the input clock with a 25/75 duty cycle. This behavior allows the DCM to lock on the correct edge with respect to the source clock.
CLK2X180	Output	1	The CLK2X180 output clock provides a clock with the same frequency as the DCM's CLK2X only phase-shifted by 180°.
CLKDV	Output	1	The frequency divide (CLKDV) output clock provides a clock that is phase aligned to CLK0 with a frequency that is a fraction of the effective CLKIN frequency. The fraction is determined by the CLKDV_DIVIDE attribute. By default, the effective CLKIN frequency is equal to the CLKIN frequency, except when the CLKIN_DIVIDE_BY_2 attribute is set to TRUE.

Port	Direction	Width	Function
CLKFX	Output	1	<p>The frequency (CLKFX) output clock provides a clock with the following frequency definition:</p> $\text{CLKFX Frequency} = (M/D) \times (\text{Effective CLKIN Frequency})$ <p>In this equation, M is the multiplier (numerator) with a value defined by the CLKFX_MULTIPLY attribute. D is the divisor (denominator) with a value defined by the CLKFX_DIVIDE attribute. Specifications for M and D, as well as input and output frequency ranges for the frequency synthesizer, are provided in the Data Sheet. The rising edge of CLKFX output is phase aligned to the rising edges of CLK0, CLK2X, and CLKDV when the feedback path (CLKFB) is used. When M and D to have no common factor, the alignment occurs only once every D cycles of CLK0. By default, the effective CLKIN frequency is equal to the CLKIN frequency, except when the CLKIN_DIVIDE_BY_2 attribute is set to TRUE.</p>
CLKFX180	Output	1	The CLKFX180 output clock provides a clock with the same frequency as the DCM's CLKFX only phase-shifted by 180°.
CLKIN	Input	1	<p>The source clock (CLKIN) input pin provides the source clock to the DCM. The CLKIN frequency must fall in the ranges specified in the Data Sheet. The clock input signal comes from one of the following buffers:</p> <ul style="list-style-type: none"> • IBUFG - Global Clock Input Buffer. The DCM compensates for the clock input path when an IBUFG on the same edge (top or bottom) of the device as the DCM is used. • BUFG/BUFGCTRL - Internal Global Clock Buffer. Any BUFGCTRL can drive any DCM in the device using the dedicated global routing. A BUFGCTRL can drive the DCM CLKIN pin when used to connect two DCM in series. • IBUF - Input Buffer. When IBUF drives CLKIN input, the PAD to DCM input skew is not compensated and increased jitter can occur. This configuration is generally not recommended.
CLKFB	Input	1	<p>The feedback clock (CLKFB) input pin provides a reference or feedback signal to the DCM to delay-compensate the clock outputs, and align it with the clock input. To provide the necessary feedback to the DCM, connect only the CLK0 output to the CLKFB input via a BUFG component in the case of internal feedback or an OBUF ' IBUFG to the case of external feedback. Set the CLK_FEEDBACK attribute to 1X. When the CLKFB pin is connected, CLK0, CLKDV, and CLKFX are phase aligned to CLKIN. When the CLKFB pin is not connected, set CLK_FEEDBACK to NONE and only the CLKFX and CLKFX180 outputs are valid. However, they are not phase aligned to CLKIN.</p>
Status Outputs/Control Inputs			
LOCKED	Output	1	Synchronous output from the PLL that provides you with an indication the PLL has achieved phase alignment and is ready for operation.
PSDONE	Output	1	Dynamic CLKIN select input. When high, '1' CLKIN1 is selected and while low, '0' CLKIN2 is selected. If dual clock selection is not necessary, connect this input to a logic 1.

Port	Direction	Width	Function
RST	Input	1	The reset (RST) input pin resets the DCM circuitry. The RST signal is an active High asynchronous reset. Asserting the RST signal asynchronously forces all DCM outputs Low (the LOCKED signal, all status signals, and all output clocks within four source clock cycles). Because the reset is asynchronous, the last cycle of the clocks can exhibit an unintended short pulse, severely distorted duty-cycle, and no longer phase adjust with respect to one another while deasserting. The RST pin must be used when reconfiguring the device or changing the input frequency. Deasserting the RST signal synchronously starts the locking process at the next CLKIN cycle. To ensure a proper DCM reset and locking process, the RST signal must be deasserted after the CLKIN signal has been present and stable for at least three clock cycles. In all designs, the DCM must be held in reset until the clock is stable. During configuration, the DCM is automatically held in reset until GSR is released. If the clock is stable when GSR is released.
PSCLK	Input	1	The phase-shift clock (PSCLK) input pin provides the source clock for the DCM phase shift. The phase-shift clock signal can be driven by any clock source (external or internal). The frequency range of PSCLK is defined by PSCLK_FREQ_LF/HF (see the Data Sheet). This input must be tied to ground when the CLKOUT_PHASE_SHIFT attribute is set to NONE or FIXED.
PSINCDEC	Input	1	The PSINCDEC input signal is synchronous with PSCLK. The PSINCDEC input signal is used to increment or decrement the phase-shift factor when CLKOUT_PHASE_SHIFT is set to one of the variable modes. As a result, the output clock is phase shifted. the PSINCDEC signal is asserted High for increment, or deasserted Low for decrement. This input must be tied to ground when the CLKOUT_PHASE_SHIFT attribute is set to NONE or FIXED.
PSEN	Input	1	The PSEN input signal is synchronous with PSCLK. A variable phase-shift operation is initiated by the PSEN input signal when CLKOUT_PHASE_SHIFT is set to a variable mode. It must be activated for one period of PSCLK. After PSEN is initiated, the phase change is effective for up to 100 CLKIN pulse cycles, plus three PSCLK cycles, and is indicated by a High pulse on PSDONE. There are no sporadic changes or glitches on any output during the phase transition. From the time PSEN is enabled until PSDONE is flagged, the DCM output clock moves bit-by-bit from its original phase shift to the target phase shift. The phase-shift is complete when PSDONE is flagged. PSEN must be tied to ground when the CLKOUT_PHASE_SHIFT attribute is set to NONE or FIXED.

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
CLK_FEEDBACK	String	"1X", "2X", or "NONE"	"1X"	Specifies the clock feedback of allowed value.
CLKDV_DIVIDE	FLOAT	1.5, 2.0, 2.5, 3.0, 3.5, 4.0, 4.5, 5.0, 5.5, 6.0, 6.5, 7.0, 7.5, 8.0, 9.0, 10.0, 11.0, 12.0, 13.0, 14.0, 15.0, 16.0	2.0	Specifies the extent to which the CLKDLL, CLKDLLL, CLKDLLHF, or DCM clock divider (CLKDV output) is to be frequency divided.
CLKFX_DIVIDE	Integer	1 to 32	1	Specifies the frequency divider value for the CLKFX output.

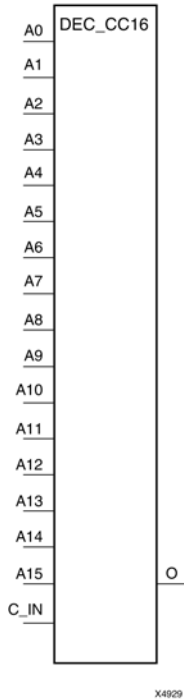
Attribute	Type	Allowed Values	Default	Description
CLKFX_MULTIPLY	Integer	2 to 32	4	Specifies the frequency multiplier value for the CLKFX output.
CLKIN_DIVIDE_BY_2	Boolean	FALSE, TRUE	FALSE	Allows for the input clock frequency to be divided in half when such a reduction is necessary to meet the DCM input clock frequency requirements.
CLKIN_PERIOD	FLOAT	1.25 to 1000.00	10.0	Specifies the period of input clock in ns from 1.25 to 1000.00.
CLKOUT_PHASE_SHIFT	String	"NONE", "FIXED", "VARIABLE_POSITIVE", "VARIABLE_CENTER" or "DIRECT"	"NONE"	Specifies the phase shift mode of allowed value.
DESKEW_ADJUST	String	"SOURCE_SYNCHRONOUS", "SYSTEM_SYNCHRONOUS" or "0" to "15"	"SYSTEM_SYNCHRONOUS"	Affects the amount of delay in the feedback path, and should be used for source-synchronous interfaces.
DFS_FREQUENCY_MODE	String	"LOW" or "HIGH"	"LOW"	Specifies the frequency mode of the frequency synthesizer.
DLL_FREQUENCY_MODE	String	"LOW" or "HIGH"	"LOW"	This specifies the DLL's frequency mode.
DUTY_CYCLE_CORRECTION	Boolean	TRUE, FALSE	TRUE	Corrects the duty cycle of the CLK0, CLK90, CLK180, and CLK270 outputs.
FACTORY_JF	Hexa-decimal	Any 16-Bit Value	F0F0	The FACTORY_JF attribute affects the DCM's jitter filter characteristic. This attribute is set and the default value should not be modified unless otherwise instructed by Xilinx.
PHASE_SHIFT	Integer	-255 to 1023	0	Specifies the phase shift numerator. The range depends on CLKOUT_PHASE_SHIFT.
STARTUP_WAIT	Boolean	FALSE, TRUE	FALSE	When set to TRUE, the configuration startup sequence waits in the specified cycle until the DCM locks.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

DEC_CC16

Macro: 16-Bit Active Low Decoder



Introduction

This design element is a 16-bit decoder that is used to build wide-decoder functions. It is implemented by cascading CY_MUX elements driven by look-up tables (LUTs). The C_IN pin can only be driven by the output (O) of a previous decode stage. When one or more of the inputs (A) are Low, the output is Low. When all the inputs are High and the C_IN input is High, the output is High. You can decode patterns by adding inverters to inputs.

Logic Table

Inputs					Outputs
A0	A1	...	Az	C_IN	O
1	1	1	1	1	1
X	X	X	X	0	0
0	X	X	X	X	0
X	0	X	X	X	0
X	X	X	0	X	0

z = 3 for DEC_CC4; z = 7 for DEC_CC8; z = 15 for DEC_CC16

Design Entry Method

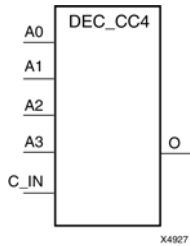
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

DEC_CC4

Macro: 4-Bit Active Low Decoder



Introduction

This design element is a 4-bit decoder that is used to build wide-decoder functions. It is implemented by cascading CY_MUX elements driven by look-up tables (LUTs). The C_IN pin can only be driven by the output (O) of a previous decode stage. When one or more of the inputs (A) are Low, the output is Low. When all the inputs are High and the C_IN input is High, the output is High. You can decode patterns by adding inverters to inputs.

Logic Table

Inputs					Outputs
A0	A1	...	Az	C_IN	O
1	1	1	1	1	1
X	X	X	X	0	0
0	X	X	X	X	0
X	0	X	X	X	0
X	X	X	0	X	0
z = 3 for DEC_CC4; z = 7 for DEC_CC8; z = 15 for DEC_CC16					

Design Entry Method

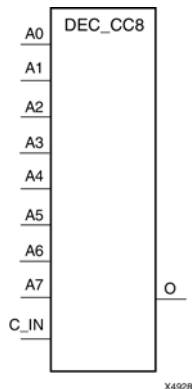
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

DEC_CC8

Macro: 8-Bit Active Low Decoder



Introduction

This design element is a 8-bit decoder that is used to build wide-decoder functions. It is implemented by cascading CY_MUX elements driven by look-up tables (LUTs). The C_IN pin can only be driven by the output (O) of a previous decode stage. When one or more of the inputs (A) are Low, the output is Low. When all the inputs are High and the C_IN input is High, the output is High. You can decode patterns by adding inverters to inputs.

Logic Table

Inputs					Outputs
A0	A1	...	Az	C_IN	O
1	1	1	1	1	1
X	X	X	X	0	0
0	X	X	X	X	0
X	0	X	X	X	0
X	X	X	0	X	0
z = 3 for DEC_CC4; z = 7 for DEC_CC8; z = 15 for DEC_CC16					

Design Entry Method

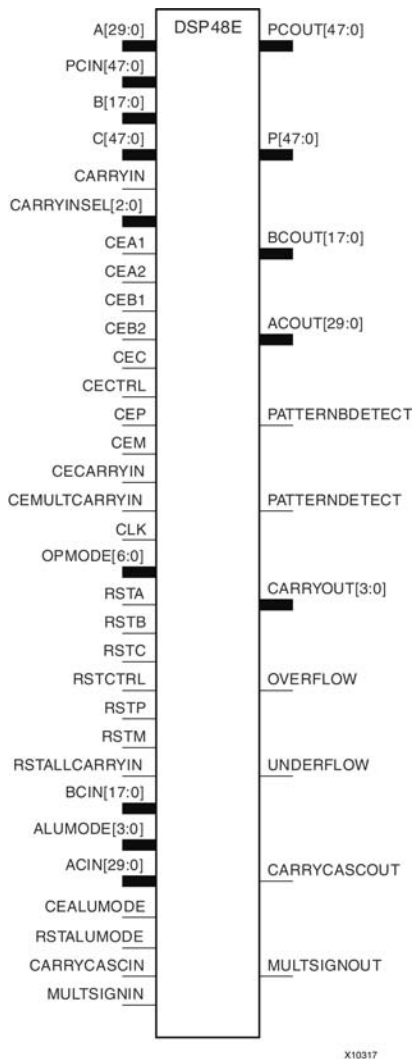
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

DSP48E

Primitive: 25x18 Two's Complement Multiplier with Integrated 48-Bit, 3-Input Adder/Subtractor/Accumulator or 2-Input Logic Unit



Introduction

This design element is a versatile, scalable, hard IP block that allows for the creation of compact, high-speed, arithmetic-intensive operations, such as those seen for many DSP algorithms. Some of the functions capable within the block include multiplication, addition, subtraction, accumulation, shifting, logical operations, and pattern detection.

Port Descriptions

Port	Direction	Width	Function
Data Ports			
A	Input	30	25-bit data input to multiplier or 30-bit MSB Data input to Adder/Logic Unit (LU).
B	Input	18	18-bit data input to multiplier or 18-bit LSB Data input to Adder/Logic Unit.

Port	Direction	Width	Function
C	Input	48	48-bit data input to adder/Logic Unit and Pattern Detector.
CARRYIN	Input	1	External carry input to the adder/Logic Unit.
P	Output	48	Primary data output.
CARRYOUT	Output	4	Carry out signal for arithmetic operations (addition, subtraction, etc.). <ul style="list-style-type: none"> If USE_SIMD="FOUR12", CARRYOUT[3:0] represents the carryout of each 12 bit field of the Accumulate/Adder/Logic Unit. If USE_SIMD="TWO24", CARRYOUT[3] and CARRYOUT[1] represents the carryout of each 24-bit field of the Accumulator/Adder. If USE_SIMD="ONE48", CARRYOUT[3] is the only valid carry out from the Accumulate/Adder/Logic Unit.
Control Inputs/Status Bits			
CLK	Input	1	DSP48E clock input.
OPMODE	Input	7	Control input to select the arithmetic operation of the DSP48E in conjunction with ALUMODE.
ALUMODE	Input	4	Control input to select Logic Unit functions including addition and subtraction.
CARRYINSEL	Input	3	Selects carry in source to the DSP48E.
OVERFLOW	Output	1	Active High output detects overflow in addition/accumulate if pattern detector is used and PREG = 1.
UNDERFLOW	Output	1	Active High output detects underflow in addition/accumulate if pattern detector is used and PREG = 1.
PATTERNDETECT	Output	1	Active High pattern detection. Detects match of P and the selected PATTERN gated by the MASK. Result arrives on the same cycle as P.
PATTERN BDETECT	Output	1	Active High pattern detection. Detects match of P and the bar of the selected PATTERN gated by the MASK. Result arrives on the same cycle as P.
Reset/Clock Enable Inputs			
RSTA	Input	1	Active High, synchronous reset for the A port registers (AREG=1 or 2). Tie to logic zero if not used.
RSTB	Input	1	Active High, synchronous reset for the B port registers (BREG=1 or 2). Tie to logic zero if not used.
RSTC	Input	1	Active High, synchronous reset for the C port registers (CREG=1). Tie to logic zero if not used.
RSTM	Input	1	Active High, synchronous reset for the multiplier registers (MREG=1). Tie to logic zero if not used.
RSTP	Input	1	Active High, synchronous reset for the P, UNDERFLOW, OVERFLOW, PATTERNDETECT and PATTERNBDETECT and CARRYOUT output registers (PREG=1). Tie to logic zero if not used.
RSTCTRL	Input	1	Active High, synchronous reset for the OPMODE and CARRYINSEL registers (OPMODEREG=1 and CARRYINSELREG=1). Tie to logic zero if not used.

Port	Direction	Width	Function
RSTALLCARRYIN	Input	1	Active High, synchronous reset for all carry-in registers (CARRYINREG=1) or MULTCARRYINREG=1. Tie to logic zero if not used.
RSTALUMODE	Input	1	Active High, synchronous reset for the ALUMODE registers (ALUMODEREG=1). Tie to logic zero if not used.
CEA1	Input	1	Active High, clock enable for the A port registers (AREG=2). Tie to logic one if not used and AREG=2. Tie to logic zero if AREG=0 or 1. When two registers are used, this is the first sequentially.
CEA2	Input	1	Active High, clock enable for the A port registers. Tie to logic one if not used and AREG=1 or 2. Tie to logic zero if AREG=0. When two registers are used, this is the second sequentially.
CEB1	Input	1	Active High, clock enable for the B port registers (BREG=2). Tie to logic one if not used and BREG=2. Tie to logic zero if BREG=0 or 1. When two registers are used, this is the first sequentially.
CEB2	Input	1	Active High, clock enable for the B port registers. Tie to logic one if not used and BREG=1 or 2. Tie to logic zero if BREG=0. When two registers are used, this is the second sequentially.
CEC	Input	1	Active High, clock enable for the C port registers (CREG=1). Tie to logic one if not used.
CEM	Input	1	Active High, clock enable for the multiplier registers (MREG=1). Tie to logic one if not used.
CEP	Input	1	Active High, clock enable for the output port registers (PREG=1). Tie to logic one if not used.
CECTRL	Input	1	Active High, clock enable for the OPMODE and Carry-in Select registers (CTRLREG=1). Tie to logic one if not used.
CECARRYIN	Input	1	Active High, clock enable for the Carry-in registers (CARRYINREG=1). Tie to logic one if not used.
CEMULTCARRYIN	Input	1	Clock enable for internal multiply symmetric rounding carry register. (MULTCARRYINREG=1).
CEALUMODE	Input	1	Clock enable for the ALUMODE input registers (ALUMODEREG=1).
Cascade Ports			
ACIN	Input	30	Cascade input for Port A. If used, connect to ACOUT of upstream cascaded DSP48E. If not used, tie port to all zeros.
BCIN	Input	18	Cascade input for Port B. If used, connect to BCOUT of upstream cascaded DSP48E. If not used, tie port to all zeros.
PCIN	Input	48	Cascade input for Port P. If used, connect to PCOUT of upstream cascaded DSP48E. If not used, tie port to all zeros.
CARRYCASCIN	Input	1	Cascaded Carryout[2] from previous DSP48E.
MULTSIGNIN	Input	1	Communicates multiplier sign output of a cascaded DSP48E slice for the purpose of sign extending the adder/accumulator output when greater than a 48-bit output is necessary. Should only be connected to the MULTSIGNOUT output pin.
ACOUT	Output	30	Cascade output for Port A. If used, connect to ACIN of downstream cascaded DSP48E. If not used, leave unconnected.
BCOUT	Output	18	Cascade output for Port B. If used, connect to BCIN of downstream cascaded DSP48E. If not used, leave unconnected.
PCOUT	Output	48	Cascade output for Port P. If used, connect to PCIN of downstream cascaded DSP48E. If not used, leave unconnected.

Port	Direction	Width	Function
CARRYCASCOUT	Output	1	Cascaded Carryout[3] to next DSP48.
MULTSIGNOUT	Output	1	Communicates multiplier sign output to a cascaded DSP48E element for the purpose of sign extending the adder/accumulator output. Should only be connected to the MULTISIGNIN input pin.

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
ACASCREG	Integer	0, 1 or 2	1	In conjunction with AREG, selects number of A input registers on the ACIN cascade input. Must be equal to or one less than AREG value.
AREG	Integer	0, 1 or 2	1	Selects whether to register the A input to the DSP48E.
ALUMODEREG	Integer	0, 1	1	Selects whether to register the ALUMODE input pins or not.
AUTORESET_PATTERN_DETECT	Boolean	TRUE or FALSE	FALSE	Automatically reset DSP48E P Register (accumulated value or Counter Value) on next clock cycle if pattern detect event as determined by AUTORESET_PATTERN_DETECT_OPTINV has occurred on this clock cycle.
AUTORESET_PATTERN_DETECT_OPTINV	String	"MATCH", "NOT_MATCH"	"MATCH"	Determines if AUTORESET_PATTERN_DETECT should cause auto reset of P Register on the next cycle A) if pattern is matched or B) whenever pattern is not matched on the current cycle but was matched on the last clock cycle.
A_INPUT	String	"DIRECT" or "CASCADE"	"DIRECT"	Selects between A ("DIRECT") and ACIN ("CASCADE") inputs.
BCASCREG	Integer	0, 1, 2	1	In conjunction with BREG, selects number of B input registers on BCIN cascade input.
BREG	Integer	0, 1, 2	1	Selects whether to register the B input to the DSP48E.
B_INPUT	String	"DIRECT" or "CASCADE"	"DIRECT"	Selects between B ("DIRECT") and BCIN ("CASCADE") inputs.
CARRYINREG	Integer	0, 1	1	Selects whether to register the CARRYIN input to the DSP48E.
CARRYINSELREG	Integer	0, 1	1	Selects whether to register the CARRYINSEL input to the DSP48E.
CREG	Integer	0, 1	1	Selects whether to register the C input to the DSP48E.
MASK	Hexadecimal	Any 48-Bit Value	3FFF	Mask to be used for pattern detector.
MREG	Integer	0, 1	1	Selects whether to register the multiplier stage of the DSP48. Enable=1/disable=0.

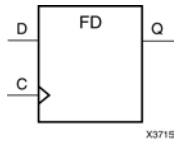
Attribute	Type	Allowed Values	Default	Description
MULTCARRYINREG	Integer	0, 1	1	Selects number of Internal Carry registers (used for Multiply Symmetric Rounding only).
OPMODEREG	Integer	0, 1	1	Selects whether to register the OPMODE inputs to the DSP48E.
PATTERN	Hexadecimal	Any 48-Bit Value	All zeros	Pattern to be used for pattern detector.
PREG	Integer	0, 1	1	Selects whether to register the P input to the DSP48E.
SEL_MASK	String	"MASK", "C"	"MASK"	Selects whether to use the static MASK or the C input for the mask of the pattern detector.
SEL_PATTERN	String	"PATTERN", "C"	"PATTERN"	Selects whether to use the static PATTERN or the C input for the pattern of the pattern detector.
SEL_ROUNDING_MASK	String	"SEL_MASK", "MODE1", "MODE2"	"SEL_MASK"	Selects special mask to be used for symmetric and convergent rounding uses of the pattern detector. If set to "MODE1" or "MODE2" SEL_MASK attribute is overridden. These are used for convergent rounding.
SIM_MODE	String	"SAFE" or "FAST"	"SAFE"	This is a simulation only attribute. It will direct the simulation model to run in performance-oriented mode when set to "FAST." Please see the <i>Synthesis and Simulation Design Guide</i> for more information.
USE_MULT	String	"MULT", "MULT_S", "NONE"	"MULT_S"	Selects usage of the Multiplier. Set to "NONE" to save power when using only the Adder/Logic Unit. Set to "MULT" if MREG is set to 0 and set to "MULT_S" if MREG is set to 1.
USE_SIMD	String	"ONE48", "TWO24", "FOUR12"	"ONE48"	Selects usage of the SIMD (Single Instruction Multiple Data) Adder/Logic Unit. Select between one 48-bit Logic Unit, two 24-bit Logic Unit, or four 12-bit Logic Unit. Note that all four 12 bit Logic Unit share the same Instruction (i.e. all can subtract on the same cycle or add on the same cycle). This does allow the 48 bit adder to be broken up into smaller adders for less computationally intensive applications. SIMD only has an effect on arithmetic operation (add, accumulate, subtract, etc.) and has no effect on logical operations.
USE_PATTERN_DETECT	String	"PAT_DET", "NO_PAT_DET"	"NO_PAT_DET"	Enables pattern detection. Only affects simulation model and speed files.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FD

Primitive: D Flip-Flop



Introduction

This design element is a D-type flip-flop with data input (D) and data output (Q). The data on the D inputs is loaded into the flip-flop during the Low-to-High clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs		Outputs
D	C	Q
0	↑	0
1	↑	1

Design Entry Method

This design element is only for use in schematics.

Available Attributes

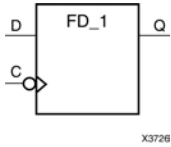
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FD_1

Primitive: D Flip-Flop with Negative-Edge Clock



Introduction

This design element is a single D-type flip-flop with data input (D) and data output (Q). The data on the (D) input is loaded into the flip-flop during the High-to-Low clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs		Outputs
D	C	Q
0	↓	0
1	↓	1

Design Entry Method

This design element is only for use in schematics.

Available Attributes

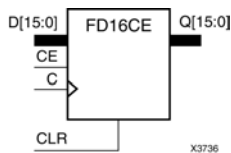
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FD16CE

Macro: 16-Bit Data Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a 16-bit data register with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q) during the Low-to-High clock (C) transition. When CLR is High, it overrides all other inputs and resets the data outputs (Q) Low. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs
CLR	CE	Dz : D0	C	Qz : Q0
1	X	X	X	0
0	0	X	X	No Change
0	1	Dn	↑	Dn
z = bit-width - 1				

Design Entry Method

This design element is only for use in schematics.

Available Attributes

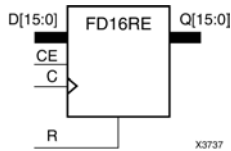
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	Any 16-bit Value	All zeros	Sets the initial value of Q output after configuration

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FD16RE

Macro: 16-Bit Data Register with Clock Enable and Synchronous Reset



Introduction

This design element is a 16-bit data registers. When the clock enable (CE) input is High, and the synchronous reset (R) input is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q0) during the Low-to-High clock (C) transition. When R is High, it overrides all other inputs and resets the data outputs (Q) Low on the Low-to-High clock transition. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs
R	CE	Dz : D0	C	Qz : Q0
1	X	X	↑	0
0	0	X	X	No Change
0	1	Dn	↑	Dn
z = bit-width - 1				

Design Entry Method

This design element is only for use in schematics.

Available Attributes

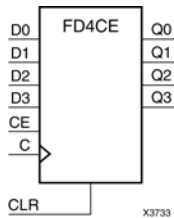
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	Any 16-Bit Value	All zeros	Sets the initial value of Q output after configuration.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FD4CE

Macro: 4-Bit Data Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a 4-bit data register with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q) during the Low-to-High clock (C) transition. When CLR is High, it overrides all other inputs and resets the data outputs (Q) Low. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs
CLR	CE	Dz : D0	C	Qz : Q0
1	X	X	X	0
0	0	X	X	No Change
0	1	Dn	↑	Dn
z = bit-width - 1				

Design Entry Method

This design element is only for use in schematics.

Available Attributes

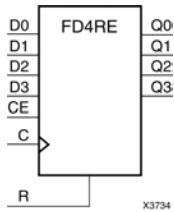
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	Any 4-Bit Value	All zeros	Sets the initial value of Q output after configuration.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FD4RE

Macro: 4-Bit Data Register with Clock Enable and Synchronous Reset



Introduction

This design element is a 4-bit data registers. When the clock enable (CE) input is High, and the synchronous reset (R) input is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q0) during the Low-to-High clock (C) transition. When R is High, it overrides all other inputs and resets the data outputs (Q) Low on the Low-to-High clock transition. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs
R	CE	Dz : D0	C	Qz : Q0
1	X	X	↑	0
0	0	X	X	No Change
0	1	Dn	↑	Dn
z = bit-width - 1				

Design Entry Method

This design element is only for use in schematics.

Available Attributes

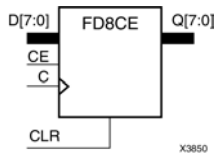
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	Any 4-Bit Value	All zeros	Sets the initial value of Q output after configuration.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FD8CE

Macro: 8-Bit Data Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a 8-bit data register with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q) during the Low-to-High clock (C) transition. When CLR is High, it overrides all other inputs and resets the data outputs (Q) Low. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs
CLR	CE	Dz : D0	C	Qz : Q0
1	X	X	X	0
0	0	X	X	No Change
0	1	Dn	↑	Dn
z = bit-width - 1				

Design Entry Method

This design element is only for use in schematics.

Available Attributes

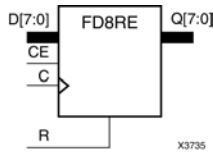
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	Any 8-Bit Value	All zeros	Sets the initial value of Q output after configuration.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FD8RE

Macro: 8-Bit Data Register with Clock Enable and Synchronous Reset



Introduction

This design element is an 8-bit data register. When the clock enable (CE) input is High, and the synchronous reset (R) input is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q0) during the Low-to-High clock (C) transition. When R is High, it overrides all other inputs and resets the data outputs (Q) Low on the Low-to-High clock transition. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs
R	CE	Dz : D0	C	Qz : Q0
1	X	X	↑	0
0	0	X	X	No Change
0	1	Dn	↑	Dn
z = bit-width - 1				

Design Entry Method

This design element is only for use in schematics.

Available Attributes

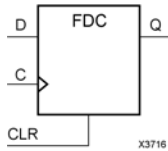
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	Any 8-Bit Value	All zeros	Sets the initial value of Q output after configuration.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FDC

Primitive: D Flip-Flop with Asynchronous Clear



Introduction

This design element is a single D-type flip-flop with data (D) and asynchronous clear (CLR) inputs and data output (Q). The asynchronous CLR, when High, overrides all other inputs and sets the (Q) output Low. The data on the (D) input is loaded into the flip-flop when CLR is Low on the Low-to-High clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
CLR	D	C	Q
1	X	X	0
0	D	↑	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

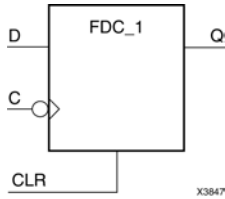
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FDC_1

Primitive: D Flip-Flop with Negative-Edge Clock and Asynchronous Clear



Introduction

FDC_1 is a single D-type flip-flop with data input (D), asynchronous clear input (CLR), and data output (Q). The asynchronous CLR, when active, overrides all other inputs and sets the (Q) output Low. The data on the (D) input is loaded into the flip-flop during the High-to-Low clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs			Outputs
CLR	D	C	Q
1	X	X	0
0	D	↓	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

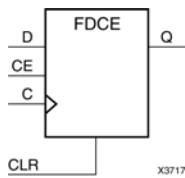
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FDCE

Primitive: D Flip-Flop with Clock Enable and Asynchronous Clear



Introduction

This design element is a single D-type flip-flop with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data input (D) of this design element is transferred to the corresponding data output (Q) during the Low-to-High clock (C) transition. When CLR is High, it overrides all other inputs and resets the data output (Q) Low. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs
CLR	CE	D	C	Q
1	X	X	X	0
0	0	X	X	No Change
0	1	D	↑	D

Design Entry Method

This design element can be used in schematics.

Available Attributes

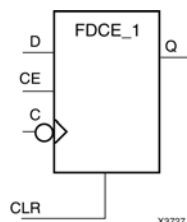
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0	0	Sets the initial value of Q output after configuration. For Spartan®-6 devices, the INIT value should always match the polarity of the set or reset. In the case of FDCE, the INIT should be 0. If set to 1, an asynchronous circuit must be created to exhibit this behavior, which Xilinx does not recommend.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FDCE_1

Primitive: D Flip-Flop with Negative-Edge Clock, Clock Enable, and Asynchronous Clear



Introduction

This design element is a single D-type flip-flop with data (D), clock enable (CE), asynchronous clear (CLR) inputs, and data output (Q). The asynchronous CLR input, when High, overrides all other inputs and sets the Q output Low. The data on the (D) input is loaded into the flip-flop when CLR is Low and CE is High on the High-to-Low clock (C) transition. When CE is Low, the clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs
CLR	CE	D	C	Q
1	X	X	X	0
0	0	X	X	No Change
0	1	D	↓	D

Design Entry Method

This design element can be used in schematics.

Available Attributes

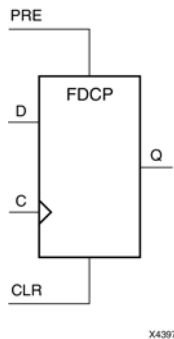
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0,1	0	Sets the initial value of Q output after configuration.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FDCP

Primitive: D Flip-Flop with Asynchronous Preset and Clear



Introduction

This design element is a single D-type flip-flop with data (D), asynchronous preset (PRE) and clear (CLR) inputs, and data output (Q). The asynchronous PRE, when High, sets the (Q) output High; CLR, when High, resets the output Low. Data on the (D) input is loaded into the flip-flop when PRE and CLR are Low on the Low-to-High clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs
CLR	PRE	D	C	Q
1	X	X	X	0
0	1	X	X	1
0	0	D	↑	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

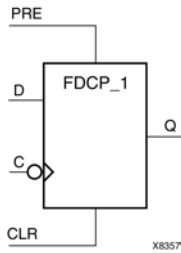
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FDCP_1

Primitive: D Flip-Flop with Negative-Edge Clock and Asynchronous Preset and Clear



Introduction

This design element is a single D-type flip-flop with data (D), asynchronous preset (PRE) and clear (CLR) inputs, and data output (Q). The asynchronous PRE, when High, sets the (Q) output High; CLR, when High, resets the output Low. Data on the (D) input is loaded into the flip-flop when PRE and CLR are Low on the High-to-Low clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs				Outputs
CLR	PRE	D	C	Q
1	X	X	X	0
0	1	X	X	1
0	0	0	↓	0
0	0	1	↓	1

Design Entry Method

This design element is only for use in schematics.

Available Attributes

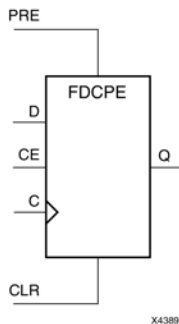
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0,1	0	Sets the initial value of Q output after configuration.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FDCPE

Primitive: D Flip-Flop with Clock Enable and Asynchronous Preset and Clear



Introduction

This design element is a single D-type flip-flop with data (D), clock enable (CE), asynchronous preset (PRE), and asynchronous clear (CLR) inputs. The asynchronous active high PRE sets the Q output High; that active high CLR resets the output Low and has precedence over the PRE input. Data on the D input is loaded into the flip-flop when PRE and CLR are Low and CE is High on the Low-to-High clock (C) transition. When CE is Low, the clock transitions are ignored and the previous value is retained. The FDCPE is generally implemented as a slice or IOB register within the device.

For FPGA devices, upon power-up, the initial value of this component is specified by the INIT attribute. If a subsequent GSR (Global Set/Reset) is asserted, the flop is asynchronously set to the INIT value.

Note While this device supports the use of asynchronous set and reset, it is not generally recommended to be used for in most cases. Use of asynchronous signals pose timing issues within the design that are difficult to detect and control and also have an adverse affect on logic optimization causing a larger design that can consume more power than if a synchronous set or reset is used.

Logic Table

Inputs					Outputs
CLR	PRE	CE	D	C	Q
1	X	X	X	X	0
0	1	X	X	X	1
0	0	0	X	X	No Change
0	0	1	D	↑	D

Port Descriptions

Port	Direction	Width	Function
Q	Output	1	Data output
C	Input	1	Clock input
CE	Input	1	Clock enable input
CLR	Input	1	Asynchronous clear input
D	Input	1	Data input
PRE	Input	1	Asynchronous set input

Design Entry Method

This design element can be used in schematics.

Available Attributes

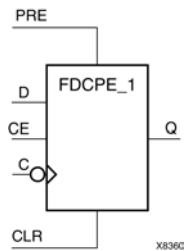
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0,1	0	Sets the initial value of Q output after configuration and on GSR.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FDCPE_1

Primitive: D Flip-Flop with Negative-Edge Clock, Clock Enable, and Asynchronous Preset and Clear



Introduction

FDCPE_1 is a single D-type flip-flop with data (D), clock enable (CE), asynchronous preset (PRE), and asynchronous clear (CLR) inputs and data output (Q). The asynchronous PRE, when High, sets the (Q) output High; CLR, when High, resets the output Low. Data on the (D) input is loaded into the flip-flop when PRE and CLR are Low and CE is High on the High-to-Low clock (C) transition. When CE is Low, the clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs					Outputs
CLR	PRE	CE	D	C	Q
1	X	X	X	X	0
0	1	X	X	X	1
0	0	0	X	X	No Change
0	0	1	D	↓	D

Port Descriptions

Port	Direction	Width	Function
Q	Output	1	Data output
C	Input	1	Clock input
CE	Input	1	Clock enable input
CLR	Input	1	Asynchronous clear input
D	Input	1	Data input
PRE	Input	1	Asynchronous set input

Design Entry Method

This design element can be used in schematics.

Available Attributes

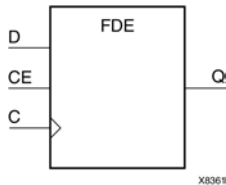
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0,1	0	Sets the initial value of Q output after configuration.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FDE

Primitive: D Flip-Flop with Clock Enable



Introduction

This design element is a single D-type flip-flop with data input (D), clock enable (CE), and data output (Q). When clock enable is High, the data on the (D) input is loaded into the flip-flop during the Low-to-High clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs
CE	D	C	Q
0	X	X	No Change
1	0	↑	0
1	1	↑	1

Design Entry Method

This design element is only for use in schematics.

Available Attributes

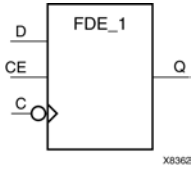
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FDE_1

Primitive: D Flip-Flop with Negative-Edge Clock and Clock Enable



Introduction

This design element is a single D-type flip-flop with data input (D), clock enable (CE), and data output (Q). When clock enable is High, the data on the (D) input is loaded into the flip-flop during the High-to-Low clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs
CE	D	C	Q
0	X	X	No Change
1	0	↓	0
1	1	↓	1

Design Entry Method

This design element is only for use in schematics.

Available Attributes

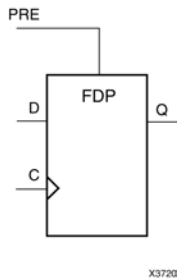
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FDP

Primitive: D Flip-Flop with Asynchronous Preset



Introduction

This design element is a single D-type flip-flop with data (D) and asynchronous preset (PRE) inputs and data output (Q). The asynchronous PRE, when High, overrides all other inputs and presets the (Q) output High. The data on the (D) input is loaded into the flip-flop when PRE is Low on the Low-to-High clock (C) transition.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
PRE	C	D	Q
1	X	X	1
0	↑	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

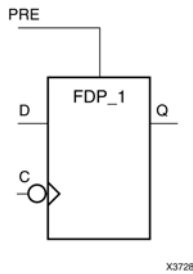
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FDP_1

Primitive: D Flip-Flop with Negative-Edge Clock and Asynchronous Preset



Introduction

This design element is a single D-type flip-flop with data (D) and asynchronous preset (PRE) inputs and data output (Q). The asynchronous PRE, when High, overrides all other inputs and presets the Q output High. The data on the D input is loaded into the flip-flop when PRE is Low on the High-to-Low clock (C) transition.

This flip-flop is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs
PRE	C	D	Q
1	X	X	1
0	↓	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

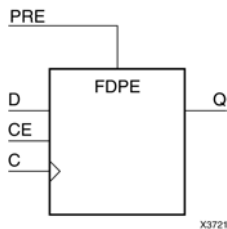
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FDPE

Primitive: D Flip-Flop with Clock Enable and Asynchronous Preset



Introduction

This design element is a single D-type flip-flop with data (D), clock enable (CE), and asynchronous preset (PRE) inputs and data output (Q). The asynchronous PRE, when High, overrides all other inputs and sets the (Q) output High. Data on the (D) input is loaded into the flip-flop when PRE is Low and CE is High on the Low-to-High clock (C) transition. When CE is Low, the clock transitions are ignored.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs
PRE	CE	D	C	Q
1	X	X	X	1
0	0	X	X	No Change
0	1	D	↑	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

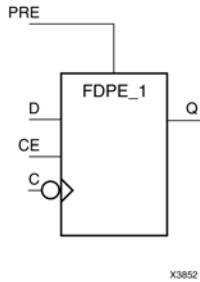
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	1	1	<p>Sets the initial value of Q output after configuration.</p> <p>For Spartan®-6 devices the INIT value should always match the polarity of the set or reset. In the case of FDPE, the init should be 1. If set to 0, an asynchronous circuit must be created to exhibit this behavior, which Xilinx does not recommend.</p>

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FDPE_1

Primitive: D Flip-Flop with Negative-Edge Clock, Clock Enable, and Asynchronous Preset



Introduction

This design element is a single D-type flip-flop with data (D), clock enable (CE), and asynchronous preset (PRE) inputs and data output (Q). The asynchronous PRE, when High, overrides all other inputs and sets the (Q) output High. Data on the (D) input is loaded into the flip-flop when PRE is Low and CE is High on the High-to-Low clock (C) transition. When CE is Low, the clock transitions are ignored.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs
PRE	CE	D	C	Q
1	X	X	X	1
0	0	X	X	No Change
0	1	D	↓	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

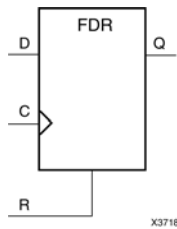
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FDR

Primitive: D Flip-Flop with Synchronous Reset



Introduction

This design element is a single D-type flip-flop with data (D) and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the (Q) output Low on the Low-to-High clock (C) transition. The data on the (D) input is loaded into the flip-flop when R is Low during the Low-to-High clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs
R	D	C	Q
1	X	↑	0
0	D	↑	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

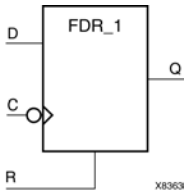
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FDR_1

Primitive: D Flip-Flop with Negative-Edge Clock and Synchronous Reset



Introduction

This design element is a single D-type flip-flop with data (D) and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the (Q) output Low on the High-to-Low clock (C) transition. The data on the (D) input is loaded into the flip-flop when R is Low during the High-to- Low clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs
R	D	C	Q
1	X	↓	0
0	D	↓	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

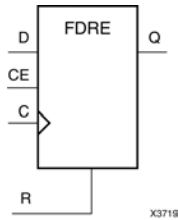
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FDRE

Primitive: D Flip-Flop with Clock Enable and Synchronous Reset



Introduction

This design element is a single D-type flip-flop with data (D), clock enable (CE), and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the (Q) output Low on the Low-to-High clock (C) transition. The data on the (D) input is loaded into the flip-flop when R is Low and CE is High during the Low-to-High clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs
R	CE	D	C	Q
1	X	X	↑	0
0	0	X	X	No Change
0	1	D	↑	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

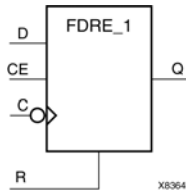
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0	0	Sets the initial value of Q output after configuration. For Spartan®-6 the INIT value should always match the polarity of the set or reset. In the case of FDRE, the INIT should be 0. If set to 1, extra logic is inserted.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FDRE_1

Primitive: D Flip-Flop with Negative-Clock Edge, Clock Enable, and Synchronous Reset



Introduction

FDRE_1 is a single D-type flip-flop with data (D), clock enable (CE), and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the (Q) output Low on the High-to-Low clock (C) transition. The data on the (D) input is loaded into the flip-flop when R is Low and CE is High during the High-to-Low clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs				Outputs
R	CE	D	C	Q
1	X	X	↓	0
0	0	X	X	No Change
0	1	D	↓	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

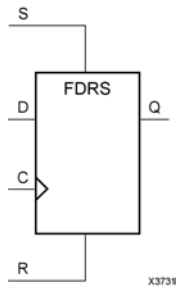
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FDRS

Primitive: D Flip-Flop with Synchronous Reset and Set



Introduction

FDRS is a single D-type flip-flop with data (D), synchronous set (S), and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the (Q) output Low during the Low-to-High clock (C) transition. (Reset has precedence over Set.) When S is High and R is Low, the flip-flop is set, output High, during the Low-to-High clock transition. When R and S are Low, data on the (D) input is loaded into the flip-flop during the Low-to-High clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs
R	S	D	C	Q
1	X	X	↓	0
0	1	X	↓	1
0	0	D	↓	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

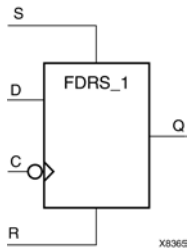
Attribute	Type	Allowed Values	Default	Description
IN	Binary	0, 1	0	Sets the initial value of Q output after configuration.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FDRS_1

Primitive: D Flip-Flop with Negative-Clock Edge and Synchronous Reset and Set



Introduction

FDRS_1 is a single D-type flip-flop with data (D), synchronous set (S), and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the (Q) output Low during the High-to-Low clock (C) transition. (Reset has precedence over Set.) When S is High and R is Low, the flip-flop is set, output High, during the High-to-Low clock transition. When R and S are Low, data on the (D) input is loaded into the flip-flop during the High-to-Low clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs				Outputs
R	S	D	C	Q
1	X	X	↓	0
0	1	X	↓	1
0	0	D	↓	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

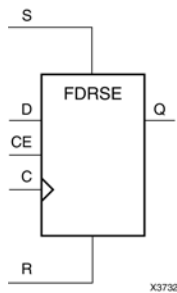
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FDRSE

Primitive: D Flip-Flop with Synchronous Reset and Set and Clock Enable



Introduction

FDRSE is a single D-type flip-flop with synchronous reset (R), synchronous set (S), clock enable (CE) inputs. The reset (R) input, when High, overrides all other inputs and resets the Q output Low during the Low-to-High clock transition. (Reset has precedence over Set.) When the set (S) input is High and R is Low, the flip-flop is set, output High, during the Low-to-High clock (C) transition. Data on the D input is loaded into the flip-flop when R and S are Low and CE is High during the Low-to-High clock transition.

Upon power-up, the initial value of this component is specified by the INIT attribute. If a subsequent GSR (Global Set/Reset) is asserted, the flop is asynchronously set to the INIT value.

Logic Table

Inputs					Outputs
R	S	CE	D	C	Q
1	X	X	X	↑	0
0	1	X	X	↑	1
0	0	0	X	X	No Change
0	0	1	1	↑	1
0	0	1	0	↑	0

Design Entry Method

This design element can be used in schematics.

Available Attributes

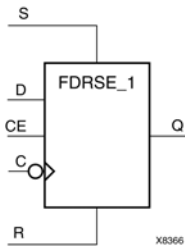
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration and on GSR.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FDRSE_1

Primitive: D Flip-Flop with Negative-Clock Edge, Synchronous Reset and Set, and Clock Enable



Introduction

FDRSE_1 is a single D-type flip-flop with synchronous reset (R), synchronous set (S), and clock enable (CE) inputs and data output (Q). The reset (R) input, when High, overrides all other inputs and resets the (Q) output Low during the High-to-Low clock transition. (Reset has precedence over Set.) When the set (S) input is High and R is Low, the flip-flop is set, output High, during the High-to-Low clock (C) transition. Data on the (D) input is loaded into the flip-flop when (R) and (S) are Low and (CE) is High during the High-to-Low clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs					Outputs
R	S	CE	D	C	Q
1	X	X	X	↓	0
0	1	X	X	↓	1
0	0	0	X	X	No Change
0	0	1	D	↓	D

Design Entry Method

This design element can be used in schematics.

Available Attributes

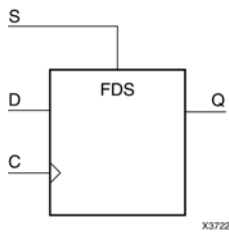
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration and on GSR.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FDS

Primitive: D Flip-Flop with Synchronous Set



Introduction

FDS is a single D-type flip-flop with data (D) and synchronous set (S) inputs and data output (Q). The synchronous set input, when High, sets the Q output High on the Low-to-High clock (C) transition. The data on the D input is loaded into the flip-flop when S is Low during the Low-to-High clock (C) transition.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
S	D	C	Q
1	X	↑	1
0	D	↑	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

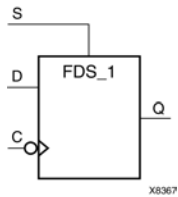
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FDS_1

Primitive: D Flip-Flop with Negative-Edge Clock and Synchronous Set



Introduction

FDS is a single D-type flip-flop with data (D) and synchronous set (S) inputs and data output (Q). The synchronous set input, when High, sets the Q output High on the Low-to-High clock (C) transition. The data on the D input is loaded into the flip-flop when S is Low during the Low-to-High clock (C) transition.

This flip-flop is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs
S	D	C	Q
1	X	↓	1
0	D	↓	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

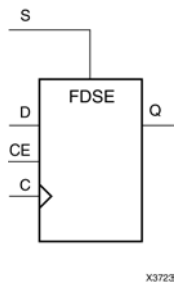
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FDSE

Primitive: D Flip-Flop with Clock Enable and Synchronous Set



Introduction

FDSE is a single D-type flip-flop with data (D), clock enable (CE), and synchronous set (S) inputs and data output (Q). The synchronous set (S) input, when High, overrides the clock enable (CE) input and sets the Q output High during the Low-to-High clock (C) transition. The data on the D input is loaded into the flip-flop when S is Low and CE is High during the Low-to-High clock (C) transition.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs				Outputs
S	CE	D	C	Q
1	X	X	↑	1
0	0	X	X	No Change
0	1	D	↑	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

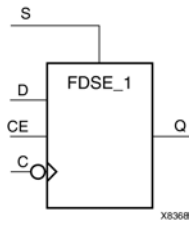
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	1	1	Sets the initial value of Q output after configuration. For Spartan®-6 devices the INIT value should always match the polarity of the set or reset. In the case of FDSE, the init should be 1. If set to 0, extra logic is inserted.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FDSE_1

Primitive: D Flip-Flop with Negative-Edge Clock, Clock Enable, and Synchronous Set



Introduction

FDSE_1 is a single D-type flip-flop with data (D), clock enable (CE), and synchronous set (S) inputs and data output (Q). The synchronous set (S) input, when High, overrides the clock enable (CE) input and sets the Q output High during the High-to-Low clock (C) transition. The data on the D input is loaded into the flip-flop when S is Low and CE is High during the High-to-Low clock (C) transition.

This flip-flop is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs				Outputs
S	CE	D	C	Q
1	X	X	↓	1
0	0	X	X	No Change
0	1	D	↓	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

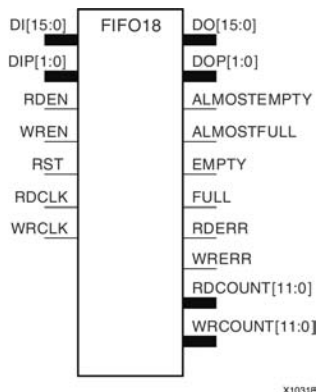
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FIFO18

Primitive: 18kb FIFO (First In, First Out) Block RAM Memory



Introduction

Virtex®-5 and above devices contain several block RAM memories, each of which can be separately configured as a FIFO, an automatic error-correction RAM, or as a general-purpose 36kb or 18kb RAM/ROM memory. These block RAM memories offer fast and flexible storage of large amounts of on-chip data. The FIFO18 uses the FIFO control logic and the 18kb block RAM. This primitive can be used in a 4-bit wide by 4K deep, 9-bit wide by 2K deep, or an 18-bit wide by 1K deep configuration. The primitive can be configured in either synchronous or multirate (asynchronous) mode, with all associated FIFO flags and status signals.

When using the dual-clock mode with independent clocks, depending on the offset between read and write clock edges, the Empty, Almost Empty, Full and Almost Full flags can deassert one cycle later. Due to the asynchronous nature of the clocks the simulation model only reflects the deassertion latency cycles listed in the architecture user guide.

Note For a 36-bit wide by 512 deep FIFO, use the FIFO18_36. For deeper or wider configurations of the FIFO, use the FIFO36 or FIFO36_72. If error-correction circuitry is desired, use the FIFO36_72.

Port Descriptions

Port	Direction	Width	Function
DO	Output	4, 8, 16	FIFO data output bus.
DOP	Output	0, 1, 2	FIFO parity data output bus.
FULL	Output	1	Active high logic indicates that the FIFO is full.
ALMOSTFULL	Output	1	Programmable flag to indicate that the FIFO is almost full. The ALMOST_FULL_OFFSET attribute specifies the threshold where this flag is triggered relative to full/empty.
EMPTY	Output	1	Active high logic to indicate that the FIFO is currently empty.
ALMOSTEMPTY	Output	1	Programmable flag to indicate the FIFO is almost empty. ALMOST_EMPTY_OFFSET attribute specifies the threshold where this flag is triggered relative to full/empty.
WRERR, RDERR	Output	1	WRERR indicates that a write occurred while the FIFO was full and RDERR indicates that a read occurred while the FIFO was empty
WRCOUNT, RDCOUNT	Output	12	FIFO write/read pointer.
DI	Input	4, 8, 16	FIFO data input bus.
DIP	Input	0, 1, 2	FIFO parity data input bus.

Port	Direction	Width	Function
WREN	Input	1	Active high FIFO write enable.
RDEN	Input	1	Active high FIFO read enable.
RST	Input	1	Asynchronous reset (active high) of all FIFO functions, flags, and pointers. RESET must be asserted for three clock cycles.
WRCLK, RDCLK	Input	1	FIFO read and write clocks (positive edge triggered).

Design Entry Method

This design element can be used in schematics.

When you want to instantiate this primitive configured in the 4-bit WIDTH mode, connect the DIP port to logic zeros and leave the DOP port unconnected. Connect DI[3:0] and DO[3:0] to the appropriate input and output signals and tie DI[15:4] to logic zeros and leave DO[15:4] unconnected.

When configuring in the 9-bit WIDTH mode, connect the DIP[0] port to the appropriate data input and the DIP[1] to a logic zero. Connect DOP[0] to the appropriate data out and leave DOP[1] unconnected. Connect DI[7:0] and DO[7:0] to the appropriate input and output signals and tie DI[15:8] to logic zeros and leave DO[15:8] unconnected.

When configuring in the 18-bit WIDTH mode, all DI, DIP, DO and DOP signals can be connected.

For any configuration, any unused DI or DIP inputs should be tied to a logic zero, and any unused DO or DOP pins should be left unconnected. When the FIFO is set to be synchronous (EN_SYN attribute is set to TRUE), the same clock source must be tied to WRCLK and RDCLK. When in asynchronous mode (EN_SYN is set to FALSE), unique clock signals can be used. Depending on the offset between read and write clock edges, the Empty, Almost Empty, Full and Almost Full flags can deassert one cycle later. Due to the asynchronous nature of the clocks the simulation model only reflects the deassertion latency cycles listed in the architecture user guide.

The FIFO must be RST after power up. The FULL, ALMOSTFULL, EMPTY and ALMOSTEMPTY output flags should be connected to the appropriate destination logic or left unconnected if not used. The WRERR, RDERR, WRCOUNT and RDCOUNT are optional outputs and can be left unconnected if not needed. Set all attributes to the FIFO to enable the desired behavior of the primitive by adjusting the generics (VHDL) or in-line defparams (Verilog) in the instantiation.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
ALMOST_FULL_OFFSET	Hexadecimal	Any 12-Bit Value	All zeros	Specifies the amount of data contents in the RAM to trigger the ALMOST_FULL flag.
ALMOST_EMPTY_OFFSET	Hexadecimal	Any 12-Bit Value	All zeros	Specifies the amount of data contents in the RAM to trigger the ALMOST_EMPTY flag.
FIRST_WORD_FALL_THROUGH	Boolean	TRUE, FALSE	FALSE	If TRUE, the first write to the FIFO will appear on DO without a first RDEN assertion.
DATA_WIDTH	Integer	4, 9, 18	4	Specifies the desired data width for the FIFO.
EN_SYN	Boolean	TRUE, FALSE	FALSE	EN_SYN denotes whether the FIFO is operating in either multirate (two independent clocks) or synchronous (a single clock) mode. Multirate must use DO_REG=1.
DO_REG	Integer	0, 1	1	Data pipeline register for EN_SYN.

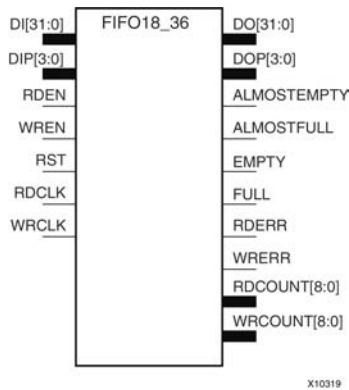
Attribute	Type	Allowed Values	Default	Description
SIM_MODE	String	"SAFE", "FAST" .	"SAFE"	This is a simulation only attribute. It will direct the simulation model to run in performance-oriented mode when set to "FAST." Please see the <i>Synthesis and Simulation Design Guide</i> for more information.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FIFO18_36

Primitive: 36-bit Wide by 512 Deep 18kb FIFO (First In, First Out) Block RAM Memory



Introduction

Virtex®-5 devices contain several block RAM memories that can be configured as FIFOs, automatic error-correction RAM, or general-purpose 36kb or 18kb RAM/ROM memories. These block RAM memories offer fast and flexible storage of large amounts of on-chip data. The FIFO18_36 allows access to the block RAM in the 18kb FIFO configuration when a wide data path is needed. This component is set to a 36-bit wide, 512 deep ration with configurable synchronous or asynchronous operation. This FIFO RAM also supplies all associated FIFO flags and status signals.

When using the dual-clock mode with independent clocks, depending on the offset between read and write clock edges, the Empty, Almost Empty, Full and Almost Full flags can deassert one cycle later. Due to the asynchronous nature of the clocks the simulation model only reflects the deassertion latency cycles listed in the architecture user guide.

Note For an 18kb FIFO in a deeper, less wide configuration, use the FIFO18 component. For deeper or wider configurations of the FIFO, use the FIFO36 or FIFO36_72 components. If you want error-correction circuitry, use FIFO36_72.

Port Descriptions

Port	Direction	Width	Function
DO	Output	32	FIFO data output bus.
DOP	Output	4	FIFO parity data output bus.
FULL	Output	1	Active high logic indicates that the FIFO contents are full.
ALMOSTFULL	Output	1	Programmable flag to indicate the FIFO is almost full. ALMOST_FULL_OFFSET attribute specifies where to trigger this flag.
EMPTY	Output	1	Active high logic indicates the FIFO is currently empty.
ALMOSTEMPTY	Output	1	Programmable flag to indicate the FIFO is almost empty. ALMOST_EMPTY_OFFSET attribute specifies where to trigger this flag.
WRERR, RDERR	Output	1	WRERR indicates that a write occurred while the FIFO was full while RDERR indicated a read occurred while the FIFO was empty
WRCOUNT, RDCOUNT	Output	9	FIFO write/read pointer.

Port	Direction	Width	Function
DI	Input	32	FIFO data input bus.
DIP	Input	4	FIFO parity data input bus.
WREN	Input	1	Active high FIFO write enable.
RDEN	Input	1	Active high FIFO read enable.
RST	Input	1	Asynchronous reset (active high) of all FIFO functions, flags, and pointers. RESET must be asserted for three clock cycles.
WRCLK, RDCLK	Input	1	FIFO read and write clocks (positive edge triggered).

Design Entry Method

This design element can be used in schematics.

DI, DIP, DO and DOP should be connected to their respective input and output data sources. When you are using fewer than 36-bits, connect any unused DI or DIP inputs to a logic zero and any unused DO or DOP pins should be left unconnected. When you are the FIFO set to be synchronous (EN_SYN attribute is set to TRUE), the same clock source should be tied to WRCLK and RDCLK. When you are in asynchronous mode (EN_SYN is set to FALSE), unique clock signals should be used. Depending on the offset between read and write clock edges, the Empty, Almost Empty, Full and Almost Full flags can deassert one cycle later. Due to the asynchronous nature of the clocks the simulation model only reflects the deassertion latency cycles listed in the architecture user guide. WREN and RDEN should be connected to the respective write enable and read enable signal/ logic. RST should be either tied to the appropriate reset signal/logic, or connected to a logic zero if unused.

The FULL, ALMOSTFULL, EMPTY and ALMOSTEMPTY output flags should be connected to the appropriate destination logic, or left unconnected, if not used. The WRERR, RDERR, WRCOUNT and RDCOUNT are optional outputs that can be left unconnected, if not needed. Set all attributes to the FIFO to enable the desired behavior of the component by adjusting the generics (VHDL) or in-line defparams (Verilog) in the instantiation code.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
ALMOST_FULL_OFFSET	Hexadecimal	Any 9-Bit Value	All zeros	Specifies the amount of data contents in the RAM to trigger the ALMOST_FULL flag.
ALMOST_EMPTY_OFFSET	Hexadecimal	Any 9-Bit Value	All zeros	Specifies the amount of data contents in the RAM to trigger the ALMOST_EMPTY flag.
FIRST_WORD_FALL_THROUGH	Boolean	TRUE, FALSE	FALSE	If TRUE, the first write to the FIFO will appear on DO without an RDEN assertion.
EN_SYN	Boolean	TRUE, FALSE	FALSE	When FALSE, specifies the FIFO to be used in asynchronous mode (two independent clock) or when TRUE in synchronous (a single clock) operation.
DO_REG	Integer	0, 1	1	Enable output register to the FIFO for improved clock-to-out timing at the expense of added read latency (one pipeline delay). DO_REG must be 1 when EN_SYN is set to FALSE.
SIM_MODE	String	"SAFE", "FAST"	"SAFE"	This is a simulation only attribute. It will direct the simulation model to run in performance-oriented mode when set to "FAST." Please see the <i>Synthesis</i>

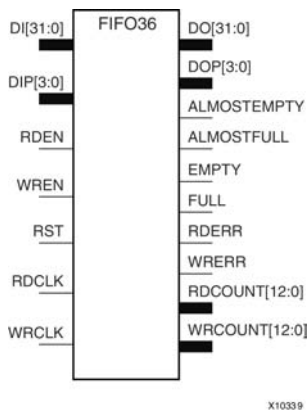
Attribute	Type	Allowed Values	Default	Description
				<i>and Simulation Design Guide</i> for more information.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FIFO36

Primitive: 36kb FIFO (First In, First Out) Block RAM Memory



Introduction

Virtex®-5 and above devices contain several block RAM memories that can be configured as FIFOs, automatic error-correction RAM, or general-purpose 36kb or 18kb RAM/ROM memories. These block RAM memories offer fast and flexible storage of large amounts of on-chip data. The FIFO36 allows access to the block RAM in the 36kb FIFO configurations. This component can be configured and used as a 4-bit wide by 8K deep, 9-bit by 4K deep, 18-bit by 2K deep or a 36-bit wide by 1K deep synchronous or multirate (asynchronous) FIFO RAM with all associated FIFO flags.

When using the dual-clock mode with independent clocks, depending on the offset between read and write clock edges, the Empty, Almost Empty, Full and Almost Full flags can deassert one cycle later. Due to the asynchronous nature of the clocks the simulation model only reflects the deassertion latency cycles listed in the architecture user guide.

Note For a 72-bit wide by 512 deep use the FIFO, the FIFO36_72 component. For smaller configurations of the FIFO, use the FIFO18 or FIFO18_36. If error-correction circuitry is desired, use the FIFO36_72.

Port Descriptions

Port	Direction	Width	Function
DO	Output	4, 8, 16, 32	FIFO data output bus.
DOP	Output	0, 1, 2, 4	FIFO parity data output bus.
FULL	Output	1	Active high logic indicates that the FIFO contents are full.
ALMOSTFULL	Output	1	Programmable flag to indicate that the FIFO is almost full. The ALMOST_FULL_OFFSET attribute specifies the threshold where this flag is triggered relative to full/empty.
EMPTY	Output	1	Active high logic indicates that the FIFO is currently empty.
ALMOSTEMPTY	Output	1	Programmable flag to indicate the FIFO is almost empty. ALMOST_EMPTY_OFFSET attribute specifies the threshold where this flag is triggered relative to full/empty.
WRERR, RDERR	Output	1	WRERR indicates that a write occurred while the FIFO was full and RDERR indicates that a read occurred while the FIFO was empty.

Port	Direction	Width	Function
WRCOUNT, RDCOUNT	Output	13	FIFO write/read pointer.
DI	Input	4, 8, 16, 32	FIFO data input bus.
DIP	Input	0, 1, 2, 4	FIFO parity data bus.
WREN	Input	1	Active high FIFO write enable.
RDEN	Input	1	Active high FIFO read enable.
RST	Input	1	Asynchronous reset (active high) of all FIFO functions, flags, and pointers. RESET must be asserted for three clock cycles.
WRCLK, RDCLK	Input	1	FIFO read and write clocks (positive edge triggered).

Design Entry Method

This design element can be used in schematics.

When you are instantiating the primitive configured in the 4-bit WIDTH mode, connect the DIP port to logic zeros and leave the DOP port unconnected. Connect DI[3:0] and DO[3:0] to the appropriate input and output signals and tie DI[31:4] to logic zeros and leave DO[31:4] unconnected.

When you are configuring in the 9-bit WIDTH mode, connect the DIP[0] port to the appropriate data input and the DIP[3:1] to a logic zero. Connect DOP[0] to the appropriate data out and leave DOP[3:1] unconnected. Connect DI[7:0] and DO[7:0] to the appropriate input and output signals and tie DI[31:8] to logic zeros and leave DO[31:8] unconnected.

When you are configuring in the 18-bit WIDTH mode, connect the DIP[1:0] port to the appropriate data input and the DIP[3:2] to a logic zero. Connect DOP[1:0] to the appropriate data out and leave DOP[3:2] unconnected. Connect DI[15:0] and DO[15:0] to the appropriate input and output signals and tie DI[31:16] to logic zeros and leave DO[31:16] unconnected.

When you are configuring in the 36-bit WIDTH mode, all DI, DIP, DO and DOP signals can be connected.

For any configuration, any unused DI or DIP inputs should be tied to a logic zero and any unused DO or DOP pins should be left unconnected. When the FIFO is set to be synchronous (EN_SYN attribute is set to TRUE), the same clock source should be tied to WRCLK and RDCLK.

When you are in asynchronous mode (EN_SYN is set to FALSE), unique clock signals should be used. Depending on the offset between read and write clock edges, the Empty, Almost Empty, Full and Almost Full flags can deassert one cycle later. Due to the asynchronous nature of the clocks the simulation model only reflects the deassertion latency cycles listed in the architecture user guide. WREN and RDEN should be connected to the respective write enable and read enable signal/ logic. RST should be either tied to the appropriate reset signal/logic or connected to a logic zero if unused. The FULL, ALMOSTFULL, EMPTY and ALMOSTEMPTY output flags should be connected to the appropriate destination logic or left unconnected if not used. The WRERR, RDERR, WRCOUNT and RDCOUNT are optional outputs and can be left unconnected if not needed. Set all attributes to the FIFO to enable the desired behavior of the component by adjusting the generics (VHDL) or in-line defparams (Verilog) in the instantiation code.

Available Attributes

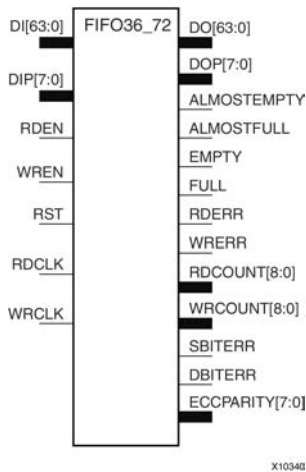
Attribute	Type	Allowed Values	Default	Description
ALMOST_FULL_OFFSET	Hexadecimal	Any 13-Bit Value	All zeros	Specifies the amount of data contents in the RAM to trigger the ALMOST_FULL flag.
ALMOST_EMPTY_OFFSET	Hexadecimal	Any 13-Bit Value	All zeros	Specifies the amount of data contents in the RAM to trigger the ALMOST_EMPTY flag.
FIRST_WORD_FALL_THROUGH	Boolean	TRUE, FALSE	FALSE	If TRUE, the first write to the FIFO will appear on DO without an RDEN assertion.
DATA_WIDTH	Integer	4 to 36	4	Specifies the desired data width for the FIFO.
EN_SYN	Boolean	TRUE, FALSE	FALSE	EN_SYN denotes whether the FIFO is operating in either multirate (two independent clocks) or synchronous (a single clock) mode. Multirate must use DO_REG=1.
DO_REG	Integer	0, 1	1	Data pipeline register for EN_SYN.
SIM_MODE	String	"SAFE", "FAST" .	"SAFE"	This is a simulation only attribute. It will direct the simulation model to run in performance-oriented mode when set to "FAST." Please see the <i>Synthesis and Simulation Design Guide</i> for more information.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FIFO36_72

Primitive: 72-Bit Wide by 512 Deep 36kb FIFO (First In, First Out) Block RAM Memory with ECC (Error Detection and Correction Circuitry)



Introduction

Virtex®-5 devices contain several block RAM memories that can be configured as FIFOs, automatic error-correction RAM, or general-purpose 36kb or 18kb RAM/ROM memories. These Block RAM memories offer fast and flexible storage of large amounts of on-chip data. This element allows access to the Block RAM in the 36kB FIFO configuration when a wide data path is needed. This component is set to a 72-bit wide, 512 deep ration, with configurable synchronous or asynchronous operation. Error detection and correction circuitry can also be enabled to uncover and rectify possible memory corruptions. This FIFO RAM also supplies all associated FIFO flags and status signals.

When using the dual-clock mode with independent clocks, depending on the offset between read and write clock edges, the Empty, Almost Empty, Full and Almost Full flags can deassert one cycle later. Due to the asynchronous nature of the clocks the simulation model only reflects the deassertion latency cycles listed in the architecture user guide.

Note For a 36kb FIFO in a deeper, less wide configuration, use the FIFO36 component. For smaller configurations of the FIFO, use the FIFO18 or FIFO18_36.

Port Descriptions

Port	Direction	Width	Function
DO	Output	64	FIFO data output bus.
DOP	Output	8	FIFO parity data output bus.
FULL	Output	1	Active high logic indicates that the FIFO contents are full.
ALMOSTFULL	Output	1	Programmable flag to indicate the FIFO is almost full. ALMOST_FULL_OFFSET attribute specifies where to trigger this flag.
EMPTY	Output	1	Active high logic indicates the FIFO is currently empty.
ALMOSTEMPTY	Output	1	Programmable flag to indicate the FIFO is almost empty. ALMOST_EMPTY_OFFSET attribute specifies where to trigger this flag.

Port	Direction	Width	Function
WRERR, RDERR	Output	1	WRERR indicates that a write occurred while the FIFO was full while RDERR indicated a read occurred while the FIFO was empty.
WRCOUNT, RDCOUNT	Output	9	FIFO write/read pointer.
SBITTERR	Output	1	Status output from ECC function to indicate a single bit error was detected. EN_ECC_READ needs to be TRUE in order to use this functionality.
DBITTERR	Output	1	Status output from ECC function to indicate a double bit error was detected. EN_ECC_READ needs to be TRUE in order to use this functionality.
ECCPARITY	Output	8	8-bit data generated by the ECC encoder used by the ECC decoder for memory error detection and correction.
DI	Input	64	FIFO data input bus.
DIP	Input	8	FIFO parity data input bus.
WREN	Input	1	Active high FIFO write enable.
RDEN	Input	1	Active high FIFO read enable.
RST	Input	1	Asynchronous reset (active high) of all FIFO functions, flags, and pointers. RESET must be asserted for three clock cycles.
WRCLK, RDCLK	Input	1	FIFO read and write clocks (positive edge triggered).

Design Entry Method

This design element can be used in schematics.

DI, DIP, DO and DOP should be connected to their respective input and output data sources unless the FIFO is operating in ECC mode in which only the DI and DO ports should be used, since the parity bits are necessary for the ECC functionality. When you are using fewer than available data bits, connect any unused DI or DIP inputs to a logic zero and any unused DO or DOP pins should be left unconnected. When the FIFO is set to be synchronous (EN_SYN attribute is set to TRUE), the same clock source should be tied to WRCLK and RDCLK.

When you are in asynchronous mode (EN_SYN is set to FALSE), unique clock signals should be used. Depending on the offset between read and write clock edges, the Empty, Almost Empty, Full, and Almost Full flags can deassert one cycle later. Due to the asynchronous nature of the clocks the simulation model only reflects the deassertion latency cycles listed in the architecture user guide. WREN and RDEN should be connected to the respective write enable and read enable signal/logic. RST should be either tied to the appropriate reset signal/logic or connected to a logic zero if unused.

The FULL, ALMOSTFULL, EMPTY and ALMOSTEMPTY output flags should be connected to the appropriate destination logic or left unconnected if not used. The WRERR, RDERR, WRCOUNT and RDCOUNT are optional outputs and can be left unconnected, if not needed. In order to use the ECC function, the EN_ECC_READ and the EN_ECC_WRITE must be set to TRUE. If you want to monitor the error detection circuit operation, connect the SBITTERR, DBITTERR and the ECCPARITY signals to the appropriate logic. Set all attributes to the FIFO to enable the desired behavior in the component by adjusting the generics (VHDL) or in-line defparams (Verilog) in the instantiation.

Available Attributes

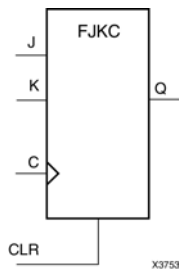
Attribute	Type	Allowed Values	Default	Description
ALMOST_FULL_OFFSET	Hexadecimal	Any 9-Bit Value	080	Specifies the amount of data contents in the RAM to trigger the ALMOST_FULL flag.
ALMOST_EMPTY_OFFSET	Hexadecimal	Any 9-Bit Value	080	Specifies the amount of data contents in the RAM to trigger the ALMOST_EMPTY flag.
FIRST_WORD_FALL_THROUGH	Boolean	TRUE, FALSE	FALSE	If TRUE, the first write to the FIFO will appear on DO without an RDEN assertion.
EN_SYN	Boolean	TRUE, FALSE	FALSE	When FALSE, specifies the FIFO to be used in asynchronous mode (two independent clock) or when TRUE in synchronous (a single clock) operation.
DO_REG	Integer	0, 1	1	Enable output register to the FIFO for improved clock-to-out timing at the expense of added read latency (one pipeline delay). DO_REG must be 1 when EN_SYN is set to FALSE.
EN_ECC_READ	Boolean	TRUE, FALSE	FALSE	Enable the ECC decoder circuitry.
EN_ECC_WRITE	Boolean	TRUE, FALSE	FALSE	Enable the ECC encoder circuitry.
SIM_MODE	String	"SAFE", "FAST"	"SAFE"	This is a simulation only attribute. It will direct the simulation model to run in performance-oriented mode when set to "FAST." Please see the <i>Synthesis and Simulation Design Guide</i> for more information.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FJKC

Macro: J-K Flip-Flop with Asynchronous Clear



Introduction

This design element is a single J-K-type flip-flop with J, K, and asynchronous clear (CLR) inputs and data output (Q). The asynchronous clear (CLR) input, when High, overrides all other inputs and resets the Q output Low. When CLR is Low, the output responds to the state of the J and K inputs, as shown in the following logic table, during the Low-to-High clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs
CLR	J	K	C	Q
1	X	X	X	0
0	0	0	↑	No Change
0	0	1	↑	0
0	1	0	↑	1
0	1	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

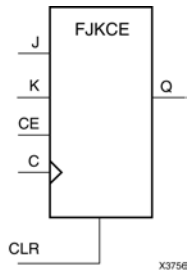
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FJKCE

Macro: J-K Flip-Flop with Clock Enable and Asynchronous Clear



Introduction

This design element is a single J-K-type flip-flop with J, K, clock enable (CE), and asynchronous clear (CLR) inputs and data output (Q). The asynchronous clear (CLR), when High, overrides all other inputs and resets the Q output Low. When CLR is Low and CE is High, Q responds to the state of the J and K inputs, as shown in the following logic table, during the Low-to-High clock transition. When CE is Low, the clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs					Outputs
CLR	CE	J	K	C	Q
1	X	X	X	X	0
0	0	X	X	X	No Change
0	1	0	0	X	No Change
0	1	0	1	↑	0
0	1	1	0	↑	1
0	1	1	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

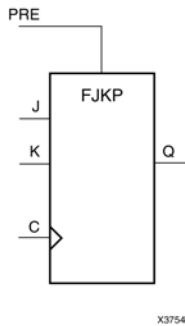
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FJKP

Macro: J-K Flip-Flop with Asynchronous Preset



Introduction

This design element is a single J-K-type flip-flop with J, K, and asynchronous preset (PRE) inputs and data output (Q). The asynchronous preset (PRE) input, when High, overrides all other inputs and sets the (Q) output High. When (PRE) is Low, the (Q) output responds to the state of the J and K inputs, as shown in the following logic table, during the Low-to-High clock transition.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs
PRE	J	K	C	Q
1	X	X	X	1
0	0	0	X	No Change
0	0	1	↑	0
0	1	0	↑	1
0	1	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

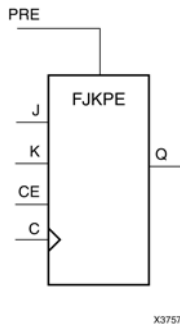
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FJKPE

Macro: J-K Flip-Flop with Clock Enable and Asynchronous Preset



Introduction

This design element is a single J-K-type flip-flop with J, K, clock enable (CE), and asynchronous preset (PRE) inputs and data output (Q). The asynchronous preset (PRE), when High, overrides all other inputs and sets the (Q) output High. When (PRE) is Low and (CE) is High, the (Q) output responds to the state of the J and K inputs, as shown in the logic table, during the Low-to-High clock (C) transition. When (CE) is Low, clock transitions are ignored.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs					Outputs
PRE	CE	J	K	C	Q
1	X	X	X	X	1
0	0	X	X	X	No Change
0	1	0	0	X	No Change
0	1	0	1	↑	0
0	1	1	0	↑	1
0	1	1	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

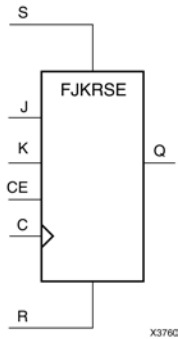
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FJKRSE

Macro: J-K Flip-Flop with Clock Enable and Synchronous Reset and Set



Introduction

This design element is a single J-K-type flip-flop with J, K, synchronous reset (R), synchronous set (S), and clock enable (CE) inputs and data output (Q). When synchronous reset (R) is High during the Low-to-High clock (C) transition, all other inputs are ignored and output (Q) is reset Low. When synchronous set (S) is High and (R) is Low, output (Q) is set High. When (R) and (S) are Low and (CE) is High, output (Q) responds to the state of the J and K inputs, according to the following logic table, during the Low-to-High clock (C) transition. When (CE) is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs						Outputs
R	S	CE	J	K	C	Q
1	X	X	X	X	↑	0
0	1	X	X	X	↑	1
0	0	0	X	X	X	No Change
0	0	1	0	0	X	No Change
0	0	1	0	1	↑	0
0	0	1	1	0	↑	1
0	0	1	1	0	↑	1
0	0	1	1	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

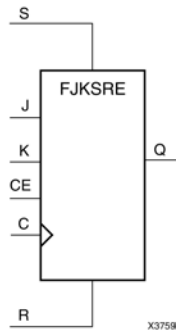
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FJKSRE

Macro: J-K Flip-Flop with Clock Enable and Synchronous Set and Reset



Introduction

This design element is a single J-K-type flip-flop with J, K, synchronous set (S), synchronous reset (R), and clock enable (CE) inputs and data output (Q). When synchronous set (S) is High during the Low-to-High clock (C) transition, all other inputs are ignored and output (Q) is set High. When synchronous reset (R) is High and (S) is Low, output (Q) is reset Low. When (S) and (R) are Low and (CE) is High, output (Q) responds to the state of the J and K inputs, as shown in the following logic table, during the Low-to-High clock (C) transition. When (CE) is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs						Outputs
S	R	CE	J	K	C	Q
1	X	X	X	X	↑	1
0	1	X	X	X	↑	0
0	0	0	X	X	X	No Change
0	0	1	0	0	X	No Change
0	0	1	0	1	↑	0
0	0	1	1	0	↑	1
0	0	1	1	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

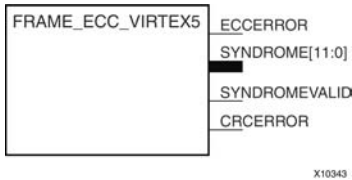
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FRAME_ECC_VIRTEX5

Primitive: Virtex®-5 Configuration Frame Error Detection and Correction Circuitry



Introduction

This design element enables the dedicated, built-in ECC (Error Detection and Correction Circuitry) for the configuration memory of the FPGA. This element contains outputs that allow monitoring of the status of the ECC circuitry and the status of the readback CRC circuitry.

Port Descriptions

Port	Direction	Width	Function
ECCERROR	Output	1	Frame ECC error found. Value is a one when SYNDROME is non-zero and a zero when SYNDROME is all zeroes indicating no errors detected.
SYNDROME	Output	12	Frame ECC error where: <ul style="list-style-type: none"> No errors: All zeros. One bit error: SYNDROME[11]=0, SYNDROME[10:0]= location of error in FRAME. Two bit errors: SYNDROME[11]=1, SYNDROME[10:0]=don't care. More than two bit errors: Unknown output.
SYNDROMEVALID	Output	1	Frame ECC output indicating that the value on SYNDROME is valid.
CRCERROR	Output	1	Readback CRC error.

Design Entry Method

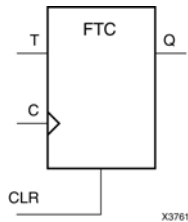
This design element can be used in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FTC

Macro: Toggle Flip-Flop with Asynchronous Clear



Introduction

This design element is a synchronous, resettable toggle flip-flop. The asynchronous clear (CLR) input, when High, overrides all other inputs and resets the data output (Q) Low. The (Q) output toggles, or changes state, when the toggle enable (T) input is High and (CLR) is Low during the Low-to-High clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs
CLR	T	C	Q
1	X	X	0
0	0	X	No Change
0	1	↑	Toggle

Design Entry Method

You can instantiate this element when targeting a CPLD, but not when you are targeting an FPGA.

Available Attributes

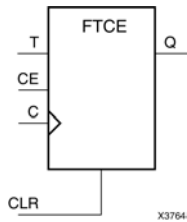
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FTCE

Macro: Toggle Flip-Flop with Clock Enable and Asynchronous Clear



Introduction

This design element is a toggle flip-flop with toggle and clock enable and asynchronous clear. When the asynchronous clear (CLR) input is High, all other inputs are ignored and the data output (Q) is reset Low. When CLR is Low and toggle enable (T) and clock enable (CE) are High, Q output toggles, or changes state, during the Low-to-High clock (C) transition. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs
CLR	CE	T	C	Q
1	X	X	X	0
0	0	X	X	No Change
0	1	0	X	No Change
0	1	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

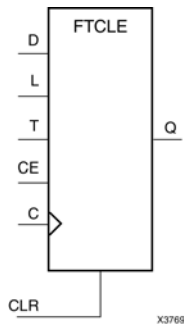
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FTCLE

Macro: Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Clear



Introduction

This design element is a toggle/loadable flip-flop with toggle and clock enable and asynchronous clear. When the asynchronous clear input (CLR) is High, all other inputs are ignored and output Q is reset Low. When load enable input (L) is High and CLR is Low, clock enable (CE) is overridden and the data on data input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition. When toggle enable (T) and CE are High and L and CLR are Low, output Q toggles, or changes state, during the Low- to-High clock transition. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs						Outputs
CLR	L	CE	T	D	C	Q
1	X	X	X	X	X	0
0	1	X	X	D	↑	D
0	0	0	X	X	X	No Change
0	0	1	0	X	X	No Change
0	0	1	1	X	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

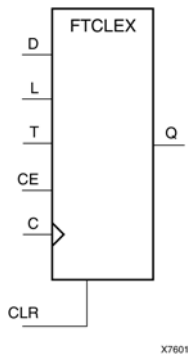
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FTCLEX

Macro: Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Clear



Introduction

This design element is a toggle/loadable flip-flop with toggle and clock enable and asynchronous clear. When the asynchronous clear input (CLR) is High, all other inputs are ignored and output Q is reset Low. When load enable input (L) is High, CLR is Low, and CE is High, the data on data input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition. When toggle enable (T) and CE are High and L and CLR are Low, output Q toggles, or changes state, during the Low- to-High clock transition. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs						Outputs
CLR	L	CE	T	D	C	Q
1	X	X	X	X	X	0
0	1	X	X	D	↑	D
0	0	0	X	X	X	No Change
0	0	1	0	X	X	No Change
0	0	1	1	X	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

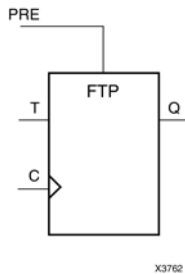
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FTP

Macro: Toggle Flip-Flop with Asynchronous Preset



Introduction

This design element is a toggle flip-flop with toggle enable and asynchronous preset. When the asynchronous preset (PRE) input is High, all other inputs are ignored and output (Q) is set High. When toggle-enable input (T) is High and (PRE) is Low, output (Q) toggles, or changes state, during the Low-to-High clock (C) transition.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
PRE	T	C	Q
1	X	X	1
0	0	X	No Change
0	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

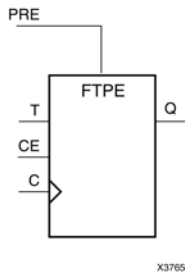
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FTPE

Macro: Toggle Flip-Flop with Clock Enable and Asynchronous Preset



Introduction

This design element is a toggle flip-flop with toggle and clock enable and asynchronous preset. When the asynchronous preset (PRE) input is High, all other inputs are ignored and output (Q) is set High. When the toggle enable input (T) is High, clock enable (CE) is High, and (PRE) is Low, output (Q) toggles, or changes state, during the Low-to-High clock transition. When (CE) is Low, clock transitions are ignored.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs
PRE	CE	T	C	Q
1	X	X	X	1
0	0	X	X	No Change
0	1	0	X	No Change
0	1	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

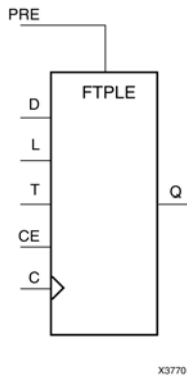
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FTPLE

Macro: Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Preset



Introduction

This design element is a toggle/loadable flip-flop with toggle and clock enable and asynchronous preset. When the asynchronous preset input (PRE) is High, all other inputs are ignored and output (Q) is set High. When the load enable input (L) is High and (PRE) is Low, the clock enable (CE) is overridden and the data (D) is loaded into the flip-flop during the Low-to-High clock transition. When L and PRE are Low and toggle-enable input (T) and (CE) are High, output (Q) toggles, or changes state, during the Low-to-High clock transition. When (CE) is Low, clock transitions are ignored.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs						Outputs
PRE	L	CE	T	D	C	Q
1	X	X	X	X	X	1
0	1	X	X	D	↑	D
0	0	0	X	X	X	No Change
0	0	1	0	X	X	No Change
0	0	1	1	X	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

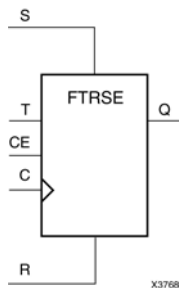
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FTRSE

Macro: Toggle Flip-Flop with Clock Enable and Synchronous Reset and Set



Introduction

This design element is a toggle flip-flop with toggle and clock enable and synchronous reset and set. When the synchronous reset input (R) is High, it overrides all other inputs and the data output (Q) is reset Low. When the synchronous set input (S) is High and (R) is Low, clock enable input (CE) is overridden and output (Q) is set High. (Reset has precedence over Set.) When toggle enable input (T) and (CE) are High and (R) and (S) are Low, output (Q) toggles, or changes state, during the Low-to-High clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs					Outputs
R	S	CE	T	C	Q
1	X	X	X	↑	0
0	1	X	X	↑	1
0	0	0	X	X	No Change
0	0	1	0	X	No Change
0	0	1	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

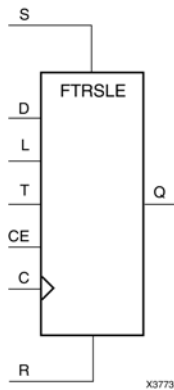
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FTRSLE

Macro: Toggle/Loadable Flip-Flop with Clock Enable and Synchronous Reset and Set



Introduction

This design element is a toggle/loadable flip-flop with toggle and clock enable and synchronous reset and set. The synchronous reset input (R), when High, overrides all other inputs and resets the data output (Q) Low. (Reset has precedence over Set.) When R is Low and synchronous set input (S) is High, the clock enable input (CE) is overridden and output Q is set High. When R and S are Low and load enable input (L) is High, CE is overridden and data on data input (D) is loaded into the flip-flop during the Low-to-High clock transition. When R, S, and L are Low, CE is High and T is High, output Q toggles, or changes state, during the Low-to-High clock transition. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs							Outputs
R	S	L	CE	T	D	C	Q
1	0	X	X	X	X	↑	0
0	1	X	X	X	X	↑	1
0	0	1	X	X	1	↑	1
0	0	1	X	X	0	↑	0
0	0	0	0	X	X	X	No Change
0	0	0	1	0	X	X	No Change
0	0	0	1	1	X	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

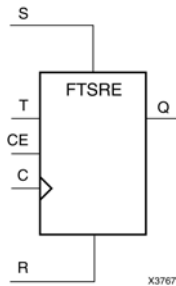
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FTSRE

Macro: Toggle Flip-Flop with Clock Enable and Synchronous Set and Reset



Introduction

This design element is a toggle flip-flop with toggle and clock enable and synchronous set and reset. The synchronous set input, when High, overrides all other inputs and sets data output (Q) High. (Set has precedence over Reset.) When synchronous reset input (R) is High and S is Low, clock enable input (CE) is overridden and output Q is reset Low. When toggle enable input (T) and CE are High and S and R are Low, output Q toggles, or changes state, during the Low-to-High clock transition. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs					Outputs
S	R	CE	T	C	Q
1	X	X	X	↑	1
0	1	X	X	↑	0
0	0	0	X	X	No Change
0	0	1	0	X	No Change
0	0	1	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

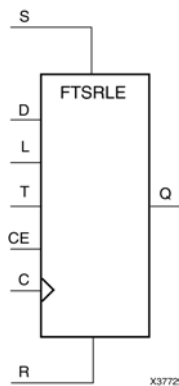
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

FTSRLE

Macro: Toggle/Loadable Flip-Flop with Clock Enable and Synchronous Set and Reset



Introduction

This design element is a toggle/loadable flip-flop with toggle and clock enable and synchronous set and reset. The synchronous set input (S), when High, overrides all other inputs and sets data output (Q) High. (Set has precedence over Reset.) When synchronous reset (R) is High and (S) is Low, clock enable input (CE) is overridden and output (Q) is reset Low. When load enable input (L) is High and S and R are Low, CE is overridden and data on data input (D) is loaded into the flip-flop during the Low-to-High clock transition. When the toggle enable input (T) and (CE) are High and (S), (R), and (L) are Low, output (Q) toggles, or changes state, during the Low-to-High clock transition. When (CE) is Low, clock transitions are ignored.

For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs							Outputs
S	R	L	CE	T	D	C	Q
1	X	X	X	X	X	↑	1
0	1	X	X	X	X	↑	0
0	0	1	X	X	1	↑	1
0	0	1	X	X	0	↑	0
0	0	0	0	X	X	X	No Change
0	0	0	1	0	X	X	No Change
0	0	0	1	1	X	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

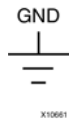
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

GND

Primitive: Ground-Connection Signal Tag



Introduction

The GND signal tag, or parameter, forces a net or input function to a Low logic level. A net tied to GND cannot have any other source.

When the logic-trimming software or fitter encounters a net or input function tied to GND, it removes any logic that is disabled by the GND signal. The GND signal is only implemented when the disabled logic cannot be removed.

Design Entry Method

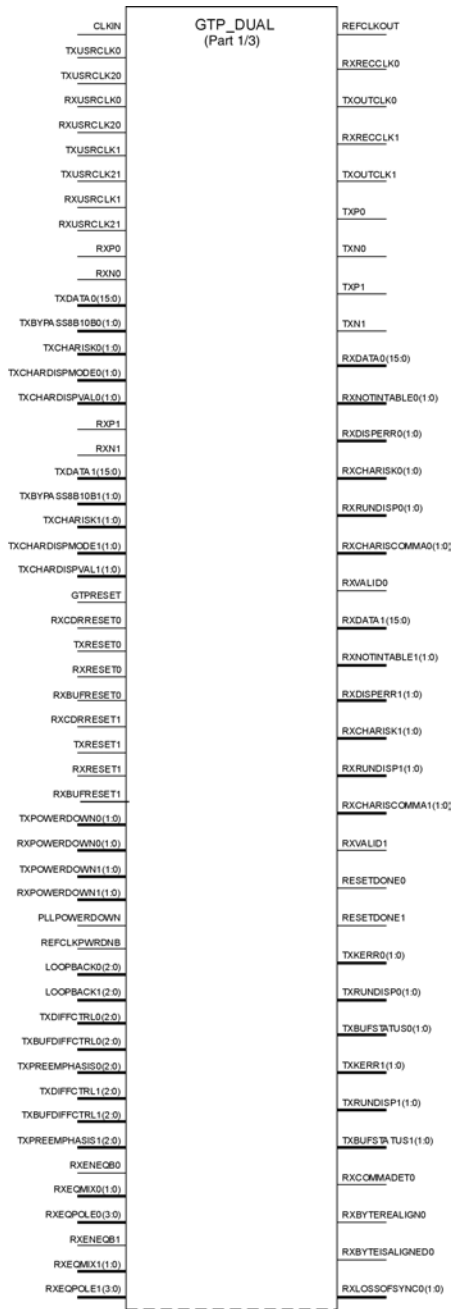
This design element is only for use in schematics.

For More Information

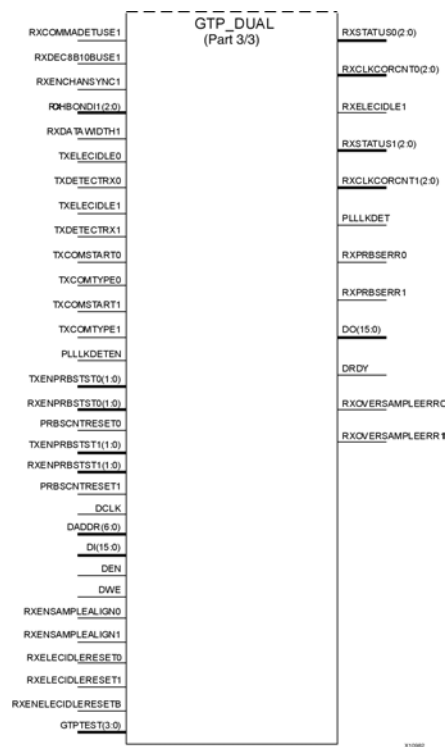
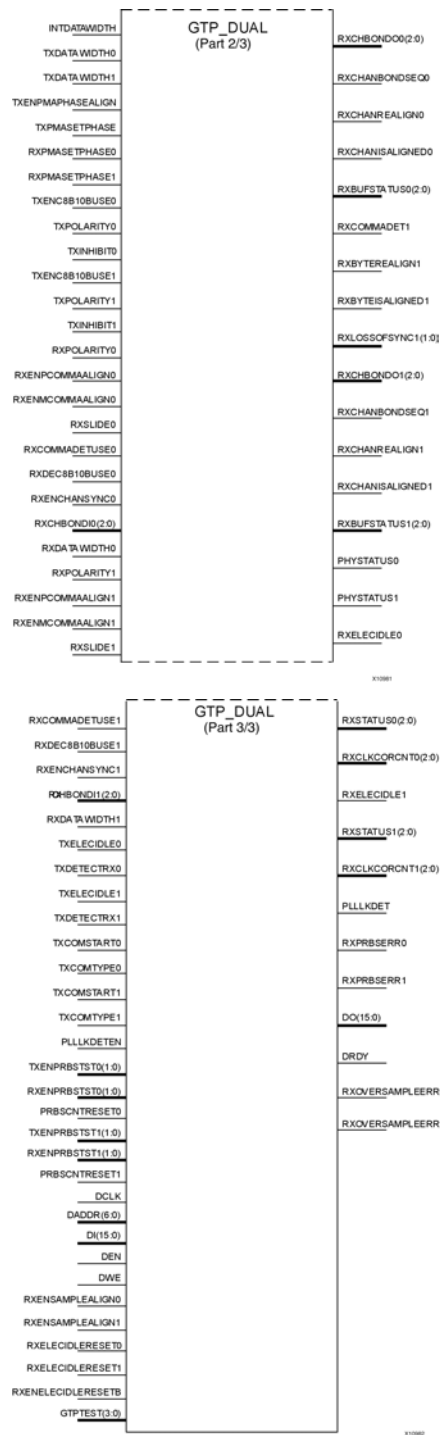
- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

GTP_DUAL

Primitive: Dual Gigabit Transceiver



X10080



Introduction

This design element is a power-efficient transceiver for Virtex®-5 FPGAs. The GTP transceiver is highly configurable and tightly integrated with the programmable logic resources of the FPGA.

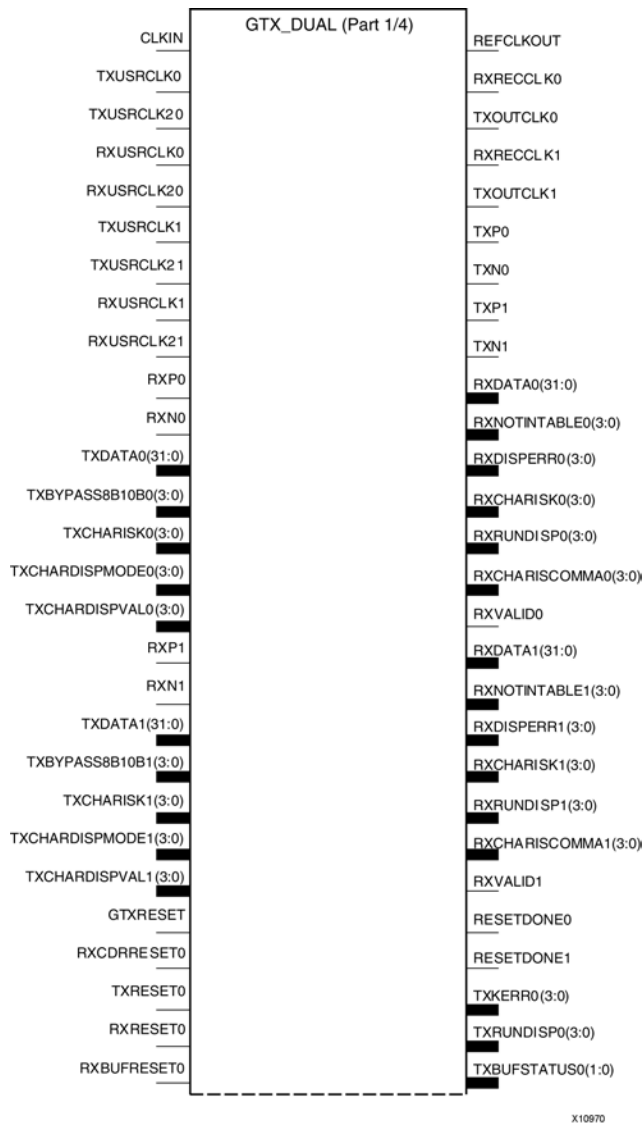
Design Entry Method

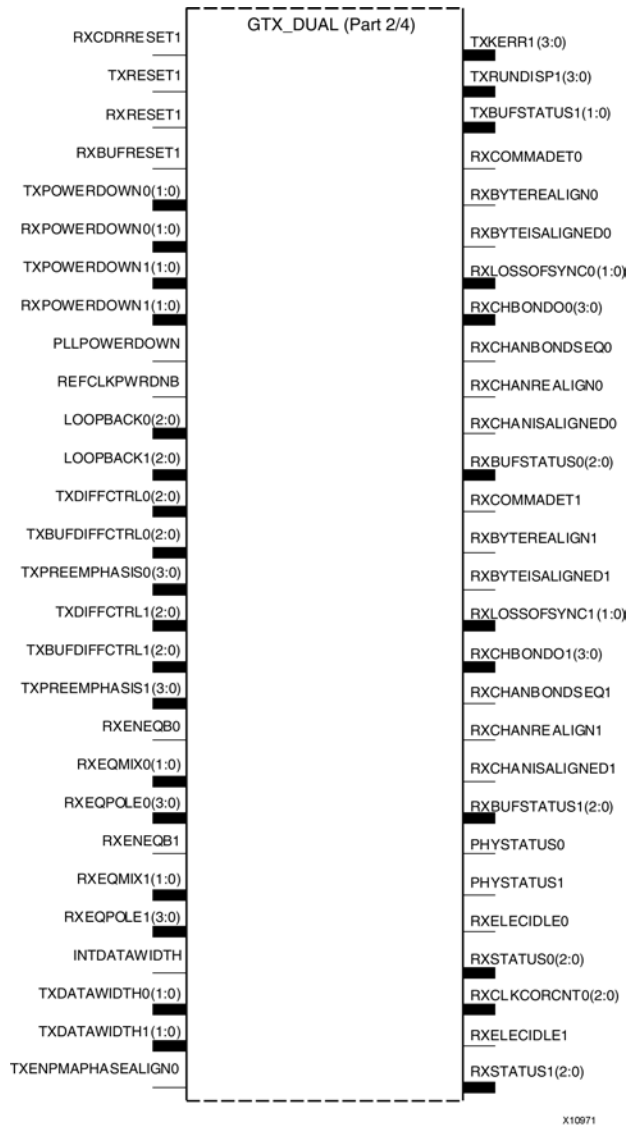
For More Information

-
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).
- See the [Virtex-5 FPGA User Guide](#).

GTX_DUAL

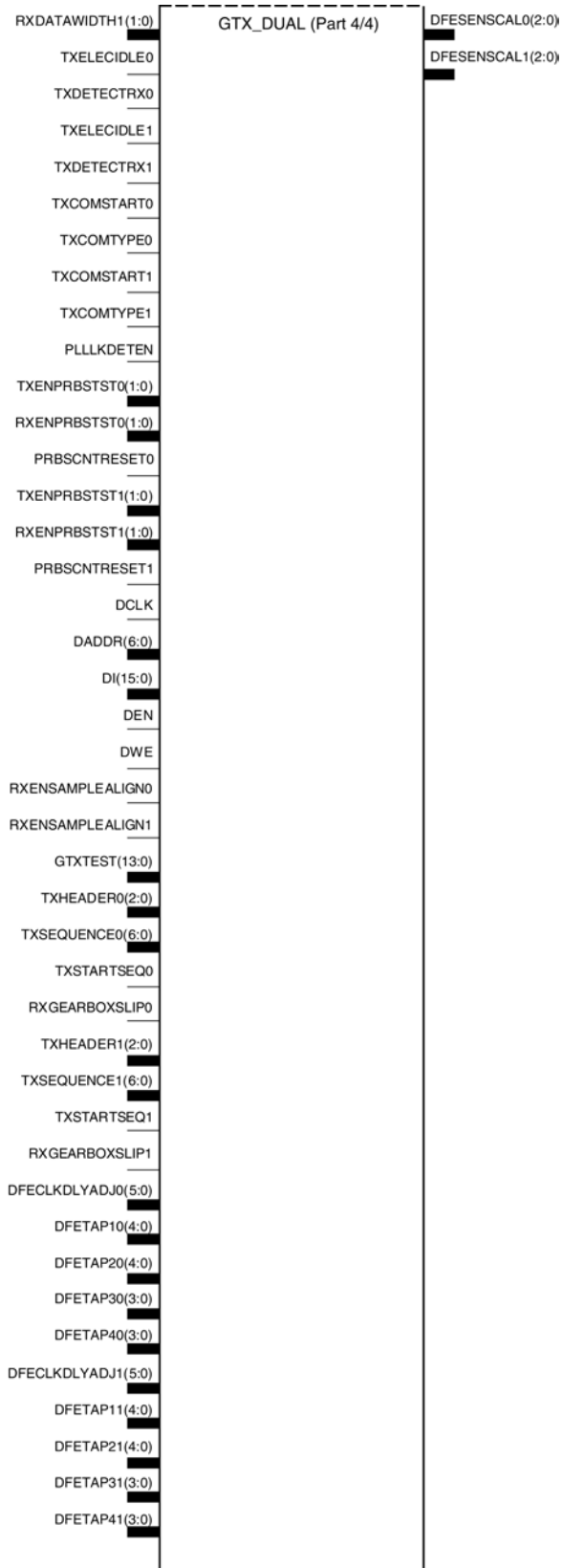
Primitive: Dual Gigabit Transceiver





GTX_DUAL (Part 3/4)		
TXPMASETPHASE0		RXCLKCORCNT1(2:0)
RXENPMAPHASEALIGN0		PLLLKDET
RXPMASETPHASE0		RXPRBSERR0
TXENPMAPHASEALIGN1		RXPRBSERR1
TXPMASETPHASE1		DO(15:0)
RXENPMAPHASEALIGN1		DRDY
RXPMASETPHASE1		RXOVERSAMPLEERR0
TXENC8B10BUSE0		RXOVERSAMPLEERR1
TXPOLARITY0		TXGEARBOXREADY0
TXINHIBIT0		RXHEADER0(2:0)
TXENC8B10BUSE1		RXHEADERVALID0
TXPOLARITY1		RXDATAVALID0
TXINHIBIT1		RXSTARTOFSEQ0
RXPOLARITY0		TXGEARBOXREADY1
RXENPCOMMAALIGN0		RXHEADER1(2:0)
RXENMCOMMAALIGN0		RXHEADERVALID1
RXSLIDE0		RXDATAVALID1
RXCOMMADETUSE0		RXSTARTOFSEQ1
RXDEC8B10BUSE0		DFECLKDLYADJMONITOR0(5:0)
RXENCHANSYNC0		DFEYEDACMONITOR0(4:0)
RXCHBOND0(3:0)		DFETAP1MONITOR0(4:0)
RXDATAWIDTH0(1:0)		DFETAP2MONITOR0(4:0)
RXPOLARITY1		DFETAP3MONITOR0(3:0)
RXENPCOMMAALIGN1		DFETAP4MONITOR0(3:0)
RXENMCOMMAALIGN1		DFECLKDLYADJMONITOR1(5:0)
RXSLIDE1		DFEYEDACMONITOR1(4:0)
RXCOMMADETUSE1		DFETAP1MONITOR1(4:0)
RXDEC8B10BUSE1		DFETAP2MONITOR1(4:0)
RXENCHANSYNC1		DFETAP3MONITOR1(3:0)
RXCHBOND1(3:0)		DFETAP4MONITOR1(3:0)

X10972



X10973

Introduction

This design element is a power-efficient transceiver for Virtex®-5 FPGAs. The GTX transceiver is highly configurable and tightly integrated with the programmable logic resources of the FPGA.

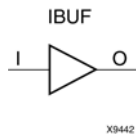
Design Entry Method

For More Information

- See the [Virtex-5 FPGA RocketIO GTX Transceivers User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).
- See the [Virtex-5 FPGA User Guide](#).

IBUF

Primitive: Input Buffer



Introduction

This design element is automatically inserted (inferred) by the synthesis tool to any signal directly connected to a top-level input or in-out port of the design. You should generally let the synthesis tool infer this buffer. However, it can be instantiated into the design if required. In order to do so, connect the input port (I) directly to the associated top-level input or in-out port, and connect the output port (O) to the logic sourced by that port. Modify any necessary generic maps (VHDL) or named parameter value assignment (Verilog) in order to change the default behavior of the component.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Buffer output
I	Input	1	Buffer input

Design Entry Method

This design element can be used in schematics.

In general, this element is inferred by the synthesis tool for any specified top-level input port to the design. It is generally not necessary to specify them in the source code. However, if desired, they be manually instantiated by either copying the instantiation code from the appropriate Libraries Guide HDL template and pasting it into the top-level entity/module of your code. It is recommended to always put all I/O components on the top-level of the design to help facilitate hierarchical design methods. Connect the I port directly to the top-level input port of the design and the O port to the logic in which this input is to source. Specify the desired generic/default values in order to configure the proper behavior of the buffer.

Available Attributes

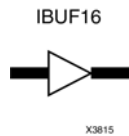
Attribute	Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet.	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

IBUF16

Macro: 16-Bit Input Buffer



Introduction

Input Buffers isolate the internal circuit from the signals coming into the chip. This design element is contained in input/output blocks (IOBs) and allows the specification of the particular I/O Standard to configure the I/O. In general, an this element should be used for all single-ended data input or bidirectional pins.

Design Entry Method

This design element can be used in schematics.

In general, this element is inferred by the synthesis tool for any specified top-level input port to the design. It is generally not necessary to specify them in the source code. However, if desired, they be manually instantiated by either copying the instantiation code from the appropriate Libraries Guide HDL template and pasting it into the top-level entity/module of your code. It is recommended to always put all I/O components on the top-level of the design to help facilitate hierarchical design methods. Connect the I port directly to the top-level input port of the design and the O port to the logic in which this input is to source. Specify the desired generic/defparam values in order to configure the proper behavior of the buffer.

Available Attributes

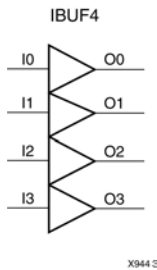
Attribute	Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet.	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

IBUF4

Macro: 4-Bit Input Buffer



Introduction

Input Buffers isolate the internal circuit from the signals coming into the chip. This design element is contained in input/output blocks (IOBs) and allows the specification of the particular I/O Standard to configure the I/O. In general, an this element should be used for all single-ended data input or bidirectional pins.

Design Entry Method

This design element can be used in schematics.

In general, this element is inferred by the synthesis tool for any specified top-level input port to the design. It is generally not necessary to specify them in the source code. However, if desired, they be manually instantiated by either copying the instantiation code from the appropriate Libraries Guide HDL template and pasting it into the top-level entity/module of your code. It is recommended to always put all I/O components on the top-level of the design to help facilitate hierarchical design methods. Connect the I port directly to the top-level input port of the design and the O port to the logic in which this input is to source. Specify the desired generic/defparam values in order to configure the proper behavior of the buffer.

Available Attributes

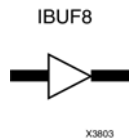
Attribute	Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet.	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

IBUF8

Macro: 8-Bit Input Buffer



Introduction

Input Buffers isolate the internal circuit from the signals coming into the chip. This design element is contained in input/output blocks (IOBs) and allows the specification of the particular I/O Standard to configure the I/O. In general, an this element should be used for all single-ended data input or bidirectional pins.

Design Entry Method

This design element can be used in schematics.

In general, this element is inferred by the synthesis tool for any specified top-level input port to the design. It is generally not necessary to specify them in the source code. However, if desired, they be manually instantiated by either copying the instantiation code from the appropriate Libraries Guide HDL template and pasting it into the top-level entity/module of your code. It is recommended to always put all I/O components on the top-level of the design to help facilitate hierarchical design methods. Connect the I port directly to the top-level input port of the design and the O port to the logic in which this input is to source. Specify the desired generic/defparam values in order to configure the proper behavior of the buffer.

Available Attributes

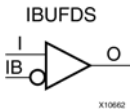
Attribute	Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet.	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

IBUFDS

Primitive: Differential Signaling Input Buffer



Introduction

This design element is an input buffer that supports low-voltage, differential signaling. In IBUFDS, a design level interface signal is represented as two distinct ports (I and IB), one deemed the "master" and the other the "slave." The master and the slave are opposite phases of the same logical signal (for example, MYNET_P and MYNET_N). Optionally, a programmable differential termination feature is available to help improve signal integrity and reduce external components.

Logic Table

Inputs		Outputs
I	IB	O
0	0	No Change
0	1	0
1	0	1
1	1	No Change

Port Descriptions

Port	Type	Width	Function
I	Input	1	Diff_p Buffer Input
IB	Input	1	Diff_n Buffer Input
O	Output	1	Buffer Output

Design Entry Method

This design element can be used in schematics.

Put all I/O components on the top-level of the design to help facilitate hierarchical design methods. Connect the I port directly to the top-level "master" input port of the design, the IB port to the top-level "slave" input port, and the O port to the logic in which this input is to source. Specify the desired generic/defparam values in order to configure the proper behavior of the buffer.

Available Attributes

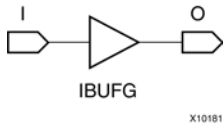
Attribute	Type	Allowed Values	Default	Description
DIFF_TERM	Boolean	TRUE or FALSE	FALSE	Enables the built-in differential termination resistor.
IOSTANDARD	String	See Data Sheet.	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

IBUFG

Primitive: Dedicated Input Clock Buffer



Introduction

The IBUFG is a dedicated input to the device which should be used to connect incoming clocks to the FPGA's global clock routing resources. The IBUFG provides dedicated connections to the DCM_SP and BUFG providing the minimum amount of clock delay and jitter to the device. The IBUFG input can only be driven by the global clock pins. The IBUFG output can drive CLKIN of a DCM_SP, BUFG, or your choice of logic.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Clock Buffer output
I	Input	1	Clock Buffer input

Design Entry Method

This design element can be used in schematics.

Available Attributes

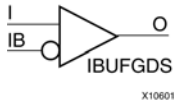
Attribute	Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

IBUFGDS

Primitive: Differential Signaling Dedicated Input Clock Buffer and Optional Delay



Introduction

This design element is a dedicated differential signaling input buffer for connection to the clock buffer (BUFG) or DCM. In IBUFGDS, a design-level interface signal is represented as two distinct ports (I and IB), one deemed the "master" and the other the "slave." The master and the slave are opposite phases of the same logical signal (for example, MYNET_P and MYNET_N). Optionally, a programmable differential termination feature is available to help improve signal integrity and reduce external components. Also available is a programmable delay to assist in the capturing of incoming data to the device.

Logic Table

Inputs		Outputs
I	IB	O
0	0	No Change
0	1	0
1	0	1
1	1	No Change

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Clock Buffer output
IB	Input	1	Diff_n Clock Buffer Input
I	Input	1	Diff_p Clock Buffer Input

Design Entry Method

This design element can be used in schematics.

Put all I/O components on the top-level of the design to help facilitate hierarchical design methods. Connect the I port directly to the top-level "master" input port of the design, the IB port to the top-level "slave" input port and the O port to a DCM, BUFG or logic in which this input is to source. Some synthesis tools infer the BUFG automatically if necessary, when connecting an IBUFG to the clock resources of the FPGA. Specify the desired generic/defparam values in order to configure the proper behavior of the buffer.

Available Attributes

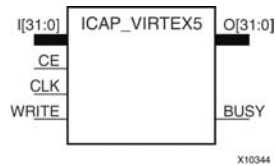
Attribute	Type	Allowed Values	Default	Description
DIFF_TERM	Boolean	TRUE or FALSE	FALSE	Enables the built-in differential termination resistor.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

ICAP_VIRTEX5

Primitive: Internal Configuration Access Port



Introduction

This design element gives you access to the configuration functions of the FPGA from the FPGA fabric. Using this component, commands and data can be written to and read from the configuration logic of the FPGA array. Since the improper use of this function can have a negative effect on the functionality and reliability of the FPGA, you shouldn't use this element unless you are very familiar with its capabilities.

Port Descriptions

Port	Direction	Width	Function
O	Output	32	Configuration data output bus
Busy	Output	1	Busy/Ready output
I	Input	32	Configuration data input bus
WRITE	Input	1	Active Low Write Input
CE	Input	1	Active Low Clock Enable Input
CLK	Input	1	Clock Input

Design Entry Method

This design element can be used in schematics.

Refer to the Configuration User Guide for more details about the parallel bus bit order.

Available Attributes

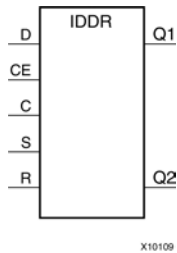
Attribute	Type	Allowed Values	Default	Description
ICAP_WIDTH	String	"X8", "X16", "X32"	"X8"	Specifies the input and output data width to be used with the ICAP_VIRTEX5.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

IDDR

Primitive: Input Dual Data-Rate Register



Introduction

This design element is a dedicated input register designed to receive external dual data rate (DDR) signals into Xilinx® FPGAs. The IDDR is available with modes that present the data to the FPGA fabric at the time and clock edge they are captured, or on the same clock edge. This feature allows you to avoid additional timing complexities and resource usage.

- **OPPOSITE_EDGE mode** - Data is recovered in the classic DDR methodology. Given a DDR data and clock at pin D and C respectively, Q1 changes after every positive edge of clock C, and Q2 changes after every negative edge of clock C.
- **SAME_EDGE mode** - Data is still recovered by opposite edges of clock C. However, an extra register has been placed in front of the negative edge data register. This extra register is clocked with positive clock edge of clock signal C. As a result, DDR data is now presented into the FPGA fabric at the same clock edge. However, because of this feature, the data pair appears to be "separated." Q1 and Q2 no longer have pair 1 and 2. Instead, the first pair presented is Pair 1 and DONT_CARE, followed by Pair 2 and 3 at the next clock cycle.
- **SAME_EDGE_PIPELINED mode** - Recovers data in a similar fashion as the SAME_EDGE mode. In order to avoid the "separated" effect of the SAME_EDGE mode, an extra register has been placed in front of the positive edge data register. A data pair now appears at the Q1 and Q2 pin at the same time. However, using this mode costs you an additional cycle of latency for Q1 and Q2 signals to change.

IDDR also works with the SelectIO™ features, such as the IODELAY.

Note For high speed interfaces, the IDDR_2CLK component can be used to specify two independent clocks to capture the data. Use this component when the performance requirements of the IDDR are not adequate, since the IDDR_2CLK requires more clocking resources and can imply placement restrictions that are not necessary when using the IDDR component.

Port Descriptions

Port	Direction	Width	Function
Q1 - Q2	Output	1	These pins are the IDDR output that connects to the FPGA fabric. Q1 is the first data pair and Q2 is the second data pair.
C	Input	1	Clock input pin.
CE	Input	1	When asserted Low, this port disables the output clock at port O.
D	Input	1	This pin is where the DDR data is presented into the IDDR module. This pin connects to a top-level input or bi-directional port, and IODELAY configured for an input delay or to an appropriate input or bidirectional buffer.
R	Input	1	Active high reset forcing Q1 and Q2 to a logic zero. Can be synchronous or asynchronous based on the SRTYPE attribute.
S	Input	1	Active high reset forcing Q1 and Q2 to a logic one. Can be synchronous or asynchronous based on the SRTYPE attribute.

Design Entry Method

This design element can be used in schematics.

Available Attributes

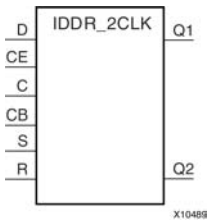
Attribute	Type	Allowed Values	Default	Description
DDR_CLK_EDGE	String	"OPPOSITE_EDGE", "SAME_EDGE", "SAME_EDGE_PIPELINED"	"OPPOSITE_EDGE"	Sets the IDDR mode of operation with respect to clock edge.
INIT_Q1	Binary	0, 1	0	Initial value on the Q1 pin after configuration startup or when GSR is asserted.
INIT_Q2	Binary	0, 1	0	Initial value on the Q2 pin after configuration startup or when GSR is asserted.
SRTYPE	String	"SYNC" or "ASYNC"	"SYNC"	Set/reset type selection. "SYNC" specifies the behavior of the reset (R) and set (S) pins to be synchronous to the positive edge of the C clock pin. "ASYNC" specifies an asynchronous set/reset function.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

IDDR_2CLK

Primitive: Input Dual Data-Rate Register with Dual Clock Inputs



Introduction

This design element is a dedicated input register designed to receive external dual data rate (DDR) signals into Xilinx® FPGAs. In general, you should only use the IDDR_2CLK for very high speed interfaces, since it requires more clocking resources, more power, and can imply certain placement restrictions that are not necessary when using the IDDR component. Alternatively, the IDDR component is easier to use, uses fewer resources, and has fewer restrictions, though it cannot operate at the same high I/O speeds. The IDDR_2CLK is available with modes that present the data to the FPGA fabric at the time and clock edge they are captured, or on the same clock edge. This feature allows designers to avoid additional timing complexities and resource usage.

- **OPPOSITE_EDGE mode** - Data is presented in the classic DDR methodology. Given a DDR data and clock at pin D and C respectively, Q1 changes after every positive edge of clock C, and Q2 changes after every positive edge of clock CB.
- **SAME_EDGE mode** - Data is still presented by positive edges of each clock. However, an extra register has been placed in front of the CB clocked data register. This extra register is clocked with positive clock edge of clock signal C. As a result, DDR data is now presented into the FPGA fabric at the positive edge of clock C. However, because of this feature, the data pair appears to be "separated." Q1 and Q2 no longer have pair 1 and 2. Instead, the first pair presented is Pair 1 and DON'T CARE, followed by Pair 2 and 3 at the next clock cycle.
- **SAME_EDGE_PIPELINED mode** - Presents data in a similar fashion as the SAME_EDGE mode. In order to avoid the "separated" effect of the SAME_EDGE mode, an extra register has been placed in front of the C clocked data register. A data pair now appears at the Q1 and Q2 pin at the same time during the positive edge of C. However, using this mode, costs you an additional cycle of latency for Q1 and Q2 signals to change.

IDDR also works with SelectIO™ features, such as the IODELAY.

Port Descriptions

Port	Direction	Width	Function
Q1 : Q2	Output	1	These pins are the IDDR output that connects to the FPGA fabric. Q1 is the first data pair and Q2 is the second data pair.
C	Input	1	Primary clock input pin used to capture the positive edge data.
CB	Input	1	Secondary clock input pin (typically 180 degrees out of phase with the primary clock) used to capture the negative edge data.
CE	Input	1	When asserted Low, this port disables the output clock at port O.
D	Input	1	This pin is where the DDR data is presented into the IDDR module. This pin connects to a top-level input or bi-directional port, and IODELAY configured for an input delay or to an appropriate input or bidirectional buffer.

Port	Direction	Width	Function
R	Input	1	Active high reset forcing Q1 and Q2 to a logic zero. Can be synchronous or asynchronous based on the SRTYPE attribute.
S	Input	1	Active high reset forcing Q1 and Q2 to a logic one. Can be synchronous or asynchronous based on the SRTYPE attribute.

Design Entry Method

This design element can be used in schematics.

- Connect the C pin to the appropriate clock source, representing the positive clock edge and CB to the clock source representing the negative clock edge.
- Connect the D pin to the top-level input, or bidirectional port, an IODELAY, or an instantiated input or bidirectional buffer.
- The Q1 and Q2 pins should be connected to the appropriate data sources.
- CE should be tied high when not used, or connected to the appropriate clock enable logic.
- R and S pins should be tied low, if not used, or to the appropriate set or reset generation logic.
- Set all attributes to the component to represent the desired behavior.
- Always instantiate this component in pairs with the same clocking, and to LOC those to the appropriate P and N I/O pair in order not to sacrifice possible I/O resources.
- Always instantiate this component in the top-level hierarchy of your design, along with any other instantiated I/O components for the design. This helps facilitate hierarchical design flows/practices.
- To minimize CLK skew, both CLK and CLKB should come from global routing (DCM / MMCM) and not from the local inversion. DCM / MMCM de-skews these clocks whereas the local inversion adds skew.

Available Attributes

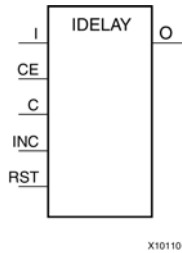
Attribute	Type	Allowed Values	Default	Description
DDR_CLK_EDGE	String	"OPPOSITE_EDGE", "SAME_EDGE" "SAME_EDGE_PIPELINED"	"OPPOSITE_EDGE"	DDR clock mode recovery mode selection. See Introduction for more explanation.
INIT_Q1	Binary	0, 1	0	Initial value on the Q1 pin after configuration startup or when GSR is asserted.
INIT_Q2	Binary	0, 1	0	Initial value on the Q2 pin after configuration startup or when GSR is asserted.
SRTYPE	String	"SYNC" or "ASYNC"	"SYNC"	Set/reset type selection. SYNC specifies the behavior of the reset (R) and set (S) pins to be synchronous to the positive edge of the C clock pin. "ASYNC" specifies an asynchronous set/reset function.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

IDELAY

Primitive: Input Delay Element



Introduction

Virtex® devices have an IDELAY module in the input path of every user I/O. IDELAY allows the implementation of deskew algorithms to correctly capture incoming data. IDELAY can be applied to data signals, clock signals, or both. IDELAY features a fully-controllable, 64-tap delay line. When used in conjunction with the IDELAYCTRL component circuitry, the IDELAY can provide precise time increments of delay independent of process, voltage, and temperature (PVT) variations. Three modes of operation are available:

- **Zero hold time delay mode** - This mode of operation allows backward compatibility for designs using the zero-hold time delay feature. When used in this mode, the IDELAYCTRL primitive does not need to be instantiated.
- **Fixed tap-delay mode** - In the fixed tap-delay mode, the delay value is set to the number determined by the attribute IOBDELAY_VALUE. This value cannot be changed during run-time. When used in this mode, the IDELAYCTRL primitive must be instantiated.
- **Variable tap-delay mode** - In the variable tap-delay mode, the delay value can be changed at run-time by manipulating the control signals CE and INC. When used in this mode, the IDELAYCTRL primitive must be instantiated.

Port Descriptions

Ports	Direction	Width	Function
I	Input	1	Serial input data from IOB
C	Input	1	Clock input
INC	Input	1	Increment/decrement number of tap delays
CE	Input	1	Enable increment/decrement function
RST	Input	1	Reset delay chain to pre-programmed value. If no value programmed, reset to 0
O	Output	1	Combinatorial output

Data Input and Output - I and O

IDELAY primitives are located in three different types of general purpose IOB locations. The input and output connectivity differs for each type of IOB location.

- **General Purpose IOBs** - The input of IDELAY in a general-purpose IOB comes directly from the input buffer, IBUF. The output of IDELAY (O) is connected directly to your logic. The input and output datapath is combinatorial and is not affected by the clock signal (C). However, you can choose to register the output signal (O) in the IOB.
- **Regional Clock-Capable IOBs** - Regional clock-capable IOBs are located in one I/O pair directly above and below an HCLK IOB. The input of IDELAY in a regional clock-capable IOB comes directly from the input buffer, IBUF. The output of IDELAY in a regional clock-capable IOB can go to one of the following locations:
 - Directly to your logic
 - BUFIO (in the case of a regional clock signal)

The regional clock buffer, BUFIO, connects the incoming regional clock signal to the regional I/O clock tree, IOCLK. BUFIO also connects to the regional clock buffer, BUFR to connect to the regional clock tree, rclk. The input and output datapath is combinatorial and is not affected by the clock signal (C). However, you can choose to register the output signal (O) in the IOB.

- **Global clock-capable IOBs** - Global clock-capable IOBs are located in the center I/O column. The input of the IDELAY module in a global clock-capable IOB comes directly from the input global clock buffer, IBUFG. The output of the IDELAY module in a global clock-capable IOB can go to one of the following locations:
 - Directly to your logic
 - BUFG (in the case of a global clock signal)

The global clock buffer, BUFG, connects the incoming regional clock signal to the global clock tree, gclk. The input and output datapath is combinatorial and is not affected by the clock signal (C). However, you can choose to register the output signal (O) in the IOB.

Clock Input - C

All control inputs to IDELAY (RST, CE and INC) are synchronous to the clock input (C). The data input and output (I and O) of IDELAY is not affected by this clock signal. This clock input is identical to the CLKDIV input for the ISERDES. All the clock sources used to drive CLKDIV can therefore drive the IDELAY clock input (C). The clock sources that can drive the clock input (C) are:

- Eight gclk (global clock tree)
- Two rclk (regional clock tree)

Module Reset - RST

The IDELAY reset signal, RST, resets the tap-delay line to a value set by the IOBDELAY_VALUE attribute. If the IOBDELAY_VALUE attribute is not specified, the tap-delay line is reset to 0.

Increment/Decrement Signals - CE, INC

The increment/decrement enable signal (CE) determines when the increment/decrement signal (INC) is activated. INC determines whether to increment or decrement the tap-delay line. When CE = 0, the tap delay remains constant no matter what the value of INC. When CE = 1, the tap-delay value increments or decrements depending on the value of INC. The tap delay is incremented or decremented synchronously with respect to the input clock (C). As long as CE = 1, the tap-delay increments or decrements by one every clock cycle. The increment/decrement operation is summarized in the following table:

Operation	RST	CE	INC
Reset to configured value of tap count	1	x	x
Increment tap count	0	1	1
Decrement tap count	0	1	0
No change	0	0	x

Note

1. RST resets delay chain to tap count specified by attribute IOBDELAY_VALUE. If IOBDELAY_VALUE is not specified, tap count reset to 0.
2. RST, CE, and INC are synchronous to the input clock signal (C).

When CE is raised, the increment/decrement operation begins on the next positive clock cycle. When CE is lowered, the increment/decrement operation ceases on the next positive clock cycle.

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
IOBDELAY_TYPE	String	"DEFAULT", "FIXED", "VARIABLE"	"DEFAULT"	This attribute sets the type of tap delay.
IOBDELAY_VALUE	Integer	0 to 63	0	This attribute specifies the initial number of tap delays.

IOBDELAY_TYPE Attribute

The IOBDELAY_TYPE attribute sets the type of delay used. The attribute values are DEFAULT, FIXED, and VARIABLE. The default value is DEFAULT. When set to DEFAULT, the zero-hold time delay element is selected. This delay element eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the device. When used, it guarantees a pad-to-pad hold time of zero.

When set to FIXED, the tap-delay value is fixed at the number of taps determined by the IOBDELAY_VALUE attribute. This value is preset and cannot be changed dynamically.

When set to VARIABLE, the variable tap delay is selected. The tap delay can be incremented by setting CE = 1 and INC = 1 or decremented by setting CE = 1 and INC = 0. The increment/decrement operation is synchronous to C, the input clock signal.

IOBDELAY_VALUE Attribute

The IOBDELAY_VALUE attribute specifies the initial number of tap delays. The possible values are any Integers from 0 to 63. The default value is 0. When set to 0, the total delay becomes the delay of the output MUX which is approximately 400 ps.

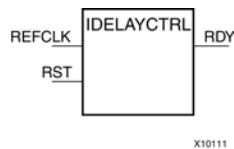
The value of the tap delay reverts to IOBDELAY_VALUE when the tap delay is reset (RST = 1), or the IOBDELAY_TYPE is set to FIXED.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

IDELAYCTRL

Primitive: IDELAY Tap Delay Value Control



Introduction

This design element must be instantiated when using the tap-delay line. This occurs when the IDELAY or ISERDES primitive is instantiated with the IOBDELAY_TYPE attribute set to Fixed or Variable. The IDELAYCTRL module provides a voltage bias, independent of process, voltage, and temperature variations to the tap-delay line using a fixed-frequency reference clock, REFCLK. This enables very accurate delay tuning.

Port Descriptions

Port	Type	Width	Function
RDY	Output	1	Indicates the validity of the reference clock input, REFCLK. When REFCLK disappears (i.e., REFCLK is held High or Low for one clock period or more), the RDY signal is deasserted.
REFCLK	Input	1	Provides a voltage bias, independent of process, voltage, and temperature variations, to the tap-delay lines in the IOBs. The frequency of REFCLK must be 200 MHz to guarantee the tap-delay value specified in the applicable data sheet.
RST	Input	1	Resets the IDELAYCTRL circuitry. The RST signal is an active-high asynchronous reset. To reset the IDELAYCTRL, assert it High for at least 50 ns.

RST (Module reset) - Resets the IDELAYCTRL circuitry. The RST signal is an active-high asynchronous reset. To reset the IDELAYCTRL, assert it High for at least 50 ns.

REFCLK (Reference Clock) - Provides a voltage bias, independent of process, voltage, and temperature variations, to the tap-delay lines in the IOBs. The frequency of REFCLK must be 200 MHz to guarantee the tap-delay value specified in the applicable data sheet.

RDY (Ready Output) - Indicates the validity of the reference clock input, REFCLK. When REFCLK disappears (i.e., REFCLK is held High or Low for one clock period or more), the RDY signal is deasserted.

Design Entry Method

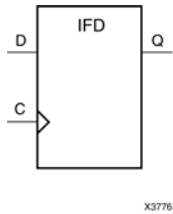
This design element can be used in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

IFD

Macro: Input D Flip-Flop



Introduction

This D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The (D) input provides data input for the flip-flop, which synchronizes data entering the chip. The data on input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs		Outputs
D	C	Q
D	↑	D

Design Entry Method

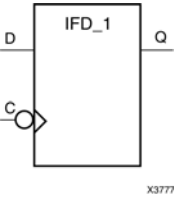
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

IFD_1

Macro: Input D Flip-Flop with Inverted Clock (Asynchronous Preset)



Introduction

This design element is a D-type flip flop which is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD. The D input also provides data input for the flip-flop, which synchronizes data entering the chip. The D input data is loaded into the flip-flop during the High-to-Low clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs		Outputs
D	C	Q
0	↓	0
1	↓	1

Design Entry Method

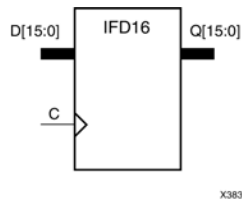
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

IFD16

Macro: 16-Bit Input D Flip-Flop



Introduction

This D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The (D) input provides data input for the flip-flop, which synchronizes data entering the chip. The data on input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs		Outputs
D	C	Q
D	↑	D

Design Entry Method

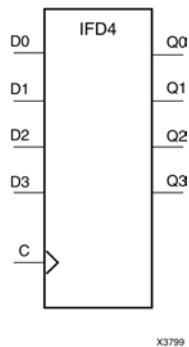
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

IFD4

Macro: 4-Bit Input D Flip-Flop



Introduction

This D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The (D) input provides data input for the flip-flop, which synchronizes data entering the chip. The data on input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs		Outputs
D	C	Q
D	↑	D

Design Entry Method

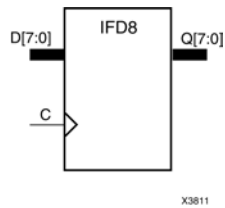
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

IFD8

Macro: 8-Bit Input D Flip-Flop



Introduction

This D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The (D) input provides data input for the flip-flop, which synchronizes data entering the chip. The data on input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs		Outputs
D	C	Q
D	↑	D

Design Entry Method

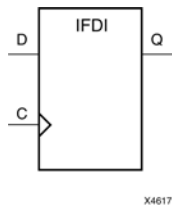
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

IFDI

Macro: Input D Flip-Flop (Asynchronous Preset)



Introduction

This design element is a D-type flip-flop which is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD. The D input provides data input for the flip-flop, which synchronizes data entering the chip. The D input data is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs		Outputs
D	C	Q
D	↑	D

Design Entry Method

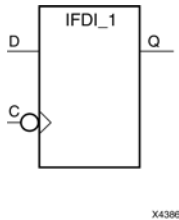
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

IFDI_1

Macro: Input D Flip-Flop with Inverted Clock (Asynchronous Preset)



Introduction

The design element is a D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD. The (D) input provides data input for the flip-flop, which synchronizes data entering the chip. The data on input (D) is loaded into the flip-flop during the High-to-Low clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs		Outputs
D	C	Q
0	↓	D

Design Entry Method

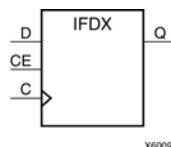
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

IFDX

Macro: Input D Flip-Flop with Clock Enable



Introduction

This D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The D input provides data input for the flip-flop, which synchronizes data entering the chip. When CE is High, the data on input D is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin. When CE is Low, flip-flop outputs do not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
CE	D	C	Q
1	D	↑	D
0	X	X	No Change

Design Entry Method

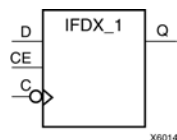
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

IFDX_1

Macro: Input D Flip-Flop with Inverted Clock and Clock Enable



Introduction

This design element is a D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD. The D input also provides data input for the flip-flop, which synchronizes data entering the chip. When CE is High, the data on input D is loaded into the flip-flop during the High-to-Low clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin. When the CE pin is Low, the output (Q) does not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs
CE	D	C	Q
1	D	↓	D
0	X	X	No Change

Design Entry Method

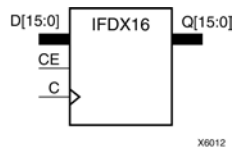
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

IFDX16

Macro: 16-Bit Input D Flip-Flops with Clock Enable



Introduction

This D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The D input provides data input for the flip-flop, which synchronizes data entering the chip. When CE is High, the data on input D is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin. When CE is Low, flip-flop outputs do not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs
CE	D	C	Q
1	D	↑	D
0	X	X	No Change

Design Entry Method

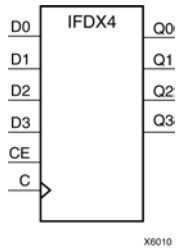
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

IFDX4

Macro: 4-Bit Input D Flip-Flop with Clock Enable



Introduction

This D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The D input provides data input for the flip-flop, which synchronizes data entering the chip. When CE is High, the data on input D is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin. When CE is Low, flip-flop outputs do not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
CE	D	C	Q
1	D	↑	D
0	X	X	No Change

Design Entry Method

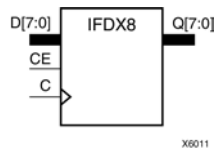
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

IFDX8

Macro: 8-Bit Input D Flip-Flop with Clock Enable



Introduction

This D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The D input provides data input for the flip-flop, which synchronizes data entering the chip. When CE is High, the data on input D is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin. When CE is Low, flip-flop outputs do not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs
CE	D	C	Q
1	D	↑	D
0	X	X	No Change

Design Entry Method

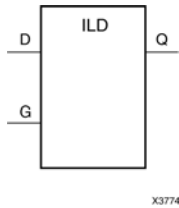
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

ILD

Macro: Transparent Input Data Latch



Introduction

This design element is a single, transparent data latch that holds transient data entering a chip. This latch is contained in an input/output block (IOB). The latch input (D) is connected to an IPAD or an IOPAD (without using an IBUF). When the gate input (G) is High, data on the input (D) appears on the output (Q). Data on the D input during the High-to-Low G transition is stored in the latch.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs		Output
G	D	Q
1	D	D
0	X	No Change
↓	D	D

Design Entry Method

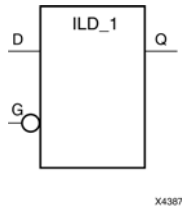
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

ILD_1

Macro: Transparent Input Data Latch with Inverted Gate



Introduction

This design element is a transparent data latch that holds transient data entering a chip. When the gate input (G) is Low, data on the data input (D) appears on the data output (Q). Data on (D) during the Low-to-High (G) transition is stored in the latch.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs		Outputs
G	D	Q
0	D	D
1	X	No Change
↑	D	D

Design Entry Method

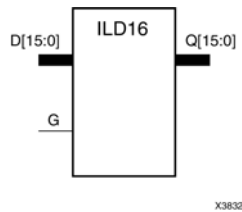
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

ILD16

Macro: Transparent Input Data Latch



Introduction

These design elements are multiple transparent data latches that hold transient data entering a chip. The ILD latch is contained in an input/output block (IOB). The latch input (D) is connected to an IPAD or an IOPAD (without using an IBUF). When the gate input (G) is High, data on the inputs (D) appears on the outputs (Q). Data on the D inputs during the High-to-Low G transition is stored in the latch.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs		Outputs
G	D	Q
1	Dn	Dn
0	X	No Change
↓	Dn	Dn

Design Entry Method

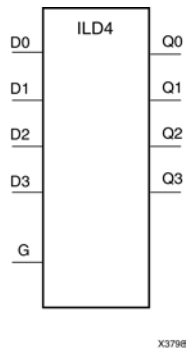
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

ILD4

Macro: Transparent Input Data Latch



Introduction

These design elements are multiple transparent data latches that hold transient data entering a chip. The ILD latch is contained in an input/output block (IOB). The latch input (D) is connected to an IPAD or an IOPAD (without using an IBUF). When the gate input (G) is High, data on the inputs (D) appears on the outputs (Q). Data on the D inputs during the High-to-Low G transition is stored in the latch.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs		Outputs
G	D	Q
1	Dn	Dn
0	X	No Change
↓	Dn	Dn

Design Entry Method

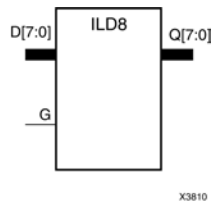
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

ILD8

Macro: Transparent Input Data Latch



Introduction

These design elements are multiple transparent data latches that hold transient data entering a chip. The ILD latch is contained in an input/output block (IOB). The latch input (D) is connected to an IPAD or an IOPAD (without using an IBUF). When the gate input (G) is High, data on the inputs (D) appears on the outputs (Q). Data on the D inputs during the High-to-Low G transition is stored in the latch.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs		Outputs
G	D	Q
1	Dn	Dn
0	X	No Change
↓	Dn	Dn

Design Entry Method

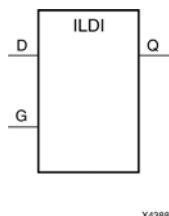
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

ILDI

Macro: Transparent Input Data Latch (Asynchronous Preset)



Introduction

This design element is a transparent data latch that holds transient data entering a chip. When the gate input (G) is High, data on the input (D) appears on the output (Q). Data on the D input during the High-to-Low G transition is stored in the latch.

The ILDI is the input flip-flop master latch. It is possible to access two different outputs from the input flip-flop: one that responds to the level of the clock signal and another that responds to an edge of the clock signal. When using both outputs from the same input flip-flop, a transparent High latch (ILDI) corresponds to a falling edge-triggered flip-flop (IFDI_1). Similarly, a transparent Low latch (ILDI_1) corresponds to a rising edge-triggered flip-flop (IFDI).

The latch is asynchronously preset, output High, when power is applied.

For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs		Outputs
G	D	Q
1	D	D
0	X	D
↓	D	D

Design Entry Method

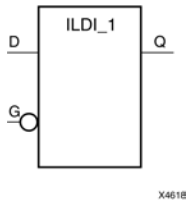
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

ILDI_1

Macro: Transparent Input Data Latch with Inverted Gate (Asynchronous Preset)



Introduction

This design element is a transparent data latch that holds transient data entering a chip. When the gate input (G) is Low, data on the data input (D) appears on the data output (Q). Data on D during the Low-to-High G transition is stored in the latch.

The latch is asynchronously preset, output High, when power is applied.

For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs		Outputs
G	D	Q
0	1	1
0	0	0
1	X	No Change
↑	D	D

Design Entry Method

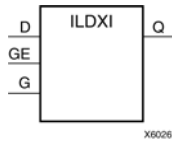
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

ILDXI

Macro: Transparent Input Data Latch (Asynchronous Preset)



Introduction

This design element is a transparent data latch that holds transient data entering a chip. When the gate input (G) is High, data on the input (D) appears on the output (Q). Data on the (D) input during the High-to-Low (G) transition is stored in the latch.

The ILDXI is the input flip-flop master latch. Two outputs can be accessed from the input flip-flop: one that responds to the level of the clock signal and another that responds to an edge of the clock signal. When using both outputs from the same input flip-flop, a transparent High latch (ILDXI) corresponds to a falling edge-triggered flip-flop (IFDXI_1). Similarly, a transparent Low latch (ILDXI_1) corresponds to a rising edge-triggered flip-flop (IFDXI).

The latch is asynchronously preset, output High, when power is applied.

For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
GE	G	D	Q
0	X	X	No Change
1	0	X	No Change
1	1	D	D
1	↓	D	D

Design Entry Method

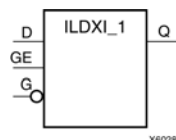
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

ILDXI_1

Macro: Transparent Input Data Latch with Inverted Gate (Asynchronous Preset)



Introduction

This design element is a transparent data latch that holds transient data entering a chip.

The latch is asynchronously preset, output High, when power is applied.

For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs			Outputs
GE	G	D	Q
0	X	X	No Change
1	1	X	No Change
1	0	D	D
1	↑	D	D

Design Entry Method

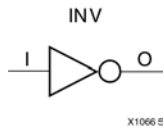
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

INV

Primitive: Inverter



Introduction

This design element is a single inverter that identifies signal inversions in a schematic.

Design Entry Method

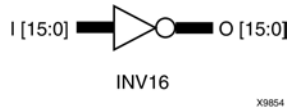
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

INV16

Macro: 16 Inverters



Introduction

This design element is a multiple inverter that identifies signal inversions in a schematic.

Design Entry Method

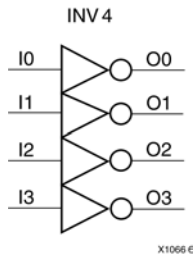
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

INV4

Macro: Four Inverters



Introduction

This design element is a multiple inverter that identifies signal inversions in a schematic.

Design Entry Method

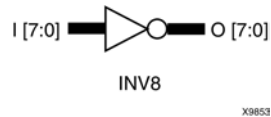
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

INV8

Macro: Eight Inverters



Introduction

This design element is a multiple inverter that identifies signal inversions in a schematic.

Design Entry Method

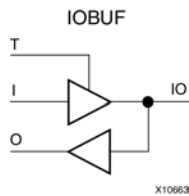
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

IOBUF

Primitive: Bi-Directional Buffer



Introduction

The design element is a bidirectional single-ended I/O Buffer used to connect internal logic to an external bidirectional pin.

Logic Table

Inputs		Bidirectional	Outputs
T	I	IO	O
1	X	Z	X
0	1	1	1
0	0	0	0

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Buffer output
IO	Inout	1	Buffer inout
I	Input	1	Buffer input
T	Input	1	3-State enable input

Design Entry Method

This design element can be used in schematics.

Available Attributes

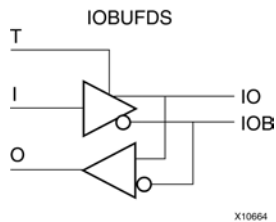
Attribute	Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Selects output drive strength (mA) for the SelectIO™ buffers that use the LVTTTL, LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, or LVCMOS33 interface I/O standard.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW", "FAST", "QUIETIO"	"SLOW"	Sets the output rise and fall time. See the Data Sheet for recommendations of the best setting for this attribute.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

IOBUFDS

Primitive: 3-State Differential Signaling I/O Buffer with Active Low Output Enable



Introduction

The design element is a bidirectional buffer that supports low-voltage, differential signaling. For the IOBUFDS, a design level interface signal is represented as two distinct ports (IO and IOB), one deemed the "master" and the other the "slave." The master and the slave are opposite phases of the same logical signal (for example, MYNET_P and MYNET_N). Optionally, a programmable differential termination feature is available to help improve signal integrity and reduce external components. Also available is a programmable delay to assist in the capturing of incoming data to the device.

Logic Table

Inputs		Bidirectional		Outputs
I	T	IO	IOB	O
X	1	Z	Z	No Change
0	0	0	1	0
1	0	1	0	1

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Buffer output
IO	Inout	1	Diff_p inout
IOB	Inout	1	Diff_n inout
I	Input	1	Buffer input
T	Input	1	3-state enable input

Design Entry Method

This design element can be used in schematics.

Available Attributes

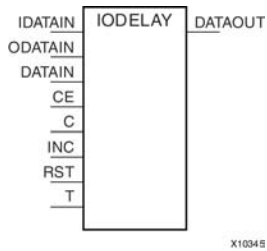
Attribute	Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

IODELAY

Primitive: Input and Output Fixed or Variable Delay Element



Introduction

This design element can be used to provide a fixed delay or an adjustable delay to the input path and a fixed delay for the output path of the FPGA. This delay can be useful for the purpose of data alignment of incoming or outgoing data to/from the chip, as well as allowing for the tracking of data alignment over process, temperature, and voltage (PVT). The IODELAY is available on all FPGA I/Os and, when used in conjunction with the IDELAYCTRL component circuitry, can provide precise time increments of delay. When used in variable mode, the input path can be adjusted for increasing and decreasing amounts of delay. The output delay path is only available in a fixed delay. The IODELAY can also be used to add additional static or variable delay to an internal path (within the FPGA fabric). However, when IODELAY is used that way, this device is no longer available to the associated I/O for input or output path delays.

Port Descriptions

Port	Direction	Width	Function
DATAOUT	Output	1	Delayed data output from input port (connect to input datapath logic)
IDATAIN	Input	1	Data input to device from the I/O (connect directly to port, I/O Buffer). When IDATAIN is used, DATAIN must be tied to a logic zero (ground).
ODATAIN	Input	1	Data input for the output datapath from the device (connect to output data source). When ODATAIN is used, DATAIN must be tied to a logic zero (ground).
DATAIN	Input	1	Data input for the internal datapath delay. When DATAIN is used, IDATAIN and ODATAIN must be tied to a logic zero (ground).
T	Input	1	3-state input control. Tie high for input-only or internal delay or tie low for output only.
CE	Input	1	Active high enable increment/decrement function
INC	Input	1	Increment / Decrement tap delay
C	Input	1	Clock input (Must be connected for variable mode)
RST	Input	1	Active high, synchronous reset, resets delay chain to IDELAY_VALUE/ ODELAY_VALUE tap. If no value is specified, the default is 0.

Design Entry Method

This design element can be used in schematics.

For input delay operation, connect the IDATAIN pin directly to either the top-level I/O port, input buffer, or I/O buffer. For output delay, connect the ODATAIN input to the logic sourcing the output data to be delayed. For internal path delays, connect the DATAIN pin to the proper source and destination logic within the FPGA. When you are using the IODELAY for internal signal delays, the IDATAIN and ODATAIN must be tied to a logic zero (ground).

In all cases, the DATAOUT should be connected to the I/Os or logic to be sourced from the delayed data. Connect the T pin to the control signal for the 3-state output operation when you are using the IODELAY. If you are using the IODELAY for output delays only, tie the T pin to a logic zero (ground). If you are using the IODELAY for input only, or for delaying an internal signal, tie the T pin to a logic one (Vcc). If the IODELAY is configured for VARIABLE delay, connect the CE, INC, C, and RST pins to the appropriate delay control signals. If only a FIXED delay mode is used, those pins should be tied to a logic zero (ground).

Available Attributes

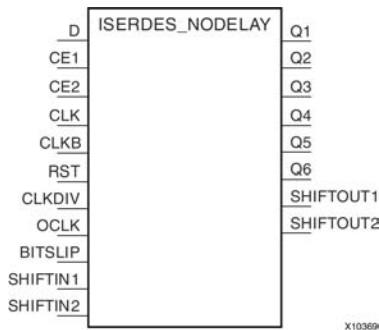
Attribute	Type	Allowed Values	Default	Description
HIGH_PERFORMANCE_MODE	Boolean	TRUE, FALSE	FALSE	When TRUE, this attribute reduces the output jitter.
DELAY_SRC	String	"I", "O", "IO" or "DATAIN"	"I"	Specifies the source to the IODELAY component. "I" means it will be connected directly to an input port or IBUF (input mode), "O" means it will be connected to an output port or OBUF (output mode), "IO" means it will be connected to a port, and "DATAIN" means it will not be connected to any port (internal mode).
IDELAY_TYPE	String	"DEFAULT", "FIXED" or "VARIABLE"	"DEFAULT"	Specifies a fixed, variable or default (eliminate hold time) input delay.
IDELAY_VALUE	Integer	0 to 63	0	Specifies the number of taps of delay for the input path when in fixed mode or the initial delay tap value for variable mode.
ODELAY_VALUE	Integer	0 to 63	0	Specifies the number of taps of delay for the output path.
REFCLK_FREQUENCY	Real	190.00 to 210.00	200.00	When using an associated IDELAYCTRL, specifies the input reference frequency to the component.
SIGNAL_PATTERN	String	"CLOCK", "DATA"	"DATA"	Used by the delay calculator to determine different propagation delays through the IODELAY block based on the setting. DATA will be the addition of per tap delay and per tap jitter. No jitter is introduced for clock-like signals.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

ISERDES_NODELAY

Primitive: Input SERIAL/DESerializer



Introduction

The ISERDES_NODELAY is an input serial-to-parallel data converter that helps facilitate high-speed, source synchronous, serial data capturing. The ISERDES_NODELAY includes logic to assist in clocking and data alignment of either single data rate (SDR) or double data rate (DDR) data to/from 2- to 6-bit data widths for a single instance (MASTER) and 7- to 10-bit data widths for two cascaded ISERDES_NODELAY (MASTER/SLAVE). The ISERDES_NODELAY can be used in memory, networking or a number of different types of data interface applications. The ISERDES_NODELAY can be used in conjunction with an IODELAY component to assist in data alignment of the input serial data. In DDR mode, the ISERDES_NODELAY can be clocked by either a single clock or two clocks for capturing data. When you are using it in two clock mode, higher performance is possible. However, using it in this way might require more clocking resources, consume more power, and require certain placement restriction. Use single clock mode when the highest I/O performance is not needed.

Port Descriptions

Port	Direction	Width	Function
Q1 - Q6	Output	1	Registered parallelized input data.
SHIFTOUT1 / SHIFTOUT2	Output	1	If ISERDES_MODE="MASTER" and two ISERDES_NODELAY are to be cascaded, connect to the slave ISERDES_NODELAY IDATASHIFTIN1/2 inputs.
D	Input	1	Input data to be connected directly to the top-level input or I/O port of the design or to an IODELAY component if additional input delay control is desired.
BITSLIP	Input	1	Input data BITSLIP function enable.
CE1 / CE2	Input	1	Input data register clock enables.
CLK	Input	1	Primary clock input pin used.
CLKB	Input	1	The bit ordering at the input of an OSERDES is the opposite of the bit ordering at the output of an ISERDES_NODELAY block. Please see the appropriate device user guide for detailed information.
CLKDIV	Input	1	Divided clock to be used for parallelized data.
OCLK	Input	1	High speed output clock typically used for memory interfaces.

Port	Direction	Width	Function
SHIFTIN1 / SHIFTIN2	Input	1	If ISERDES_MODE="SLAVE" connect to the master ISERDES_NODELAY IDATASHIFTOUT1/2 outputs. This pin must be grounded.
RST	Input	1	Active high asynchronous reset signal for the registers of the SERDES.

Design Entry Method

This design element can be used in schematics.

Available Attributes

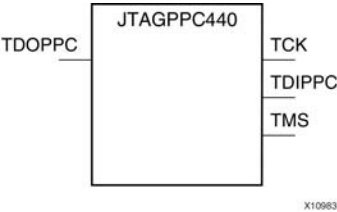
Attribute	Type	Allowed Values	Default	Description
BITSLIP_ENABLE	Boolean	TRUE or FALSE	FALSE	Enable the BITSLIP functionality. Only available in NETWORKING mode.
DATA_RATE	String	"SDR" or "DDR"	"DDR"	Single Data Rate or Double Data Rate operation
DATA_WIDTH	Integer	4,6,8 or 10 if DATA_RATE="DDR", 2,3,4,5,6,7 or 8 if DATA_RATE="SDR"	4	Parallel data width selection
INTERFACE_TYPE	String	"MEMORY" or "NETWORKING"	"MEMORY"	Memory or Networking interface type
SERDES_MODE	String	"MASTER" or "SLAVE"	"MASTER"	Specify whether the ISERDES is operating in master or slave modes when cascaded width expansion.
NUM_CE	Integer	1 or 2	2	Specifies the number of clock enables used for the ISERDES_NODELAY.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

JTAGPPC440

Primitive: JTAG Primitive for the Power PC



Introduction

This design element connects the JTAG logic in the PPC440 core to the JTAG logic of the FPGA device in which the core resides. The connections are made through programmable routing, so the connection only exists after configuration.

Port Descriptions

Inputs	Outputs
TDOPPC	TCK
	TDIPPC
	TMS

Design Entry Method

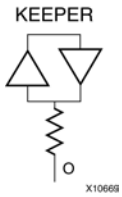
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

KEEPER

Primitive: KEEPER Symbol



Introduction

The design element is a weak keeper element that retains the value of the net connected to its bidirectional O pin. For example, if a logic 1 is being driven onto the net, KEEPER drives a weak/resistive 1 onto the net. If the net driver is then 3-stated, KEEPER continues to drive a weak/resistive 1 onto the net.

Port Descriptions

Name	Direction	Width	Function
O	Output	1-Bit	Keeper output

Design Entry Method

This design element can be used in schematics.

This element can be connected to a net in the following locations on a top-level schematic file:

- A net connected to an input IO Marker
- A net connected to both an output IO Marker and 3-statable IO element, such as an OBUFT.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

KEY_CLEAR

Primitive: Virtex-5 Configuration Encryption Key Erase



Introduction

This design element allows you to erase the configuration encryption circuit key register from internal logic.

Port Descriptions

Port	Direction	Width	Function
KEYCLEARB	Input	1	Active low input, clears the configuration encryption key

Design Entry Method

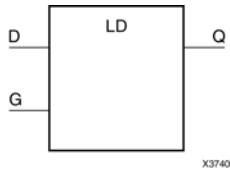
This design element can be used in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LD

Primitive: Transparent Data Latch



Introduction

LD is a transparent data latch. The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is High. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs		Outputs
G	D	Q
1	D	D
0	X	No Change
↓	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

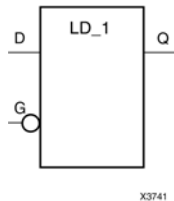
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LD_1

Primitive: Transparent Data Latch with Inverted Gate



Introduction

This design element is a transparent data latch with an inverted gate. The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is Low. The data on the (D) input during the Low-to-High gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains High.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs		Outputs
G	D	Q
0	D	D
1	X	No Change
↑	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

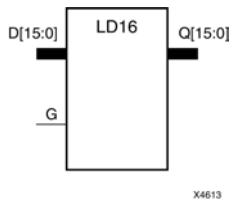
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LD16

Macro: Multiple Transparent Data Latch



Introduction

This design element has 16 transparent data latches with a common gate enable (G). The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is High. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs		Outputs
G	D	Q
1	D _n	D _n
0	X	No Change
↓	D _n	D _n

Design Entry Method

This design element is only for use in schematics.

Available Attributes

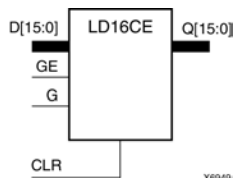
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	Any 16-Bit Value	All zeros	Sets the initial value of Q output after configuration

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LD16CE

Macro: Transparent Data Latch with Asynchronous Clear and Gate Enable



Introduction

This design element has 16 transparent data latches with asynchronous clear and gate enable. When the asynchronous clear input (CLR) is High, it overrides the other inputs and resets the data (Q) outputs Low. (Q) reflects the data (D) inputs while the gate (G) and gate enable (GE) are High, and (CLR) is Low. If (GE) is Low, data on (D) cannot be latched. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) or (GE) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs
CLR	GE	G	Dn	Qn
1	X	X	X	0
0	0	X	X	No Change
0	1	1	Dn	Dn
0	1	0	X	No Change
0	1	↓	Dn	Dn

Design Entry Method

This design element is only for use in schematics.

Available Attributes

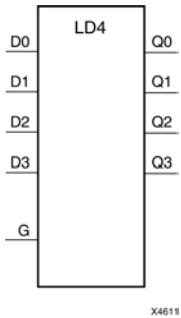
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	Any 16-Bit Value	All zeros	Sets the initial value of Q output after configuration

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LD4

Macro: Multiple Transparent Data Latch



Introduction

This design element has four transparent data latches with a common gate enable (G). The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is High. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs		Outputs
G	D	Q
1	Dn	Dn
0	X	No Change
↓	Dn	Dn

Design Entry Method

This design element is only for use in schematics.

Available Attributes

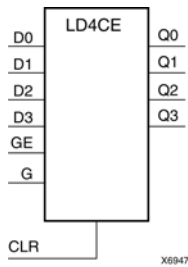
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	Any 4-Bit Value	All zeros	Sets the initial value of Q output after configuration

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LD4CE

Macro: Transparent Data Latch with Asynchronous Clear and Gate Enable



Introduction

This design element has 4 transparent data latches with asynchronous clear and gate enable. When the asynchronous clear input (CLR) is High, it overrides the other inputs and resets the data (Q) outputs Low. (Q) reflects the data (D) inputs while the gate (G) and gate enable (GE) are High, and (CLR) is Low. If (GE) is Low, data on (D) cannot be latched. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) or (GE) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs
CLR	GE	G	Dn	Qn
1	X	X	X	0
0	0	X	X	No Change
0	1	1	Dn	Dn
0	1	0	X	No Change
0	1	↓	Dn	Dn

Design Entry Method

This design element is only for use in schematics.

Available Attributes

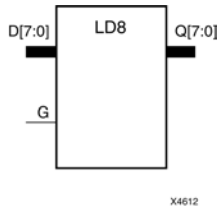
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	Any 4-Bit Value	All zeros	Sets the initial value of Q output after configuration

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LD8

Macro: Multiple Transparent Data Latch



Introduction

This design element has 8 transparent data latches with a common gate enable (G). The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is High. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs		Outputs
G	D	Q
1	Dn	Dn
0	X	No Change
↓	Dn	Dn

Design Entry Method

This design element is only for use in schematics.

Available Attributes

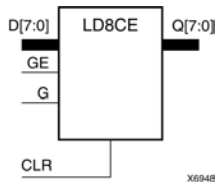
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	Any 8-Bit Value	All zeros	Sets the initial value of Q output after configuration

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LD8CE

Macro: Transparent Data Latch with Asynchronous Clear and Gate Enable



Introduction

This design element has 8 transparent data latches with asynchronous clear and gate enable. When the asynchronous clear input (CLR) is High, it overrides the other inputs and resets the data (Q) outputs Low. (Q) reflects the data (D) inputs while the gate (G) and gate enable (GE) are High, and (CLR) is Low. If (GE) is Low, data on (D) cannot be latched. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) or (GE) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs
CLR	GE	G	Dn	Qn
1	X	X	X	0
0	0	X	X	No Change
0	1	1	Dn	Dn
0	1	0	X	No Change
0	1	↓	Dn	Dn

Design Entry Method

This design element is only for use in schematics.

Available Attributes

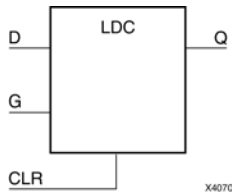
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	Any 8-Bit Value	All zeros	Sets the initial value of Q output after configuration.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LDC

Primitive: Macro: Transparent Data Latch with Asynchronous Clear



Introduction

This design element is a transparent data latch with asynchronous clear. When the asynchronous clear input (CLR) is High, it overrides the other inputs and resets the data (Q) output Low. (Q) reflects the data (D) input while the gate enable (G) input is High and (CLR) is Low. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
CLR	G	D	Q
1	X	X	0
0	1	D	D
0	0	X	No Change
0	↓	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

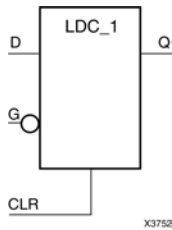
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LDC_1

Primitive: Transparent Data Latch with Asynchronous Clear and Inverted Gate



Introduction

This design element is a transparent data latch with asynchronous clear and inverted gate. When the asynchronous clear input (CLR) is High, it overrides the other inputs (D and G) and resets the data (Q) output Low. (Q) reflects the data (D) input while the gate enable (G) input and CLR are Low. The data on the (D) input during the Low-to-High gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains High.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
CLR	G	D	Q
1	X	X	0
0	0	D	D
0	1	X	No Change
0	↑	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

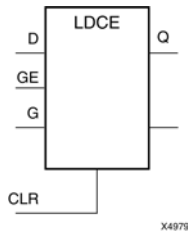
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LDCE

Primitive: Transparent Data Latch with Asynchronous Clear and Gate Enable



Introduction

This design element is a transparent data latch with asynchronous clear and gate enable. When the asynchronous clear input (CLR) is High, it overrides the other inputs and resets the data (Q) output Low. Q reflects the data (D) input while the gate (G) input and gate enable (GE) are High and CLR is Low. If (GE) is Low, data on (D) cannot be latched. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) or (GE) remains low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs
CLR	GE	G	D	Q
1	X	X	X	0
0	0	X	X	No Change
0	1	1	D	D
0	1	0	X	No Change
0	1	↓	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

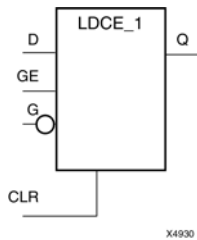
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LDCE_1

Primitive: Transparent Data Latch with Asynchronous Clear, Gate Enable, and Inverted Gate



Introduction

This design element is a transparent data latch with asynchronous clear, gate enable, and inverted gate. When the asynchronous clear input (CLR) is High, it overrides the other inputs and resets the data (Q) output Low. (Q) reflects the data (D) input while the gate (G) input and (CLR) are Low and gate enable (GE) is High. The data on the (D) input during the Low-to-High gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains High or (GE) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs				Outputs
CLR	GE	G	D	Q
1	X	X	X	0
0	0	X	X	No Change
0	1	0	D	D
0	1	1	X	No Change
0	1	↑	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

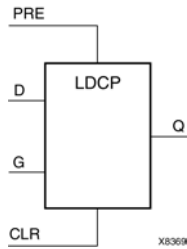
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LDCP

Primitive: Transparent Data Latch with Asynchronous Clear and Preset



Introduction

The design element is a transparent data latch with data (D), asynchronous clear (CLR) and preset (PRE) inputs. When CLR is High, it overrides the other inputs and resets the data (Q) output Low. When PRE is High and CLR is low, it presets the data (Q) output High. Q reflects the data (D) input while the gate (G) input is High and CLR and PRE are Low. The data on the D input during the High-to-Low gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs
CLR	PRE	G	D	Q
1	X	X	X	0
0	1	X	X	1
0	0	1	D	D
0	0	0	X	No Change
0	0	↓	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

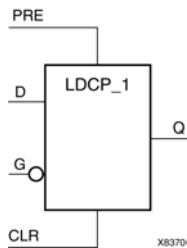
Attribute	Type	Allowed Values	Default	Description
INIT	Integer	0, 1	0	Specifies the initial value upon power-up or the assertion of GSR for the (Q) port.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LDCP_1

Primitive: Transparent Data Latch with Asynchronous Clear and Preset and Inverted Gate



Introduction

This design element is a transparent data latch with data (D), asynchronous clear (CLR), preset (PRE) inputs, and inverted gate (G). When (CLR) is High, it overrides the other inputs and resets the data (Q) output Low. When (PRE) is High and (CLR) is Low, it presets the data (Q) output High. (Q) reflects the data (D) input while gate (G) input, (CLR), and (PRE) are Low. The data on the (D) input during the Low-to-High gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains High.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs				Outputs
CLR	PRE	G	D	Q
1	X	X	X	0
0	1	X	X	1
0	0	0	D	D
0	0	1	X	No Change
0	0	↑	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

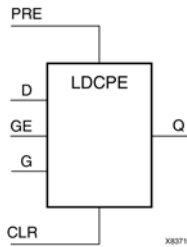
Attribute	Type	Allowed Values	Default	Description
INIT	Integer	0, 1	0	Specifies the initial value upon power-up or the assertion of GSR for the (Q) port.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LDCPE

Primitive: Transparent Data Latch with Asynchronous Clear and Preset and Gate Enable



Introduction

This design element is a transparent data latch with data (D), asynchronous clear (CLR), asynchronous preset (PRE), and gate enable (GE). When (CLR) is High, it overrides the other inputs and resets the data (Q) output Low. When (PRE) is High and (CLR) is Low, it presets the data (Q) output High. Q reflects the data (D) input while the gate (G) input and gate enable (GE) are High and (CLR) and PRE are Low. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the Q output remains unchanged as long as (G) or (GE) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs					Outputs
CLR	PRE	GE	G	D	Q
1	X	X	X	X	0
0	1	X	X	X	1
0	0	0	X	X	No Change
0	0	1	1	0	0
0	0	1	1	1	1
0	0	1	0	X	No Change
0	0	1	↓	D	D

Port Descriptions

Port	Direction	Width	Function
Q	Output	1	Data Output
CLR	Input	1	Asynchronous clear/reset input
D	Input	1	Data Input
G	Input	1	Gate Input
GE	Input	1	Gate Enable Input
PRE	Input	1	Asynchronous preset/set input

Design Entry Method

This design element can be used in schematics.

Available Attributes

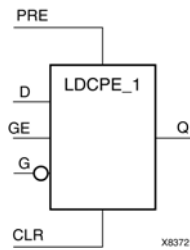
Attribute	Type	Allowed Values	Default	Description
INIT	Integer	0, 1	0	Sets the initial value of Q output after configuration.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LDCPE_1

Primitive: Transparent Data Latch with Asynchronous Clear and Preset, Gate Enable, and Inverted Gate



Introduction

This design element is a transparent data latch with data (D), asynchronous clear (CLR), asynchronous preset (PRE), gate enable (GE), and inverted gate (G). When (CLR) is High, it overrides the other inputs and resets the data (Q) output Low. When PRE is High and (CLR) is Low, it presets the data (Q) output High. (Q) reflects the data (D) input while gate enable (GE) is High and gate (G), (CLR), and (PRE) are Low. The data on the (D) input during the Low-to-High gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) is High or (GE) is Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs					Outputs
CLR	PRE	GE	G	D	Q
1	X	X	X	X	0
0	1	X	X	X	1
0	0	0	X	X	No Change
0	0	1	0	D	D
0	0	1	1	X	No Change
0	0	1	↑	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

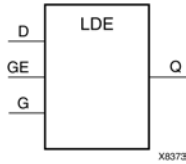
Attribute	Type	Allowed Values	Default	Description
INIT	Integer	0, 1	0	Specifies the initial value upon power-up or the assertion of GSR for the (Q) port.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LDE

Primitive: Transparent Data Latch with Gate Enable



Introduction

This design element is a transparent data latch with data (D) and gate enable (GE) inputs. Output (Q) reflects the data (D) while the gate (G) input and gate enable (GE) are High. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) or (GE) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
GE	G	D	Q
0	X	X	No Change
1	1	D	D
1	0	X	No Change
1	↓	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

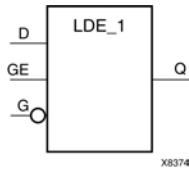
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Specifies the initial value upon power-up or the assertion of GSR for the (Q) port.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LDE_1

Primitive: Transparent Data Latch with Gate Enable and Inverted Gate



Introduction

This design element is a transparent data latch with data (D), gate enable (GE), and inverted gate (G). Output (Q) reflects the data (D) while the gate (G) input is Low and gate enable (GE) is High. The data on the (D) input during the Low-to-High gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) is High or (GE) is Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs
GE	G	D	Q
0	X	X	No Change
1	0	D	D
1	1	X	No Change
1	↑	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

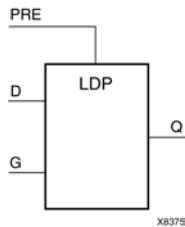
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Specifies the initial value upon power-up or the assertion of GSR for the (Q) port.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LDP

Primitive: Macro: Transparent Data Latch with Asynchronous Preset



Introduction

This design element is a transparent data latch with asynchronous preset (PRE). When PRE is High it overrides the other inputs and presets the data (Q) output High. Q reflects the data (D) input while gate (G) input is High and PRE is Low. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains Low.

The latch is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
PRE	G	D	Q
1	X	X	1
0	1	0	0
0	1	1	1
0	0	X	No Change
0	↓	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

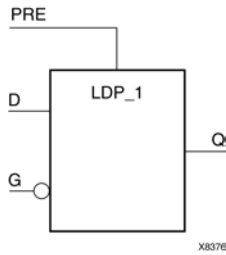
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Specifies the initial value upon power-up or the assertion of GSR for the Q port.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LDP_1

Primitive: Transparent Data Latch with Asynchronous Preset and Inverted Gate



Introduction

This design element is a transparent data latch with asynchronous preset (PRE) and inverted gate (G). When the (PRE) input is High, it overrides the other inputs and presets the data (Q) output High. (Q) reflects the data (D) input while gate (G) input and (PRE) are Low. The data on the (D) input during the Low-to-High gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains High.

The latch is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs
PRE	G	D	Q
1	X	X	1
0	0	D	D
0	1	X	No Change
0	↑	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

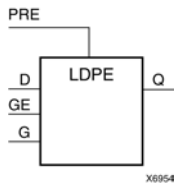
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Specifies the initial value upon power-up or the assertion of GSR for the (Q) port.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LDPE

Primitive: Transparent Data Latch with Asynchronous Preset and Gate Enable



Introduction

This design element is a transparent data latch with asynchronous preset and gate enable. When the asynchronous preset (PRE) is High, it overrides the other input and presets the data (Q) output High. Q reflects the data (D) input while the gate (G) input and gate enable (GE) are High. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) or (GE) remains Low.

The latch is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs
PRE	GE	G	D	Q
1	X	X	X	1
0	0	X	X	No Change
0	1	1	D	D
0	1	0	X	No Change
0	1	↓	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

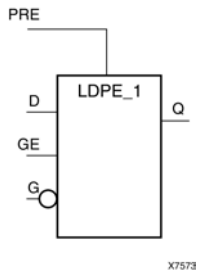
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Specifies the initial value upon power-up or the assertion of GSR for the (Q) port.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LDPE_1

Primitive: Transparent Data Latch with Asynchronous Preset, Gate Enable, and Inverted Gate



Introduction

This design element is a transparent data latch with asynchronous preset, gate enable, and inverted gate. When the asynchronous preset (PRE) is High, it overrides the other input and presets the data (Q) output High. (Q) reflects the data (D) input while the gate (G) and (PRE) are Low and gate enable (GE) is High. The data on the (D) input during the Low-to-High gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains High or (GE) remains Low.

The latch is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs				Outputs
PRE	GE	G	D	Q
1	X	X	X	1
0	0	X	X	No Change
0	1	0	D	D
0	1	1	X	No Change
0	1	↑	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

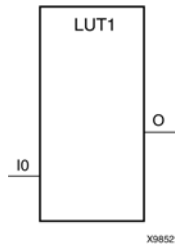
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Specifies the initial value upon power-up or the assertion of GSR for the (Q) port.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LUT1

Macro: 1-Bit Look-Up Table with General Output



Introduction

This design element is a 1-bit look-up table (LUT) with general output (O).

An INIT attribute with an appropriate number of hexadecimal digits for the number of inputs must be attached to the LUT to specify its function. This element provides a look-up table version of a buffer or inverter. These elements are the basic building blocks. Two LUTs are available in each CLB slice; four LUTs are available in each CLB. Multiple variants of LUTs accommodate additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs	Outputs
I0	O
0	INIT[0]
1	INIT[1]
INIT = Binary number assigned to the INIT attribute	

Design Entry Method

This design element can be used in schematics.

Available Attributes

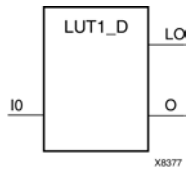
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 2-Bit Value	All zeros	Initializes look-up tables.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LUT1_D

Macro: 1-Bit Look-Up Table with Dual Output



Introduction

This design element is a 1-bit look-up table (LUT) with two functionally identical outputs, O and LO. It provides a look-up table version of a buffer or inverter.

The O output is a general interconnect. The LO output is used to connect to another output within the same CLB slice and to the fast connect buffer. A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs	Outputs	
I0	O	LO
0	INIT[0]	INIT[0]
1	INIT[1]	INIT[1]
INIT = Binary number assigned to the INIT attribute		

Design Entry Method

This design element can be used in schematics.

Available Attributes

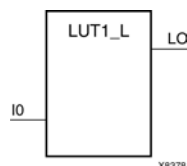
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 2-Bit Value	All zeros	Initializes look-up tables.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LUT1_L

Macro: 1-Bit Look-Up Table with Local Output



Introduction

This design element is a 1-bit look-up table (LUT) with a local output (LO) that is used to connect to another output within the same CLB slice and to the fast connect buffer. It provides a look-up table version of a buffer or inverter.

A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs	Outputs
IO	LO
0	INIT[0]
1	INIT[1]
INIT = Binary number assigned to the INIT attribute	

Design Entry Method

This design element can be used in schematics.

Available Attributes

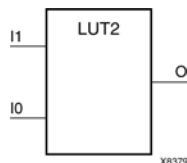
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 2-Bit Value	All zeros	Initializes look-up tables.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LUT2

Macro: 2-Bit Look-Up Table with General Output



Introduction

This design element is a 2-bit look-up table (LUT) with general output (O).

An INIT attribute with an appropriate number of hexadecimal digits for the number of inputs must be attached to the LUT to specify its function. This element provides a look-up table version of a buffer or inverter. These elements are the basic building blocks. Two LUTs are available in each CLB slice; four LUTs are available in each CLB. Multiple variants of LUTs accommodate additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs		Outputs
I1	I0	O
0	0	INIT[0]
0	1	INIT[1]
1	0	INIT[2]
1	1	INIT[3]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute		

Design Entry Method

This design element can be used in schematics.

Available Attributes

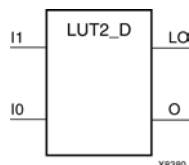
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 4-Bit Value	All zeros	Initializes look-up tables.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LUT2_D

Macro: 2-Bit Look-Up Table with Dual Output



Introduction

This design element is a 2-bit look-up table (LUT) with two functionally identical outputs, O and LO.

The O output is a general interconnect. The LO output is used to connect to another output within the same CLB slice and to the fast connect buffer. A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The LogicTable Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs		Outputs	
I1	I0	O	LO
0	0	INIT[0]	INIT[0]
0	1	INIT[1]	INIT[1]
1	0	INIT[2]	INIT[2]
1	1	INIT[3]	INIT[3]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute			

Design Entry Method

This design element can be used in schematics.

Available Attributes

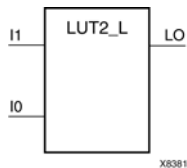
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 4-Bit Value	All zeros	Initializes look-up tables.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LUT2_L

Macro: 2-Bit Look-Up Table with Local Output



Introduction

This design element is a 2-bit look-up table (LUT) with a local output (LO) that is used to connect to another output within the same CLB slice and to the fast connect buffer. It provides a look-up table version of a buffer or inverter.

A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs		Outputs
I1	I0	LO
0	0	INIT[0]
0	1	INIT[1]
1	0	INIT[2]
1	1	INIT[3]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute		

Design Entry Method

This design element can be used in schematics.

Available Attributes

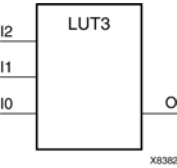
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 4-Bit Value	All zeros	Initializes look-up tables.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LUT3

Macro: 3-Bit Look-Up Table with General Output



Introduction

This design element is a 3-bit look-up table (LUT) with general output (O). A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

An INIT attribute with an appropriate number of hexadecimal digits for the number of inputs must be attached to the LUT to specify its function. This element provides a look-up table version of a buffer or inverter. These elements are the basic building blocks. Two LUTs are available in each CLB slice; four LUTs are available in each CLB. Multiple variants of LUTs accommodate additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs			Outputs
I2	I1	I0	O
0	0	0	INIT[0]
0	0	1	INIT[1]
0	1	0	INIT[2]
0	1	1	INIT[3]
1	0	0	INIT[4]
1	0	1	INIT[5]
1	1	0	INIT[6]
1	1	1	INIT[7]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute			

Design Entry Method

This design element can be used in schematics.

Available Attributes

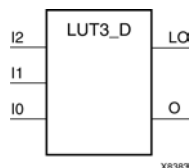
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 8-Bit Value	All zeros	Initializes look-up tables.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LUT3_D

Macro: 3-Bit Look-Up Table with Dual Output



Introduction

This design element is a 3-bit look-up table (LUT) with two functionally identical outputs, O and LO.

The O output is a general interconnect. The LO output is used to connect to another output within the same CLB slice and to the fast connect buffer. A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs			Outputs	
I2	I1	I0	O	LO
0	0	0	INIT[0]	INIT[0]
0	0	1	INIT[1]	INIT[1]
0	1	0	INIT[2]	INIT[2]
0	1	1	INIT[3]	INIT[3]
1	0	0	INIT[4]	INIT[4]
1	0	1	INIT[5]	INIT[5]
1	1	0	INIT[6]	INIT[6]
1	1	1	INIT[7]	INIT[7]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute				

Design Entry Method

This design element can be used in schematics.

Available Attributes

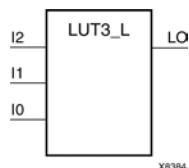
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 8-Bit Value	All zeros	Initializes look-up tables.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LUT3_L

Macro: 3-Bit Look-Up Table with Local Output



Introduction

This design element is a 3-bit look-up table (LUT) with a local output (LO) that is used to connect to another output within the same CLB slice and to the fast connect buffer. It provides a look-up table version of a buffer or inverter.

A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs			Outputs
I2	I1	I0	LO
0	0	0	INIT[0]
0	0	1	INIT[1]
0	1	0	INIT[2]
0	1	1	INIT[3]
1	0	0	INIT[4]
1	0	1	INIT[5]
1	1	0	INIT[6]
1	1	1	INIT[7]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute			

Design Entry Method

This design element can be used in schematics.

Available Attributes

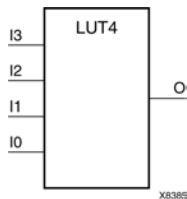
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 8-Bit Value	All zeros	Initializes look-up tables.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LUT4

Macro: 4-Bit Look-Up-Table with General Output



Introduction

This design element is a 4-bit look-up table (LUT) with general output (O).

An INIT attribute with an appropriate number of hexadecimal digits for the number of inputs must be attached to the LUT to specify its function. This element provides a look-up table version of a buffer or inverter. These elements are the basic building blocks. Two LUTs are available in each CLB slice; four LUTs are available in each CLB. Multiple variants of LUTs accommodate additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs				Outputs
I3	I2	I1	I0	O
0	0	0	0	INIT[0]
0	0	0	1	INIT[1]
0	0	1	0	INIT[2]
0	0	1	1	INIT[3]
0	1	0	0	INIT[4]
0	1	0	1	INIT[5]
0	1	1	0	INIT[6]
0	1	1	1	INIT[7]
1	0	0	0	INIT[8]
1	0	0	1	INIT[9]
1	0	1	0	INIT[10]
1	0	1	1	INIT[11]
1	1	0	0	INIT[12]
1	1	0	1	INIT[13]
1	1	1	0	INIT[14]
1	1	1	1	INIT[15]

INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute

Design Entry Method

This design element can be used in schematics.

Available Attributes

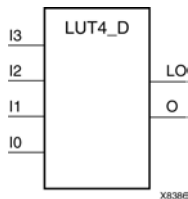
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Initializes look-up tables.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LUT4_D

Macro: 4-Bit Look-Up Table with Dual Output



Introduction

This design element is a 4-bit look-up table (LUT) with two functionally identical outputs, O and LO

The O output is a general interconnect. The LO output is used to connect to another output within the same CLB slice and to the fast connect buffer. A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs				Outputs	
I3	I2	I1	I0	O	LO
0	0	0	0	INIT[0]	INIT[0]
0	0	0	1	INIT[1]	INIT[1]
0	0	1	0	INIT[2]	INIT[2]
0	0	1	1	INIT[3]	INIT[3]
0	1	0	0	INIT[4]	INIT[4]
0	1	0	1	INIT[5]	INIT[5]
0	1	1	0	INIT[6]	INIT[6]
0	1	1	1	INIT[7]	INIT[7]
1	0	0	0	INIT[8]	INIT[8]
1	0	0	1	INIT[9]	INIT[9]
1	0	1	0	INIT[10]	INIT[10]
1	0	1	1	INIT[11]	INIT[11]
1	1	0	0	INIT[12]	INIT[12]
1	1	0	1	INIT[13]	INIT[13]
1	1	1	0	INIT[14]	INIT[14]
1	1	1	1	INIT[15]	INIT[15]

INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute

Design Entry Method

This design element can be used in schematics.

Available Attributes

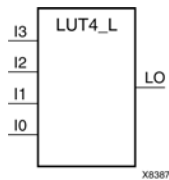
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Initializes look-up tables.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LUT4_L

Macro: 4-Bit Look-Up Table with Local Output



Introduction

This design element is a 4-bit look-up table (LUT) with a local output (LO) that is used to connect to another output within the same CLB slice and to the fast connect buffer. It provides a look-up table version of a buffer or inverter.

A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs				Outputs
I3	I2	I1	I0	LO
0	0	0	0	INIT[0]
0	0	0	1	INIT[1]
0	0	1	0	INIT[2]
0	0	1	1	INIT[3]
0	1	0	0	INIT[4]
0	1	0	1	INIT[5]
0	1	1	0	INIT[6]
0	1	1	1	INIT[7]
1	0	0	0	INIT[8]
1	0	0	1	INIT[9]
1	0	1	0	INIT[10]
1	0	1	1	INIT[11]
1	1	0	0	INIT[12]
1	1	0	1	INIT[13]
1	1	1	0	INIT[14]
1	1	1	1	INIT[15]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute				

Design Entry Method

This design element can be used in schematics.

Available Attributes

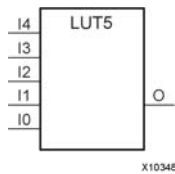
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Initializes look-up tables.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LUT5

Primitive: 5-Input Lookup Table with General Output



Introduction

This design element is a 5-input, 1-output look-up table (LUT) that can either act as an asynchronous 32-bit ROM (with 5-bit addressing) or implement any 5-input logic function. LUTs are the basic logic building blocks and are used to implement most logic functions of the design. One LUT5 is packed into a LUT6 within a slice, or two LUT5s can be packed into a single LUT6 with some restrictions. The functionality of the LUT5, LUT5_L and LUT5_D is the same. However, the LUT5_L and LUT5_D allow the additional specification to connect the LUT5 output signal to an internal slice or CLB connection using the LO output. The LUT5_L specifies that the only connections from the LUT5 will be within a slice or CLB, while the LUT5_D allows the specification to connect the output of the LUT to both inter-slice/CLB logic and external logic as well. The LUT5 does not state any specific output connections and should be used in all cases except where internal slice or CLB signal connections must be implicitly specified.

An INIT attribute consisting of a 32-bit hexadecimal value must be specified to indicate the LUTs logical function. The INIT value is calculated by assigning a 1 to the corresponding INIT bit value when the associated inputs are applied. For instance, a Verilog INIT value of 32'h80000000 (X"80000000" for VHDL) makes the output zero unless all of the inputs are one (a 5-input AND gate). A Verilog INIT value of 32'hfffffffe (X"FFFFFFFE" for VHDL) makes the output one unless all zeros are on the inputs (a 5-input OR gate).

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs					Outputs
I4	I3	I2	I1	I0	LO
0	0	0	0	0	INIT[0]
0	0	0	0	1	INIT[1]
0	0	0	1	0	INIT[2]
0	0	0	1	1	INIT[3]
0	0	1	0	0	INIT[4]
0	0	1	0	1	INIT[5]
0	0	1	1	0	INIT[6]
0	0	1	1	1	INIT[7]
0	1	0	0	0	INIT[8]
0	1	0	0	1	INIT[9]
0	1	0	1	0	INIT[10]
0	1	0	1	1	INIT[11]
0	1	1	0	0	INIT[12]
0	1	1	0	1	INIT[13]
0	1	1	1	0	INIT[14]
0	1	1	1	1	INIT[15]
1	0	0	0	0	INIT[16]
1	0	0	0	1	INIT[17]
1	0	0	1	0	INIT[18]
1	0	0	1	1	INIT[19]
1	0	1	0	0	INIT[20]
1	0	1	0	1	INIT[21]
1	0	1	1	0	INIT[22]
1	0	1	1	1	INIT[23]
1	1	0	0	0	INIT[24]
1	1	0	0	1	INIT[25]
1	1	0	1	0	INIT[26]
1	1	0	1	1	INIT[27]
1	1	1	0	0	INIT[28]
1	1	1	0	1	INIT[29]
1	1	1	1	0	INIT[30]
1	1	1	1	1	INIT[31]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute					

Port Description

Name	Direction	Width	Function
O	Output	1	5-LUT output
I0, I1, I2, I3, I4	Input	1	LUT inputs

Design Entry Method

This design element can be used in schematics.

Available Attributes

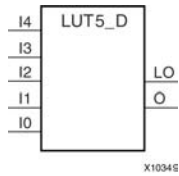
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 32-Bit Value	All zeros	Specifies the logic value for the look-up tables.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LUT5_D

Primitive: 5-Input Lookup Table with General and Local Outputs



Introduction

This design element is a 5-input, 1-output look-up table (LUT) that can either act as an asynchronous 32-bit ROM (with 5-bit addressing) or implement any 5-input logic function. LUTs are the basic logic building blocks and are used to implement most logic functions of the design. One LUT5 will be packed into a LUT6 within a slice, or two LUT5s can be packed into a single LUT6 with some restrictions. The functionality of the LUT5, LUT5_L and LUT5_D is the same. However, the LUT5_L and LUT5_D allow the additional specification to connect the LUT5 output signal to an internal slice or CLB connection using the LO output. The LUT5_L specifies that the only connections from the LUT5 will be within a slice or CLB, while the LUT5_D allows the specification to connect the output of the LUT to both inter-slice/CLB logic and external logic as well. The LUT5 does not state any specific output connections and should be used in all cases except where internal slice or CLB signal connections must be implicitly specified.

An INIT attribute consisting of a 32-bit hexadecimal value must be specified to indicate the LUTs logical function. The INIT value is calculated by assigning a 1 to the corresponding INIT bit value when the associated inputs are applied. For instance, a Verilog INIT value of 32'h80000000 (X"80000000" for VHDL) will make the output zero unless all of the inputs are one (a 5-input AND gate). A Verilog INIT value of 32'hfffffffe (X"FFFFFFFE" for VHDL) will make the output one unless all zeros are on the inputs (a 5-input OR gate).

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs					Outputs	
I4	I3	I2	I1	I0	O	LO
0	0	0	0	0	INIT[0]	INIT[0]
0	0	0	0	1	INIT[1]	INIT[1]
0	0	0	1	0	INIT[2]	INIT[2]
0	0	0	1	1	INIT[3]	INIT[3]
0	0	1	0	0	INIT[4]	INIT[4]
0	0	1	0	1	INIT[5]	INIT[5]
0	0	1	1	0	INIT[6]	INIT[6]
0	0	1	1	1	INIT[7]	INIT[7]
0	1	0	0	0	INIT[8]	INIT[8]
0	1	0	0	1	INIT[9]	INIT[9]
0	1	0	1	0	INIT[10]	INIT[10]
0	1	0	1	1	INIT[11]	INIT[11]
0	1	1	0	0	INIT[12]	INIT[12]
0	1	1	0	1	INIT[13]	INIT[13]
0	1	1	1	0	INIT[14]	INIT[14]
0	1	1	1	1	INIT[15]	INIT[15]
1	0	0	0	0	INIT[16]	INIT[16]
1	0	0	0	1	INIT[17]	INIT[17]
1	0	0	1	0	INIT[18]	INIT[18]
1	0	0	1	1	INIT[19]	INIT[19]
1	0	1	0	0	INIT[20]	INIT[20]
1	0	1	0	1	INIT[21]	INIT[21]
1	0	1	1	0	INIT[22]	INIT[22]
1	0	1	1	1	INIT[23]	INIT[23]
1	1	0	0	0	INIT[24]	INIT[24]
1	1	0	0	1	INIT[25]	INIT[25]
1	1	0	1	0	INIT[26]	INIT[26]
1	1	0	1	1	INIT[27]	INIT[27]
1	1	1	0	0	INIT[28]	INIT[28]
1	1	1	0	1	INIT[29]	INIT[29]
1	1	1	1	0	INIT[30]	INIT[30]
1	1	1	1	1	INIT[31]	INIT[31]

INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute

Port Description

Name	Direction	Width	Function
O	Output	1	5-LUT output
L0	Output	1	5-LUT output for internal CLB connection
I0, I1, I2, I3, I4	Input	1	LUT inputs

Design Entry Method

This design element can be used in schematics.

Available Attributes

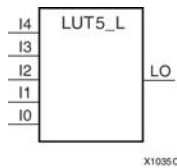
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 32-Bit Value	All zeros	Specifies the logic value for the look-up tables.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LUT5_L

Primitive: 5-Input Lookup Table with Local Output



Introduction

This design element is a 5-input, 1-output look-up table (LUT) that can either act as an asynchronous 32-bit ROM (with 5-bit addressing) or implement any 5-input logic function. LUTs are the basic logic building blocks and are used to implement most logic functions of the design. One LUT5 will be packed into a LUT6 within a slice, or two LUT5s can be packed into a single LUT6 with some restrictions. The functionality of the LUT5, LUT5_L and LUT5_D is the same. However, the LUT5_L and LUT5_D allow the additional specification to connect the LUT5 output signal to an internal slice or CLB connection using the LO output. The LUT5_L specifies that the only connections from the LUT5 is within a slice or CLB, while the LUT5_D allows the specification to connect the output of the LUT to both inter-slice/CLB logic and external logic as well. The LUT5 does not state any specific output connections and should be used in all cases except where internal slice or CLB signal connections must be implicitly specified.

An INIT attribute consisting of a 32-bit hexadecimal value must be specified to indicate the LUTs logical function. The INIT value is calculated by assigning a 1 to the corresponding INIT bit value when the associated inputs are applied. For instance, a Verilog INIT value of 32'h80000000 (X"80000000" for VHDL) makes the output zero unless all of the inputs are one (a 5-input AND gate). A Verilog INIT value of 32'hfffffffe (X"FFFFFFFE" for VHDL) makes the output one unless all zeros are on the inputs (a 5-input OR gate).

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary truth table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed logic value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs					Outputs
I4	I3	I2	I1	I0	LO
0	0	0	0	0	INIT[0]
0	0	0	0	1	INIT[1]
0	0	0	1	0	INIT[2]
0	0	0	1	1	INIT[3]
0	0	1	0	0	INIT[4]
0	0	1	0	1	INIT[5]
0	0	1	1	0	INIT[6]
0	0	1	1	1	INIT[7]
0	1	0	0	0	INIT[8]
0	1	0	0	1	INIT[9]
0	1	0	1	0	INIT[10]
0	1	0	1	1	INIT[11]
0	1	1	0	0	INIT[12]
0	1	1	0	1	INIT[13]
0	1	1	1	0	INIT[14]
0	1	1	1	1	INIT[15]
1	0	0	0	0	INIT[16]
1	0	0	0	1	INIT[17]
1	0	0	1	0	INIT[18]
1	0	0	1	1	INIT[19]
1	0	1	0	0	INIT[20]
1	0	1	0	1	INIT[21]
1	0	1	1	0	INIT[22]
1	0	1	1	1	INIT[23]
1	1	0	0	0	INIT[24]
1	1	0	0	1	INIT[25]
1	1	0	1	0	INIT[26]
1	1	0	1	1	INIT[27]
1	1	1	0	0	INIT[28]
1	1	1	0	1	INIT[29]
1	1	1	1	0	INIT[30]
1	1	1	1	1	INIT[31]

INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute

Port Description

Name	Direction	Width	Function
L0	Output	1	6/5-LUT output for internal CLB connection
I0, I1, I2, I3, I4	Input	1	LUT inputs

Design Entry Method

This design element can be used in schematics.

Available Attributes

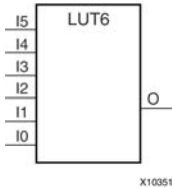
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 32-Bit Value	All zeros	Specifies the logic value for the look-up tables.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LUT6

Primitive: 6-Input Lookup Table with General Output



Introduction

This design element is a 6-input, 1-output look-up table (LUT) that can either act as an asynchronous 64-bit ROM (with 6-bit addressing) or implement any 6-input logic function. LUTs are the basic logic building blocks and are used to implement most logic functions of the design. A LUT6 is mapped to one of the four look-up tables in the slice. The functionality of the LUT6, LUT6_L and LUT6_D is the same. However, the LUT6_L and LUT6_D allow the additional specification to connect the LUT6 output signal to an internal slice, or CLB connection, using the LO output. The LUT6_L specifies that the only connections from the LUT6 will be within a slice, or CLB, while the LUT6_D allows the specification to connect the output of the LUT to both inter-slice/CLB logic and external logic as well. The LUT6 does not state any specific output connections and should be used in all cases except where internal slice or CLB signal connections must be implicitly specified.

An INIT attribute consisting of a 64-bit Hexadecimal value must be specified to indicate the LUTs logical function. The INIT value is calculated by assigning a 1 to corresponding INIT bit value when the associated inputs are applied. For instance, a Verilog INIT value of 64'h8000000000000000 (X"8000000000000000" for VHDL) makes the output zero unless all of the inputs are one (a 6-input AND gate). A Verilog INIT value of 64'hffffffffffff (X"FFFFFFFFFFFFFFFF" for VHDL) makes the output one unless all zeros are on the inputs (a 6-input OR gate).

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs						Outputs
I5	I4	I3	I2	I1	I0	O
0	0	0	0	0	0	INIT[0]
0	0	0	0	0	1	INIT[1]
0	0	0	0	1	0	INIT[2]
0	0	0	0	1	1	INIT[3]
0	0	0	1	0	0	INIT[4]
0	0	0	1	0	1	INIT[5]
0	0	0	1	1	0	INIT[6]
0	0	0	1	1	1	INIT[7]

Inputs						Outputs
I5	I4	I3	I2	I1	I0	O
0	0	1	0	0	0	INIT[8]
0	0	1	0	0	1	INIT[9]
0	0	1	0	1	0	INIT[10]
0	0	1	0	1	1	INIT[11]
0	0	1	1	0	0	INIT[12]
0	0	1	1	0	1	INIT[13]
0	0	1	1	1	0	INIT[14]
0	0	1	1	1	1	INIT[15]
0	1	0	0	0	0	INIT[16]
0	1	0	0	0	1	INIT[17]
0	1	0	0	1	0	INIT[18]
0	1	0	0	1	1	INIT[19]
0	1	0	1	0	0	INIT[20]
0	1	0	1	0	1	INIT[21]
0	1	0	1	1	0	INIT[22]
0	1	0	1	1	1	INIT[23]
0	1	1	0	0	0	INIT[24]
0	1	1	0	0	1	INIT[25]
0	1	1	0	1	0	INIT[26]
0	1	1	0	1	1	INIT[27]
0	1	1	1	0	0	INIT[28]
0	1	1	1	0	1	INIT[29]
0	1	1	1	1	0	INIT[30]
0	1	1	1	1	1	INIT[31]
1	0	0	0	0	0	INIT[32]
1	0	0	0	0	1	INIT[33]
1	0	0	0	1	0	INIT[34]
1	0	0	0	1	1	INIT[35]
1	0	0	1	0	0	INIT[36]
1	0	0	1	0	1	INIT[37]
1	0	0	1	1	0	INIT[38]
1	0	0	1	1	1	INIT[39]
1	0	1	0	0	0	INIT[40]
1	0	1	0	0	1	INIT[41]
1	0	1	0	1	0	INIT[42]
1	0	1	0	1	1	INIT[43]
1	0	1	1	0	0	INIT[44]
1	0	1	1	0	1	INIT[45]

Inputs						Outputs
I5	I4	I3	I2	I1	I0	O
1	0	1	1	1	0	INIT[46]
1	0	1	1	1	1	INIT[47]
1	1	0	0	0	0	INIT[48]
1	1	0	0	0	1	INIT[49]
1	1	0	0	1	0	INIT[50]
1	1	0	0	1	1	INIT[51]
1	1	0	1	0	0	INIT[52]
1	1	0	1	0	1	INIT[53]
1	1	0	1	1	0	INIT[54]
1	1	0	1	1	1	INIT[55]
1	1	1	0	0	0	INIT[56]
1	1	1	0	0	1	INIT[57]
1	1	1	0	1	0	INIT[58]
1	1	1	0	1	1	INIT[59]
1	1	1	1	0	0	INIT[60]
1	1	1	1	0	1	INIT[61]
1	1	1	1	1	0	INIT[62]
1	1	1	1	1	1	INIT[63]

INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute

Port Description

Name	Direction	Width	Function
O	Output	1	6/5-LUT output
I0, I1, I2, I3, I4, I5	Input	1	LUT inputs

Design Entry Method

This design element can be used in schematics.

Available Attributes

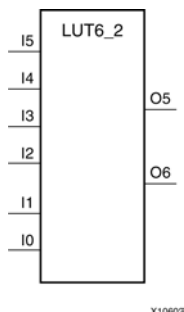
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 64-Bit Value	All zeros	Specifies the logic value for the look-up tables.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LUT6_2

Primitive: Six-input, 2-output, Look-Up Table



Introduction

This design element is a 6-input, 2-output look-up table (LUT) that can either act as a dual asynchronous 32-bit ROM (with 5-bit addressing), implement any two 5-input logic functions with shared inputs, or implement a 6-input logic function and a 5-input logic function with shared inputs and shared logic values. LUTs are the basic logic building blocks and are used to implement most logic functions of the design. A LUT6_2 will be mapped to one of the four look-up tables in the slice.

An INIT attribute consisting of a 64-bit hexadecimal value must be specified to indicate the LUTs logical function. The INIT value is calculated by assigning a 1 to corresponding INIT bit value when the associated inputs are applied. For instance, a Verilog INIT value of 64'hffffffffffffe (X"FFFFFFFFFFFFFFFE" for VHDL) makes the O6 output 1 unless all zeros are on the inputs and the O5 output a 1, or unless I[4:0] are all zeroes (a 5-input and 6-input OR gate). The lower half (bits 31:0) of the INIT values apply to the logic function of the O5 output.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs						Outputs	
I5	I4	I3	I2	I1	I0	O5	O6
0	0	0	0	0	0	INIT[0]	INIT[0]
0	0	0	0	0	1	INIT[1]	INIT[1]
0	0	0	0	1	0	INIT[2]	INIT[2]
0	0	0	0	1	1	INIT[3]	INIT[3]
0	0	0	1	0	0	INIT[4]	INIT[4]
0	0	0	1	0	1	INIT[5]	INIT[5]
0	0	0	1	1	0	INIT[6]	INIT[6]
0	0	0	1	1	1	INIT[7]	INIT[7]

Inputs						Outputs	
0	0	1	0	0	0	INIT[8]	INIT[8]
0	0	1	0	0	1	INIT[9]	INIT[9]
0	0	1	0	1	0	INIT[10]	INIT[10]
0	0	1	0	1	1	INIT[11]	INIT[11]
0	0	1	1	0	0	INIT[12]	INIT[12]
0	0	1	1	0	1	INIT[13]	INIT[13]
0	0	1	1	1	0	INIT[14]	INIT[14]
0	0	1	1	1	1	INIT[15]	INIT[15]
0	1	0	0	0	0	INIT[16]	INIT[16]
0	1	0	0	0	1	INIT[17]	INIT[17]
0	1	0	0	1	0	INIT[18]	INIT[18]
0	1	0	0	1	1	INIT[19]	INIT[19]
0	1	0	1	0	0	INIT[20]	INIT[20]
0	1	0	1	0	1	INIT[21]	INIT[21]
0	1	0	1	1	0	INIT[22]	INIT[22]
0	1	0	1	1	1	INIT[23]	INIT[23]
0	1	1	0	0	0	INIT[24]	INIT[24]
0	1	1	0	0	1	INIT[25]	INIT[25]
0	1	1	0	1	0	INIT[26]	INIT[26]
0	1	1	0	1	1	INIT[27]	INIT[27]
0	1	1	1	0	0	INIT[28]	INIT[28]
0	1	1	1	0	1	INIT[29]	INIT[29]
0	1	1	1	1	0	INIT[30]	INIT[30]
0	1	1	1	1	1	INIT[31]	INIT[31]
1	0	0	0	0	0	INIT[0]	INIT[32]
1	0	0	0	0	1	INIT[1]	INIT[33]
1	0	0	0	1	0	INIT[2]	INIT[34]
1	0	0	0	1	1	INIT[3]	INIT[35]
1	0	0	1	0	0	INIT[4]	INIT[36]
1	0	0	1	0	1	INIT[5]	INIT[37]
1	0	0	1	1	0	INIT[6]	INIT[38]
1	0	0	1	1	1	INIT[7]	INIT[39]
1	0	1	0	0	0	INIT[8]	INIT[40]
1	0	1	0	0	1	INIT[9]	INIT[41]
1	0	1	0	1	0	INIT[10]	INIT[42]
1	0	1	0	1	1	INIT[11]	INIT[43]
1	0	1	1	0	0	INIT[12]	INIT[44]
1	0	1	1	0	1	INIT[13]	INIT[45]
1	0	1	1	1	0	INIT[14]	INIT[46]

Inputs						Outputs	
1	0	1	1	1	1	INIT[15]	INIT[47]
1	1	0	0	0	0	INIT[16]	INIT[48]
1	1	0	0	0	1	INIT[17]	INIT[49]
1	1	0	0	1	0	INIT[18]	INIT[50]
1	1	0	0	1	1	INIT[19]	INIT[51]
1	1	0	1	0	0	INIT[20]	INIT[52]
1	1	0	1	0	1	INIT[21]	INIT[53]
1	1	0	1	1	0	INIT[22]	INIT[54]
1	1	0	1	1	1	INIT[23]	INIT[55]
1	1	1	0	0	0	INIT[24]	INIT[56]
1	1	1	0	0	1	INIT[25]	INIT[57]
1	1	1	0	1	0	INIT[26]	INIT[58]
1	1	1	0	1	1	INIT[27]	INIT[59]
1	1	1	1	0	0	INIT[28]	INIT[60]
1	1	1	1	0	1	INIT[29]	INIT[61]
1	1	1	1	1	0	INIT[30]	INIT[62]
1	1	1	1	1	1	INIT[31]	INIT[63]

INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute

Port Descriptions

Port	Direction	Width	Function
O6	Output	1	6/5-LUT output
O5	Output	1	5-LUT output
I0, I1, I2, I3, I4, I5	Input	1	LUT inputs

Design Entry Method

This design element can be used in schematics.

Available Attributes

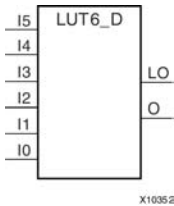
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 64-Bit Value	All zeros	Specifies the LUT5/6 output function.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LUT6_D

Primitive: 6-Input Lookup Table with General and Local Outputs



Introduction

This design element is a six-input, one-output look-up table (LUT) that can either act as an asynchronous 64-bit ROM (with 6-bit addressing) or implement any 6-input logic function. LUTs are the basic logic building blocks and are used to implement most logic functions of the design. A LUT6 is mapped to one of the four look-up tables in the slice. The functionality of the LUT6, LUT6_L and LUT6_D is the same. However, the LUT6_L and LUT6_D allow the additional specification to connect the LUT6 output signal to an internal slice, or CLB connection, using the LO output. The LUT6_L specifies that the only connections from the LUT6 will be within a slice, or CLB, while the LUT6_D allows the specification to connect the output of the LUT to both inter-slice/CLB logic and external logic as well. The LUT6 does not state any specific output connections and should be used in all cases except where internal slice or CLB signal connections must be implicitly specified.

An INIT attribute consisting of a 64-bit Hexadecimal value must be specified to indicate the LUTs logical function. The INIT value is calculated by assigning a 1 to corresponding INIT bit value when the associated inputs are applied. For instance, a Verilog INIT value of 64'h8000000000000000 (X"8000000000000000" for VHDL) makes the output zero unless all of the inputs are one (a 6-input AND gate). A Verilog INIT value of 64'hffffffffffff (X"FFFFFFFFFFFFFF" for VHDL) makes the output one unless all zeros are on the inputs (a 6-input OR gate).

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and more is self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs						Outputs	
I5	I4	I3	I2	I1	I0	O	LO
0	0	0	0	0	0	INIT[0]	INIT[0]
0	0	0	0	0	1	INIT[1]	INIT[1]
0	0	0	0	1	0	INIT[2]	INIT[2]
0	0	0	0	1	1	INIT[3]	INIT[3]
0	0	0	1	0	0	INIT[4]	INIT[4]
0	0	0	1	0	1	INIT[5]	INIT[5]
0	0	0	1	1	0	INIT[6]	INIT[6]
0	0	0	1	1	1	INIT[7]	INIT[7]

Inputs						Outputs	
I5	I4	I3	I2	I1	I0	O	LO
0	0	1	0	0	0	INIT[8]	INIT[8]
0	0	1	0	0	1	INIT[9]	INIT[9]
0	0	1	0	1	0	INIT[10]	INIT[10]
0	0	1	0	1	1	INIT[11]	INIT[11]
0	0	1	1	0	0	INIT[12]	INIT[12]
0	0	1	1	0	1	INIT[13]	INIT[13]
0	0	1	1	1	0	INIT[14]	INIT[14]
0	0	1	1	1	1	INIT[15]	INIT[15]
0	1	0	0	0	0	INIT[16]	INIT[16]
0	1	0	0	0	1	INIT[17]	INIT[17]
0	1	0	0	1	0	INIT[18]	INIT[18]
0	1	0	0	1	1	INIT[19]	INIT[19]
0	1	0	1	0	0	INIT[20]	INIT[20]
0	1	0	1	0	1	INIT[21]	INIT[21]
0	1	0	1	1	0	INIT[22]	INIT[22]
0	1	0	1	1	1	INIT[23]	INIT[23]
0	1	1	0	0	0	INIT[24]	INIT[24]
0	1	1	0	0	1	INIT[25]	INIT[25]
0	1	1	0	1	0	INIT[26]	INIT[26]
0	1	1	0	1	1	INIT[27]	INIT[27]
0	1	1	1	0	0	INIT[28]	INIT[28]
0	1	1	1	0	1	INIT[29]	INIT[29]
0	1	1	1	1	0	INIT[30]	INIT[30]
0	1	1	1	1	1	INIT[31]	INIT[31]
1	0	0	0	0	0	INIT[32]	INIT[32]
1	0	0	0	0	1	INIT[33]	INIT[33]
1	0	0	0	1	0	INIT[34]	INIT[34]
1	0	0	0	1	1	INIT[35]	INIT[35]
1	0	0	1	0	0	INIT[36]	INIT[36]
1	0	0	1	0	1	INIT[37]	INIT[37]
1	0	0	1	1	0	INIT[38]	INIT[38]
1	0	0	1	1	1	INIT[39]	INIT[39]
1	0	1	0	0	0	INIT[40]	INIT[40]
1	0	1	0	0	1	INIT[41]	INIT[41]
1	0	1	0	1	0	INIT[42]	INIT[42]
1	0	1	0	1	1	INIT[43]	INIT[43]
1	0	1	1	0	0	INIT[44]	INIT[44]
1	0	1	1	0	1	INIT[45]	INIT[45]

Inputs						Outputs	
I5	I4	I3	I2	I1	I0	O	LO
1	0	1	1	1	0	INIT[46]	INIT[46]
1	0	1	1	1	1	INIT[47]	INIT[47]
1	1	0	0	0	0	INIT[48]	INIT[48]
1	1	0	0	0	1	INIT[49]	INIT[49]
1	1	0	0	1	0	INIT[50]	INIT[50]
1	1	0	0	1	1	INIT[51]	INIT[51]
1	1	0	1	0	0	INIT[52]	INIT[52]
1	1	0	1	0	1	INIT[53]	INIT[53]
1	1	0	1	1	0	INIT[54]	INIT[54]
1	1	0	1	1	1	INIT[55]	INIT[55]
1	1	1	0	0	0	INIT[56]	INIT[56]
1	1	1	0	0	1	INIT[57]	INIT[57]
1	1	1	0	1	0	INIT[58]	INIT[58]
1	1	1	0	1	1	INIT[59]	INIT[59]
1	1	1	1	0	0	INIT[60]	INIT[60]
1	1	1	1	0	1	INIT[61]	INIT[61]
1	1	1	1	1	0	INIT[62]	INIT[62]
1	1	1	1	1	1	INIT[63]	INIT[63]

INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute

Port Description

Name	Direction	Width	Function
O6	Output	1	6/5-LUT output
O5	Output	1	5-LUT output
I0, I1, I2, I3, I4, I5	Input	1	LUT inputs

Design Entry Method

This design element can be used in schematics.

Available Attributes

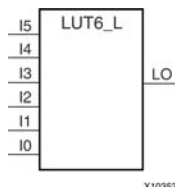
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 64-Bit Value	All zeros	Specifies the logic value for the look-up tables.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

LUT6_L

Primitive: 6-Input Lookup Table with Local Output



Introduction

This design element is a 6-input, 1-output look-up table (LUT) that can either act as an asynchronous 64-bit ROM (with 6-bit addressing) or implement any 6-input logic function. LUTs are the basic logic building blocks and are used to implement most logic functions of the design. A LUT6 is mapped to one of the four look-up tables in the slice. The functionality of the LUT6, LUT6_L and LUT6_D is the same. However, the LUT6_L and LUT6_D allow the additional specification to connect the LUT6 output signal to an internal slice, or CLB connection, using the LO output. The LUT6_L specifies that the only connections from the LUT6 are within a slice, or CLB, while the LUT6_D allows the specification to connect the output of the LUT to both inter-slice/CLB logic and external logic as well. The LUT6 does not state any specific output connections and should be used in all cases except where internal slice or CLB signal connections must be implicitly specified.

An INIT attribute consisting of a 64-bit hexadecimal value must be specified to indicate the LUT's logical function. The INIT value is calculated by assigning a 1 to the corresponding INIT bit value when the associated inputs are applied. For instance, a Verilog INIT value of 64'h8000000000000000 (X"8000000000000000" for VHDL) will make the output zero unless all of the inputs are one (a 6-input AND gate). A Verilog INIT value of 64'hfffffffffffffe (X"FFFFFFFFFFFFFFFE" for VHDL) will make the output one unless all zeros are on the inputs (a 6-input OR gate).

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary truth table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs						Outputs
I5	I4	I3	I2	I1	I0	LO
0	0	0	0	0	0	INIT[0]
0	0	0	0	0	1	INIT[1]
0	0	0	0	1	0	INIT[2]
0	0	0	0	1	1	INIT[3]
0	0	0	1	0	0	INIT[4]
0	0	0	1	0	1	INIT[5]
0	0	0	1	1	0	INIT[6]

Inputs						Outputs
I5	I4	I3	I2	I1	I0	LO
0	0	0	1	1	1	INIT[7]
0	0	1	0	0	0	INIT[8]
0	0	1	0	0	1	INIT[9]
0	0	1	0	1	0	INIT[10]
0	0	1	0	1	1	INIT[11]
0	0	1	1	0	0	INIT[12]
0	0	1	1	0	1	INIT[13]
0	0	1	1	1	0	INIT[14]
0	0	1	1	1	1	INIT[15]
0	1	0	0	0	0	INIT[16]
0	1	0	0	0	1	INIT[17]
0	1	0	0	1	0	INIT[18]
0	1	0	0	1	1	INIT[19]
0	1	0	1	0	0	INIT[20]
0	1	0	1	0	1	INIT[21]
0	1	0	1	1	0	INIT[22]
0	1	0	1	1	1	INIT[23]
0	1	1	0	0	0	INIT[24]
0	1	1	0	0	1	INIT[25]
0	1	1	0	1	0	INIT[26]
0	1	1	0	1	1	INIT[27]
0	1	1	1	0	0	INIT[28]
0	1	1	1	0	1	INIT[29]
0	1	1	1	1	0	INIT[30]
0	1	1	1	1	1	INIT[31]
1	0	0	0	0	0	INIT[32]
1	0	0	0	0	1	INIT[33]
1	0	0	0	1	0	INIT[34]
1	0	0	0	1	1	INIT[35]
1	0	0	1	0	0	INIT[36]
1	0	0	1	0	1	INIT[37]
1	0	0	1	1	0	INIT[38]
1	0	0	1	1	1	INIT[39]
1	0	1	0	0	0	INIT[40]
1	0	1	0	0	1	INIT[41]
1	0	1	0	1	0	INIT[42]
1	0	1	0	1	1	INIT[43]
1	0	1	1	0	0	INIT[44]

Inputs						Outputs
I5	I4	I3	I2	I1	I0	LO
1	0	1	1	0	1	INIT[45]
1	0	1	1	1	0	INIT[46]
1	0	1	1	1	1	INIT[47]
1	1	0	0	0	0	INIT[48]
1	1	0	0	0	1	INIT[49]
1	1	0	0	1	0	INIT[50]
1	1	0	0	1	1	INIT[51]
1	1	0	1	0	0	INIT[52]
1	1	0	1	0	1	INIT[53]
1	1	0	1	1	0	INIT[54]
1	1	0	1	1	1	INIT[55]
1	1	1	0	0	0	INIT[56]
1	1	1	0	0	1	INIT[57]
1	1	1	0	1	0	INIT[58]
1	1	1	0	1	1	INIT[59]
1	1	1	1	0	0	INIT[60]
1	1	1	1	0	1	INIT[61]
1	1	1	1	1	0	INIT[62]
1	1	1	1	1	1	INIT[63]

INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute

Port Description

Name	Direction	Width	Function
LO	Output	1	6/5-LUT output or internal CLB connection
I0, I1, I2, I3, I4, I5	Input	1	LUT inputs

Design Entry Method

This design element can be used in schematics.

Available Attributes

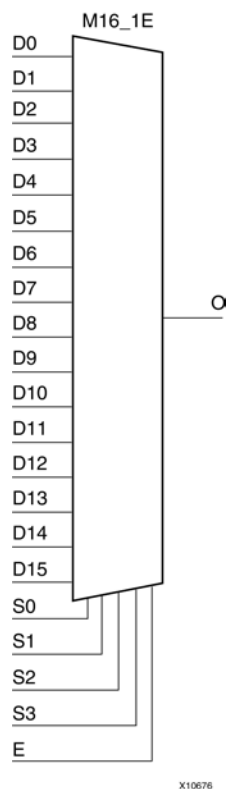
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 64-Bit Value	All zeros	Specifies the logic value for the look-up tables.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

M16_1E

Macro: 16-to-1 Multiplexer with Enable



Introduction

This design element is a 16-to-1 multiplexer with enable. When the enable input (E) is High, the M16_1E multiplexer chooses one data bit from 16 sources (D15 : D0) under the control of the select inputs (S3 : S0). The output (O) reflects the state of the selected input as shown in the logic table. When (E) is Low, the output is Low.

Logic Table

Inputs						Outputs
E	S3	S2	S1	S0	D15-D0	O
0	X	X	X	X	X	0
1	0	0	0	0	D0	D0
1	0	0	0	1	D1	D1
1	0	0	1	0	D2	D2
1	0	0	1	1	D3	D3
.
.
.
1	1	1	0	0	D12	D12
1	1	1	0	1	D13	D13
1	1	1	1	0	D14	D14
1	1	1	1	1	D15	D15

Design Entry Method

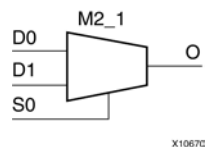
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

M2_1

Macro: 2-to-1 Multiplexer



Introduction

This design element chooses one data bit from two sources (D1 or D0) under the control of the select input (S0). The output (O) reflects the state of the selected data input. When Low, S0 selects D0 and when High, S0 selects D1.

Logic Table

Inputs			Outputs
S0	D1	D0	O
1	D1	X	D1
0	X	D0	D0

Design Entry Method

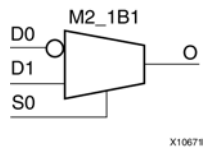
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

M2_1B1

Macro: 2-to-1 Multiplexer with D0 Inverted



Introduction

This design element chooses one data bit from two sources (D1 or D0) under the control of select input (S0). When S0 is Low, the output (O) reflects the inverted value of (D0). When S0 is High, (O) reflects the state of D1.

Logic Table

Inputs			Outputs
S0	D1	D0	O
1	1	X	1
1	0	X	0
0	X	1	0
0	X	0	1

Design Entry Method

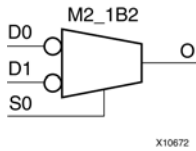
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

M2_1B2

Macro: 2-to-1 Multiplexer with D0 and D1 Inverted



Introduction

This design element chooses one data bit from two sources (D1 or D0) under the control of select input (S0). When S0 is Low, the output (O) reflects the inverted value of D0. When S0 is High, O reflects the inverted value of D1.

Logic Table

Inputs			Outputs
S0	D1	D0	O
1	1	X	0
1	0	X	1
0	X	1	0
0	X	0	1

Design Entry Method

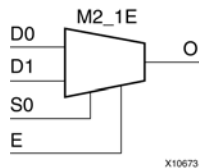
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

M2_1E

Macro: 2-to-1 Multiplexer with Enable



Introduction

This design element is a 2-to-1 multiplexer with enable. When the enable input (E) is High, the M2_1E chooses one data bit from two sources (D1 or D0) under the control of select input (S0). When Low, S0 selects D0 and when High, S0 selects D1. When (E) is Low, the output is Low.

Logic Table

Inputs				Outputs
E	S0	D1	D0	O
0	X	X	X	0
1	0	X	1	1
1	0	X	0	0
1	1	1	X	1
1	1	0	X	0

Design Entry Method

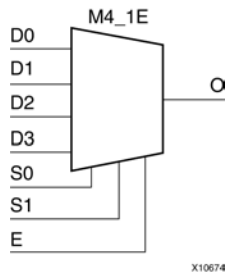
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

M4_1E

Macro: 4-to-1 Multiplexer with Enable



Introduction

This design element is a 4-to-1 multiplexer with enable. When the enable input (E) is High, the M4_1E multiplexer chooses one data bit from four sources (D3, D2, D1, or D0) under the control of the select inputs (S1 : S0). The output (O) reflects the state of the selected input as shown in the logic table. When (E) is Low, the output is Low.

Logic Table

Inputs							Outputs
E	S1	S0	D0	D1	D2	D3	O
0	X	X	X	X	X	X	0
1	0	0	D0	X	X	X	D0
1	0	1	X	D1	X	X	D1
1	1	0	X	X	D2	X	D2
1	1	1	X	X	X	D3	D3

Design Entry Method

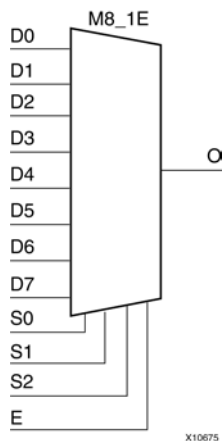
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

M8_1E

Macro: 8-to-1 Multiplexer with Enable



Introduction

This design element is an 8-to-1 multiplexer with enable. When the enable input (E) is High, the M8_1E multiplexer chooses one data bit from eight sources (D7 : D0) under the control of the select inputs (S2 : S0). The output (O) reflects the state of the selected input as shown in the logic table. When (E) is Low, the output is Low.

Logic Table

Inputs					Outputs
E	S2	S1	S0	D7-D0	O
0	X	X	X	X	0
1	0	0	0	D0	D0
1	0	0	1	D1	D1
1	0	1	0	D2	D2
1	0	1	1	D3	D3
1	1	0	0	D4	D4
1	1	0	1	D5	D5
1	1	1	0	D6	D6
1	1	1	1	D7	D7

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

MULT18X18

Primitive: 18 x 18 Signed Multiplier



Introduction

MULT18X18 is a combinational signed 18-bit by 18-bit multiplier. The value represented in the 18-bit input A is multiplied by the value represented in the 18-bit input B. Output P is the 36-bit product of A and B.

Logic Table

Inputs		Output
A	B	P
A	B	A x B
A, B, and P are two's complement.		

Design Entry Method

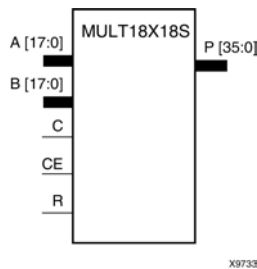
This design element can be used in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

MULT18X18S

Primitive: 18 x 18 Signed Multiplier – Registered Version



Introduction

MULT18X18S is the registered version of the 18 x 18 signed multiplier with output P and inputs A, B, C, CE, and R. The registers are initialized to 0 after the GSR pulse.

The value represented in the 18-bit input A is multiplied by the value represented in the 18-bit input B. Output P is the 36-bit product of A and B.

Logic Table

Inputs					Output
C	CE	Am	Bn	R	P
↑	X	X	X	1	0
↑	1	Am	Bn	0	A x B
X	0	X	X	0	No Change

A, B, and P are two's complement.

Design Entry Method

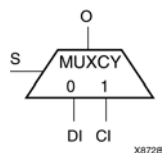
This design element can be used in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

MUXCY

Primitive: 2-to-1 Multiplexer for Carry Logic with General Output



Introduction

The direct input (DI) of a slice is connected to the (DI) input of the MUXCY. The carry in (CI) input of an LC is connected to the CI input of the MUXCY. The select input (S) of the MUXCY is driven by the output of the look-up table (LUT) and configured as a MUX function. The carry out (O) of the MUXCY reflects the state of the selected input and implements the carry out function of each LC. When Low, S selects DI; when High, S selects CI.

The variants “MUXCY_D” and “MUXCY_L” provide additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

Logic Table

Inputs			Outputs
S	DI	CI	O
0	1	X	1
0	0	X	0
1	X	1	1
1	X	0	0

Design Entry Method

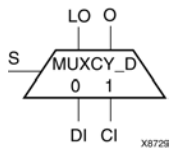
This design element can be used in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

MUXCY_D

Primitive: 2-to-1 Multiplexer for Carry Logic with Dual Output



Introduction

This design element implements a 1-bit, high-speed carry propagate function. One such function can be implemented per logic cell (LC), for a total of 4-bits per configurable logic block (CLB). The direct input (DI) of an LC is connected to the DI input of the MUXCY_D. The carry in (CI) input of an LC is connected to the CI input of the MUXCY_D. The select input (S) of the MUX is driven by the output of the look-up table (LUT) and configured as an XOR function. The carry out (O and LO) of the MUXCY_D reflects the state of the selected input and implements the carry out function of each LC. When Low, S selects DI; when High, S selects CI.

Outputs O and LO are functionally identical. The O output is a general interconnect. See also “MUXCY” and “MUXCY_L”.

Logic Table

Inputs			Outputs	
S	DI	CI	O	LO
0	1	X	1	1
0	0	X	0	0
1	X	1	1	1
1	X	0	0	0

Design Entry Method

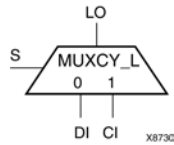
This design element can be used in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

MUXCY_L

Primitive: 2-to-1 Multiplexer for Carry Logic with Local Output



Introduction

This design element implements a 1-bit high-speed carry propagate function. One such function is implemented per logic cell (LC), for a total of 4-bits per configurable logic block (CLB). The direct input (DI) of an LC is connected to the DI input of the MUXCY_L. The carry in (CI) input of an LC is connected to the CI input of the MUXCY_L. The select input (S) of the MUXCY_L is driven by the output of the look-up table (LUT) and configured as an XOR function. The carry out (LO) of the MUXCY_L reflects the state of the selected input and implements the carry out function of each (LC). When Low, (S) selects DI; when High, (S) selects (CI).

See also “MUXCY” and “MUXCY_D.”

Logic Table

Inputs			Outputs
S	DI	CI	LO
0	1	X	1
0	0	X	0
1	X	1	1
1	X	0	0

Design Entry Method

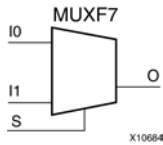
This design element can be used in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

MUXF7

Primitive: 2-to-1 Look-Up Table Multiplexer with General Output



Introduction

This design element provides a multiplexer function for use in creating a function-of-7 look-up table or an 8-to-1 multiplexer in combination with the associated look-up tables. Local outputs (LO) of MUXF6 are connected to the I0 and I1 inputs of the MUXF7. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

The variants, “MUXF7_D” and “MUXF7_L”, provide additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

Logic Table

Inputs			Outputs
S	I0	I1	O
0	I0	X	I0
1	X	I1	I1
X	0	0	0
X	1	1	1

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Output of MUX to general routing
I0	Input	1	Input (tie to MUXF6 LO out)
I1	Input	1	Input (tie to MUXF6 LO out)
S	Input	1	Input select to MUX

Design Entry Method

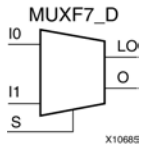
This design element can be used in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

MUXF7_D

Primitive: 2-to-1 Look-Up Table Multiplexer with Dual Output



Introduction

This design element provides a multiplexer function for use in creating a function-of-7 look-up table or a 16-to-1 multiplexer in combination with the associated look-up tables. Local outputs (LO) of MUXF6 are connected to the I0 and I1 inputs of the MUXF7. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

Outputs O and LO are functionally identical. The O output is a general interconnect. The LO output connects to other inputs in the same CLB slice.

Logic Table

Inputs			Outputs	
S	I0	I1	O	LO
0	I0	X	I0	I0
1	X	I1	I1	I1
X	0	0	0	0
X	1	1	1	1

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Output of MUX to general routing
LO	Output	1	Output of MUX to local routing
I0	Input	1	Input (tie to MUXF6 LO out)
I1	Input	1	Input (tie to MUXF6 LO out)
S	Input	1	Input select to MUX

Design Entry Method

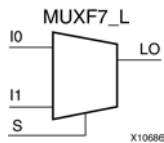
This design element can be used in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

MUXF7_L

Primitive: 2-to-1 look-up table Multiplexer with Local Output



Introduction

This design element provides a multiplexer function for use in creating a function-of-7 look-up table or a 16-to-1 multiplexer in combination with the associated look-up tables. Local outputs (LO) of MUXF6 are connected to the I0 and I1 inputs of the MUXF7. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

The LO output connects to other inputs in the same CLB slice.

Logic Table

Inputs			Output
S	I0	I1	LO
0	I0	X	I0
1	X	I1	I1
X	0	0	0
X	1	1	1

Port Descriptions

Port	Direction	Width	Function
LO	Output	1	Output of MUX to local routing
I0	Input	1	Input
I1	Input	1	Input
S	Input	1	Input select to MUX

Design Entry Method

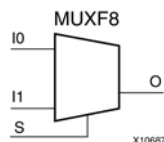
This design element can be used in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

MUXF8

Primitive: 2-to-1 Look-Up Table Multiplexer with General Output



Introduction

This design element provides a multiplexer function in eight slices for creating a function-of-8 look-up table or a 16-to-1 multiplexer in combination with the associated look-up tables, MUXF5s, MUXF6s, and MUXF7s. Local outputs (LO) of MUXF7 are connected to the I0 and I1 inputs of the MUXF8. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

Logic Table

Inputs			Outputs
S	I0	I1	O
0	I0	X	I0
1	X	I1	I1
X	0	0	0
X	1	1	1

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Output of MUX to general routing
I0	Input	1	Input (tie to MUXF7 LO out)
I1	Input	1	Input (tie to MUXF7 LO out)
S	Input	1	Input select to MUX

Design Entry Method

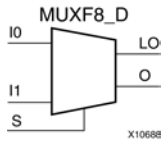
This design element can be used in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

MUXF8_D

Primitive: 2-to-1 Look-Up Table Multiplexer with Dual Output



Introduction

This design element provides a multiplexer function in eight slices for creating a function-of-8 look-up table or a 32-to-1 multiplexer in combination with the associated four look-up tables and two MUXF8s. Local outputs (LO) of MUXF7 are connected to the I0 and I1 inputs of the MUXF8. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

Outputs O and LO are functionally identical. The O output is a general interconnect. The LO output connects to other inputs in the same CLB slice.

Logic Table

Inputs			Outputs	
S	I0	I1	O	LO
0	I0	X	I0	I0
1	X	I1	I1	I1
X	0	0	0	0
X	1	1	1	1

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Output of MUX to general routing
LO	Output	1	Output of MUX to local routing
I0	Input	1	Input (tie to MUXF7 LO out)
I1	Input	1	Input (tie to MUXF7 LO out)
S	Input	1	Input select to MUX

Design Entry Method

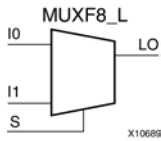
This design element can be used in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

MUXF8_L

Primitive: 2-to-1 Look-Up Table Multiplexer with Local Output



Introduction

This design element provides a multiplexer function in eight slices for creating a function-of-8 look-up table or a 32-to-1 multiplexer in combination with the associated four look-up tables and two MUXF8s. Local outputs (LO) of MUXF7 are connected to the I0 and I1 inputs of the MUXF8. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

The LO output connects to other inputs in the same CLB slice.

Logic Table

Inputs			Output
S	I0	I1	LO
0	I0	X	I0
1	X	I1	I1
X	0	0	0
X	1	1	1

Port Descriptions

Port	Direction	Width	Function
LO	Output	1	Output of MUX to local routing
I0	Input	1	Input (tie to MUXF7 LO out)
I1	Input	1	Input (tie to MUXF7 LO out)
S	Input	1	Input select to MUX

Design Entry Method

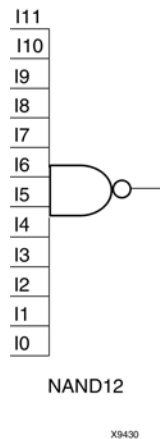
This design element can be used in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NAND12

Macro: 12- Input NAND Gate with Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

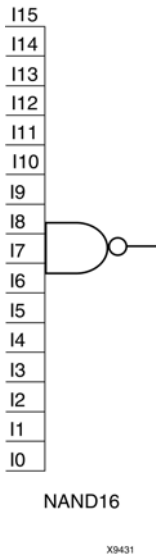
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NAND16

Macro: 16- Input NAND Gate with Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

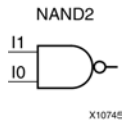
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NAND2

Primitive: 2-Input NAND Gate with Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NAND2B1

Primitive: 2-Input NAND Gate with 1 Inverted and 1 Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

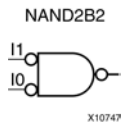
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NAND2B2

Primitive: 2-Input NAND Gate with Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

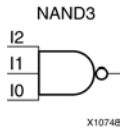
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NAND3

Primitive: 3-Input NAND Gate with Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

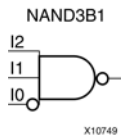
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NAND3B1

Primitive: 3-Input NAND Gate with 1 Inverted and 2 Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

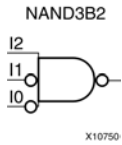
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NAND3B2

Primitive: 3-Input NAND Gate with 2 Inverted and 1 Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

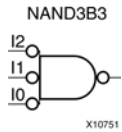
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NAND3B3

Primitive: 3-Input NAND Gate with Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

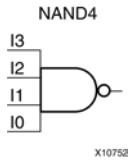
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NAND4

Primitive: 4-Input NAND Gate with Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

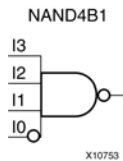
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NAND4B1

Primitive: 4-Input NAND Gate with 1 Inverted and 3 Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

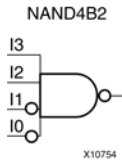
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NAND4B2

Primitive: 4-Input NAND Gate with 2 Inverted and 2 Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

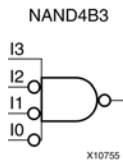
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NAND4B3

Primitive: 4-Input NAND Gate with 3 Inverted and 1 Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

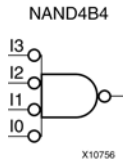
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NAND4B4

Primitive: 4-Input NAND Gate with Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

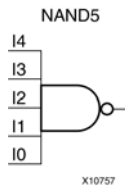
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NAND5

Primitive: 5-Input NAND Gate with Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

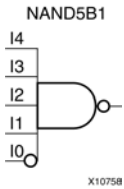
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NAND5B1

Primitive: 5-Input NAND Gate with 1 Inverted and 4 Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

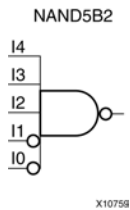
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NAND5B2

Primitive: 5-Input NAND Gate with 2 Inverted and 3 Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

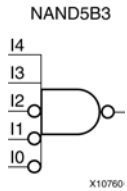
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NAND5B3

Primitive: 5-Input NAND Gate with 3 Inverted and 2 Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

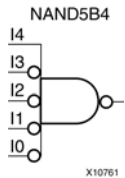
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NAND5B4

Primitive: 5-Input NAND Gate with 4 Inverted and 1 Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

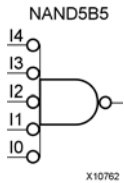
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NAND5B5

Primitive: 5-Input NAND Gate with Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

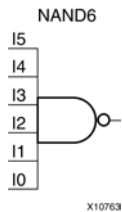
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NAND6

Macro: 6-Input NAND Gate with Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

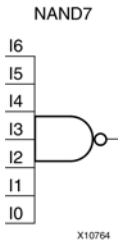
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NAND7

Macro: 7-Input NAND Gate with Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

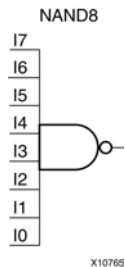
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NAND8

Macro: 8-Input NAND Gate with Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

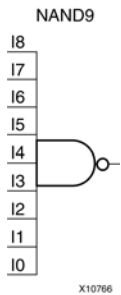
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NAND9

Macro: 9-Input NAND Gate with Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

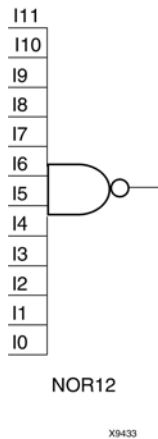
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NOR12

Macro: 12-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

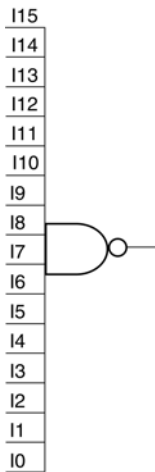
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NOR16

Macro: 16-Input NOR Gate with Non-Inverted Inputs



NOR16

X9434

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

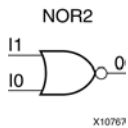
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NOR2

Primitive: 2-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

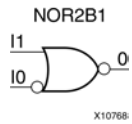
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NOR2B1

Primitive: 2-Input NOR Gate with 1 Inverted and 1 Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

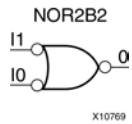
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NOR2B2

Primitive: 2-Input NOR Gate with Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

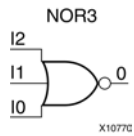
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NOR3

Primitive: 3-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

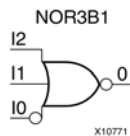
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NOR3B1

Primitive: 3-Input NOR Gate with 1 Inverted and 2 Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

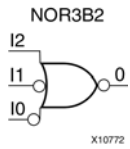
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NOR3B2

Primitive: 3-Input NOR Gate with 2 Inverted and 1 Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

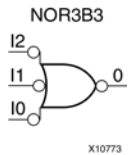
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NOR3B3

Primitive: 3-Input NOR Gate with Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

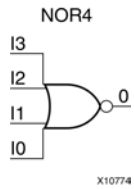
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NOR4

Primitive: 4-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

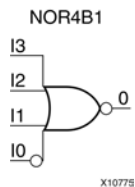
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NOR4B1

Primitive: 4-Input NOR Gate with 1 Inverted and 3 Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

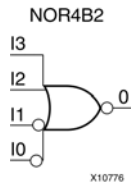
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NOR4B2

Primitive: 4-Input NOR Gate with 2 Inverted and 2 Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

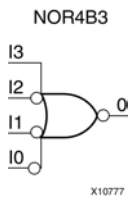
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NOR4B3

Primitive: 4-Input NOR Gate with 3 Inverted and 1 Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

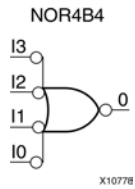
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NOR4B4

Primitive: 4-Input NOR Gate with Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

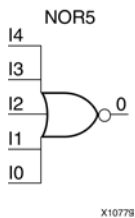
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NOR5

Primitive: 5-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

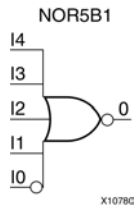
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NOR5B1

Primitive: 5-Input NOR Gate with 1 Inverted and 4 Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

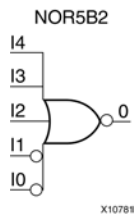
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NOR5B2

Primitive: 5-Input NOR Gate with 2 Inverted and 3 Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

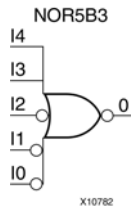
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NOR5B3

Primitive: 5-Input NOR Gate with 3 Inverted and 2 Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

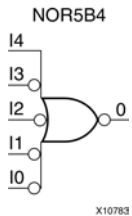
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NOR5B4

Primitive: 5-Input NOR Gate with 4 Inverted and 1 Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

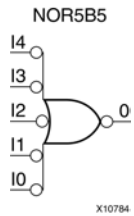
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NOR5B5

Primitive: 5-Input NOR Gate with Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

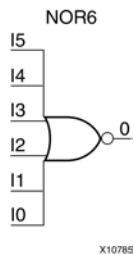
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NOR6

Macro: 6-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

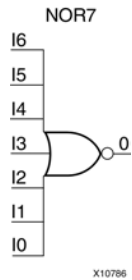
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NOR7

Macro: 7-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

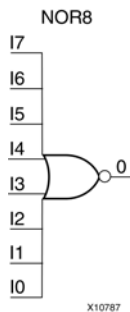
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NOR8

Macro: 8-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

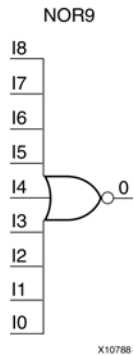
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

NOR9

Macro: 9-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

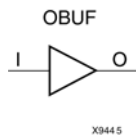
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OBUF

Primitive: Output Buffer



Introduction

This design element is a simple output buffer used to drive output signals to the FPGA device pins that do not need to be 3-stated (constantly driven). Either an OBUF, OBUFT, OBUFDS, or OBUFTDS must be connected to every output port in the design.

This element isolates the internal circuit and provides drive current for signals leaving a chip. It exists in input/output blocks (IOB). Its output (O) is connected to an OPAD or an IOPAD. The interface standard used by this element is LVTTTL. Also, this element has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Output of OBUF to be connected directly to top-level output port.
I	Input	1	Input of OBUF. Connect to the logic driving the output port.

Design Entry Method

This design element can be used in schematics.

Available Attributes

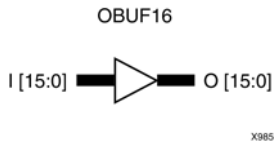
Attribute	Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Specifies the output current drive strength of the I/O. It is suggested that you set this to the lowest setting tolerable for the design drive and timing requirements.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. Consult the product Data Sheet for recommendations of the best setting for this attribute.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OBUF16

Macro: 16-Bit Output Buffer



Introduction

This design element is a multiple output buffer.

This element isolates the internal circuit and provides drive current for signals leaving a chip. It exists in input/output blocks (IOB). Its output (O) is connected to an OPAD or an IOPAD. The interface standard used by this element is LVTTTL. Also, this element has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

Design Entry Method

This design element can be used in schematics.

Available Attributes

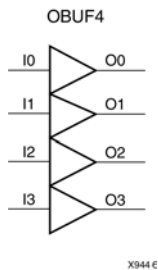
Attribute	Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Specifies the output current drive strength of the I/O. It is suggested that you set this to the lowest setting tolerable for the design drive and timing requirements.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. Consult the product Data Sheet for recommendations of the best setting for this attribute.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OBUF4

Macro: 4-Bit Output Buffer



Introduction

This design element is a multiple output buffer.

This element isolates the internal circuit and provides drive current for signals leaving a chip. It exists in input/output blocks (IOB). Its output (O) is connected to an OPAD or an IOPAD. The interface standard used by this element is LVTTTL. Also, this element has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

Design Entry Method

This design element can be used in schematics.

Available Attributes

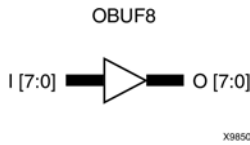
Attribute	Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Specifies the output current drive strength of the I/O. It is suggested that you set this to the lowest setting tolerable for the design drive and timing requirements.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. Consult the product Data Sheet for recommendations of the best setting for this attribute.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OBUF8

Macro: 8-Bit Output Buffer



Introduction

This design element is a multiple output buffer.

This element isolates the internal circuit and provides drive current for signals leaving a chip. It exists in input/output blocks (IOB). Its output (O) is connected to an OPAD or an IOPAD. The interface standard used by this element is LVTTTL. Also, this element has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

Design Entry Method

This design element can be used in schematics.

Available Attributes

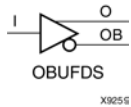
Attribute	Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Specifies the output current drive strength of the I/O. It is suggested that you set this to the lowest setting tolerable for the design drive and timing requirements.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. Consult the product Data Sheet for recommendations of the best setting for this attribute.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OBUFDS

Primitive: Differential Signaling Output Buffer



Introduction

This design element is a single output buffer that supports low-voltage, differential signaling (1.8 v CMOS). OBUFDS isolates the internal circuit and provides drive current for signals leaving the chip. Its output is represented as two distinct ports (O and OB), one deemed the "master" and the other the "slave." The master and the slave are opposite phases of the same logical signal (for example, MYNET and MYNETB).

Logic Table

Inputs	Outputs	
I	O	OB
0	0	1
1	1	0

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Diff_p output (connect directly to top level port)
OB	Output	1	Diff_n output (connect directly to top level port)
I	Input	1	Buffer input

Design Entry Method

This design element can be used in schematics.

Available Attributes

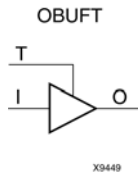
Attribute	Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OBUFT

Primitive: 3-State Output Buffer with Active Low Output Enable



Introduction

This design element is a single, 3-state output buffer with input I, output O, and active-Low output enables (T). This element uses the LVTTL standard and has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

When T is Low, data on the inputs of the buffers is transferred to the corresponding outputs. When T is High, the output is high impedance (off or Z state). OBUFTs are generally used when a single-ended output is needed with a 3-state capability, such as the case when building bidirectional I/O.

Logic Table

Inputs		Outputs
T	I	O
1	X	Z
0	I	F

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Buffer output (connect directly to top-level port)
I	Input	1	Buffer input
T	Input	1	3-state enable input

Design Entry Method

This design element can be used in schematics.

Available Attributes

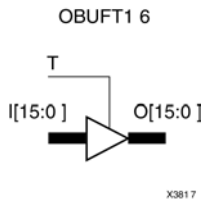
Attribute	Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Specifies the output current drive strength of the I/O. It is suggested that you set this to the lowest setting tolerable for the design drive and timing requirements.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. See the Data Sheet for recommendations of the best setting for this attribute.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OBUFT16

Macro: 16-Bit 3-State Output Buffer with Active Low Output Enable



Introduction

This design element is a multiple, 3-state output buffer with input I, output O, and active-Low output enables (T). This element uses the LVTTTL standard and has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

When T is Low, data on the inputs of the buffers is transferred to the corresponding outputs. When T is High, the output is high impedance (off or Z state). OBUFTs are generally used when a single-ended output is needed with a 3-state capability, such as the case when building bidirectional I/O.

Logic Table

Inputs		Outputs
T	I	O
1	X	Z
0	I	F

Design Entry Method

This design element is only for use in schematics.

Available Attributes

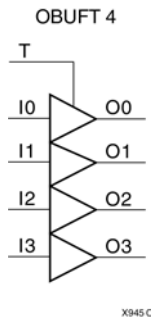
Attribute	Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Specifies the output current drive strength of the I/O. It is suggested that you set this to the lowest setting tolerable for the design drive and timing requirements.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. See the Data Sheet for recommendations of the best setting for this attribute.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OBUFT4

Macro: 4-Bit 3-State Output Buffers with Active-Low Output Enable



Introduction

This design element is a multiple, 3-state output buffer with input I, output O, and active-Low output enables (T). This element uses the LVTTTL standard and has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

When T is Low, data on the inputs of the buffers is transferred to the corresponding outputs. When T is High, the output is high impedance (off or Z state). OBUFTs are generally used when a single-ended output is needed with a 3-state capability, such as the case when building bidirectional I/O.

Logic Table

Inputs		Outputs
T	I	O
1	X	Z
0	I	F

Design Entry Method

This design element is only for use in schematics.

Available Attributes

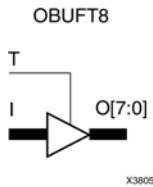
Attribute	Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Specifies the output current drive strength of the I/O. It is suggested that you set this to the lowest setting tolerable for the design drive and timing requirements.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. See the Data Sheet for recommendations of the best setting for this attribute.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OBUFT8

Macro: 8-Bit 3-State Output Buffers with Active-Low Output Enable



Introduction

This design element is a multiple, 3-state output buffer with input I, output O, and active-Low output enables (T). This element uses the LVTTTL standard and has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

When T is Low, data on the inputs of the buffers is transferred to the corresponding outputs. When T is High, the output is high impedance (off or Z state). OBUFTs are generally used when a single-ended output is needed with a 3-state capability, such as the case when building bidirectional I/O.

Logic Table

Inputs		Outputs
T	I	O
1	X	Z
0	I	F

Design Entry Method

This design element is only for use in schematics.

Available Attributes

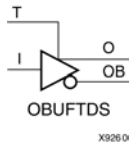
Attribute	Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Specifies the output current drive strength of the I/O. It is suggested that you set this to the lowest setting tolerable for the design drive and timing requirements.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. See the Data Sheet for recommendations of the best setting for this attribute.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OBUFTDS

Primitive: 3-State Output Buffer with Differential Signaling, Active-Low Output Enable



Introduction

This design element is an output buffer that supports low-voltage, differential signaling. For the OBUFTDS, a design level interface signal is represented as two distinct ports (O and OB), one deemed the "master" and the other the "slave." The master and the slave are opposite phases of the same logical signal (for example, MYNET_P and MYNET_N).

Logic Table

Inputs		Outputs	
I	T	O	OB
X	1	Z	Z
0	0	0	1
1	0	1	0

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Diff_p output (connect directly to top level port)
OB	Output	1	Diff_n output (connect directly to top level port)
I	Input	1	Buffer input
T	Input	1	3-state enable input

Design Entry Method

This design element can be used in schematics.

Available Attributes

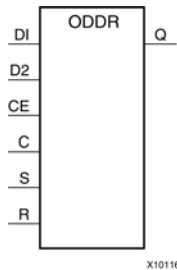
Attribute	Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

ODDR

Primitive: Dedicated Dual Data Rate (DDR) Output Register



Introduction

This design element is a dedicated output register for use in transmitting dual data rate (DDR) signals from FPGA devices. The ODDR primitive's interface with the FPGA fabric are not limited to opposite edges. The ODDR is available with modes that allow data to be presented from the FPGA fabric at the same clock edge. This feature allows designers to avoid additional timing complexities and CLB usage. In addition, the ODDR works in conjunction with SelectIO™ features.

ODDR Modes

This element has two modes of operation. These modes are set by the DDR_CLK_EDGE attribute.

- **OPPOSITE_EDGE mode** - The data transmit interface uses the classic DDR methodology. Given a data and clock at pin D1-2 and C respectively, D1 is sampled at every positive edge of clock C, and D2 is sampled at every negative edge of clock C. Q changes every clock edge.
- **SAME_EDGE mode** - Data is still transmitted at the output of the ODDR by opposite edges of clock C. However, the two inputs to the ODDR are clocked with a positive clock edge of clock signal C and an extra register is clocked with a negative clock edge of clock signal C. Using this feature, DDR data can now be presented into the ODDR at the same clock edge.

Port Descriptions

Port	Type	Width	Function
Q	Output	1	Data Output (DDR) - The ODDR output that connects to the IOB pad.
C	Input	1	Clock Input - The C pin represents the clock input pin.
CE	Input	1	Clock Enable Input - When asserted High, this port enables the clock input on port C.
D1 : D2	Input	1 (each)	Data Input - This pin is where the DDR data is presented into the ODDR module.
R	Input	1	Reset - Depends on how SRTYPE is set.
S	Input	1	Set - Active High asynchronous set pin. This pin can also be Synchronous depending on the SRTYPE attribute.

Design Entry Method

This design element can be used in schematics.

Available Attributes

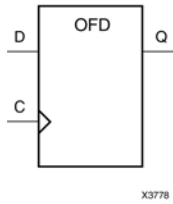
Attribute	Type	Allowed Values	Default	Description
DDR_CLK_EDGE	String	"OPPOSITE_EDGE", "SAME_EDGE"	"OPPOSITE_EDGE"	DDR clock mode recovery mode selection.
INIT	Integer	0, 1	1	Q initialization value.
SRTYPE	String	"SYNC", "ASYNC"	"SYNC"	Set/Reset type selection.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OFD

Macro: Output D Flip-Flop



Introduction

This design element is a single output D flip-flop.

The outputs are connected to OPADs or IOPADs. The data on the (D) inputs is loaded into the flip-flops during the Low-to-High clock (C) transition and appears on the (Q) outputs.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs		Outputs
D	C	Q
D	↑	D

Design Entry Method

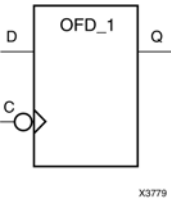
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OFD_1

Macro: Output D Flip-Flop with Inverted Clock



Introduction

The design element is located in an input/output block (IOB). The output (Q) of the D flip-flop is connected to an OPAD or an IOPAD. The data on the (D) input is loaded into the flip-flop during the High-to-Low clock (C) transition and appears on the (Q) output.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs		Outputs
D	C	Q
D	↓	D

Design Entry Method

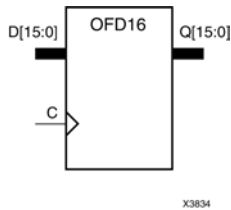
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OFD16

Macro: 16-Bit Output D Flip-Flop



Introduction

This design element is a multiple output D flip-flop.

The outputs are connected to OPADs or IOPADs. The data on the (D) inputs is loaded into the flip-flops during the Low-to-High clock (C) transition and appears on the (Q) outputs.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs		Outputs
D	C	Q
D	↑	D

Design Entry Method

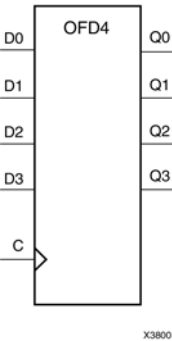
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OFD4

Macro: 4-Bit Output D Flip-Flop



Introduction

This design element is a multiple output D flip-flop.

The outputs are connected to OPADs or IOPADs. The data on the (D) inputs is loaded into the flip-flops during the Low-to-High clock (C) transition and appears on the (Q) outputs.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs		Outputs
D	C	Q
D	↑	D

Design Entry Method

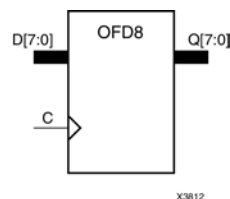
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OFD8

Macro: 8-Bit Output D Flip-Flop



Introduction

This design element is a multiple output D flip-flop.

The outputs are connected to OPADs or IOPADs. The data on the (D) inputs is loaded into the flip-flops during the Low-to-High clock (C) transition and appears on the (Q) outputs.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs		Outputs
D	C	Q
D	↑	D

Design Entry Method

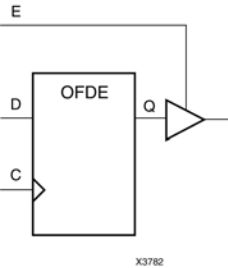
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OFDE

Macro: D Flip-Flop with Active-High Enable Output Buffers



Introduction

This is a single D flip-flop whose output is enabled by a 3-state buffer. The flip-flop data output (Q) is connected to the input of output buffer (OBUFE). The OBUFE output (O) is connected to an OPAD or IOPAD. The data on the data input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition. When the active-High enable input (E) is High, the data on the flip-flop output (Q) appears on the OBUFE (O) output. When (E) is Low, the output is high impedance (Z state or Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs			Output
E	D	C	O
0	X	X	Z
1	Dn	↑	Dn

Design Entry Method

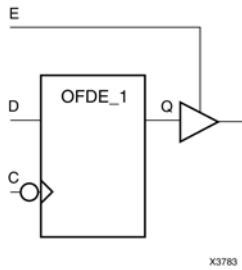
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OFDE_1

Macro: D Flip-Flop with Active-High Enable Output Buffer and Inverted Clock



Introduction

This design element and its output buffer are located in an input/output block (IOB). The data output of the flip-flop (Q) is connected to the input of an output buffer or OBUFE. The output of the OBUFE is connected to an OPAD or an IOPAD. The data on the data input (D) is loaded into the flip-flop on the High-to-Low clock (C) transition. When the active-High enable input (E) is High, the data on the flip-flop output (Q) appears on the (O) output. When (E) is Low, the output is high impedance (Z state or Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs
E	D	C	O
0	X	X	Z
1	D	↓	D

Design Entry Method

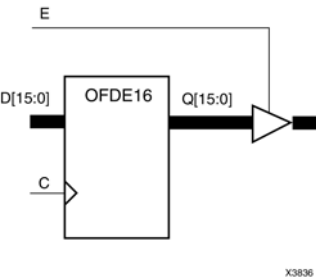
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OFDE16

Macro: 16-Bit D Flip-Flop with Active-High Enable Output Buffers



Introduction

This is a multiple D flip-flop whose outputs are enabled by 3-state buffers. The flip-flop data outputs (Q) are connected to the inputs of output buffers (OBUFE). The OBUFE outputs (O) are connected to OPADs or IOPADs. The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-High enable inputs (E) are High, the data on the flip-flop outputs (Q) appears on the OBUFE outputs (O). When (E) is Low, outputs are high impedance (Z state or Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
E	D	C	O
0	X	X	Z
1	Dn	↑	Dn

Design Entry Method

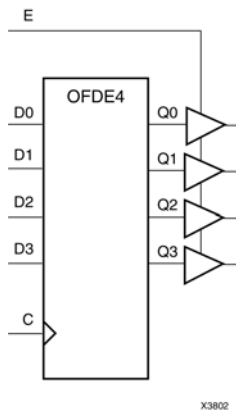
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OFDE4

Macro: 4-Bit D Flip-Flop with Active-High Enable Output Buffers



Introduction

This is a multiple D flip-flop whose outputs are enabled by 3-state buffers. The flip-flop data outputs (Q) are connected to the inputs of output buffers (OBUFE). The OBUFE outputs (O) are connected to OPADs or IOPADs. The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-High enable inputs (E) are High, the data on the flip-flop outputs (Q) appears on the OBUFE outputs (O). When (E) is Low, outputs are high impedance (Z state or Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
E	D	C	O
0	X	X	Z
1	Dn	↑	Dn

Design Entry Method

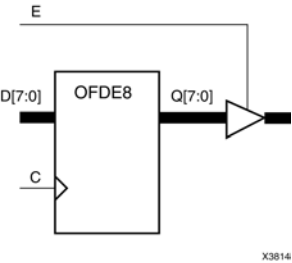
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OFDE8

Macro: 8-Bit D Flip-Flop with Active-High Enable Output Buffers



Introduction

This is a multiple D flip-flop whose outputs are enabled by 3-state buffers. The flip-flop data outputs (Q) are connected to the inputs of output buffers (OBUFE). The OBUFE outputs (O) are connected to OPADs or IOPADs. The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-High enable inputs (E) are High, the data on the flip-flop outputs (Q) appears on the OBUFE outputs (O). When (E) is Low, outputs are high impedance (Z state or Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs			Outputs
E	D	C	O
0	X	X	Z
1	Dn	↑	Dn

Design Entry Method

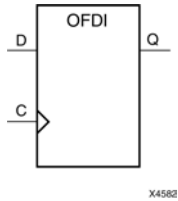
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OFDI

Macro: Output D Flip-Flop (Asynchronous Preset)



Introduction

The design element is contained in an input/output block (IOB). The output (Q) of the (D) flip-flop is connected to an OPAD or an IOPAD. The data on the (D) input is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q).

This flip-flop is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs		Outputs
D	C	Q
D	↑	D

Design Entry Method

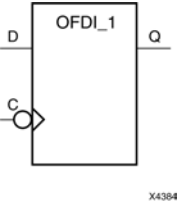
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OFDI_1

Macro: Output D Flip-Flop with Inverted Clock (Asynchronous Preset)



Introduction

This design element exists in an input/output block (IOB). The (D) flip-flop output (Q) is connected to an OPAD or an IOPAD. The data on the (D) input is loaded into the flip-flop during the High-to-Low clock (C) transition and appears on the (Q) output.

This flip-flop is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs		Outputs
D	C	Q
D	↓	D

Design Entry Method

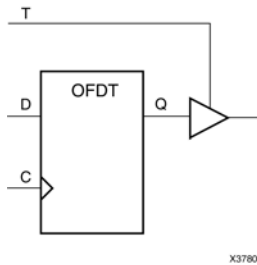
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OFDT

Macro: D Flip-Flop with Active-Low 3-State Output Buffer



Introduction

This design element is a single D flip-flops whose output is enabled by a 3-state buffer.

The data outputs (Q) of the flip-flops are connected to the inputs of output buffers (OBUFT). The outputs of the OBUFTs (O) are connected to OPADs or IOPADs. The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-Low enable inputs (T) are Low, the data on the flip-flop outputs (Q) appears on the (O) outputs. When (T) is High, outputs are high impedance (Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs
T	D	C	O
1	X	X	Z
0	D	↑	D

Design Entry Method

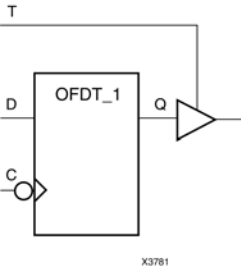
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OFDT_1

Macro: D Flip-Flop with Active-Low 3-State Output Buffer and Inverted Clock



Introduction

The design element and its output buffer are located in an input/output block (IOB). The flip-flop data output (Q) is connected to the input of an output buffer (OBUFT). The OBUFT output is connected to an OPAD or an IOPAD. The data on the data input (D) is loaded into the flip-flop on the High-to-Low clock (C) transition. When the active-Low enable input (T) is Low, the data on the flip-flop output (Q) appears on the (O) output. When (T) is High, the output is high impedance (Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs			Outputs
T	D	C	O
1	X	X	Z
0	D	↓	D

Design Entry Method

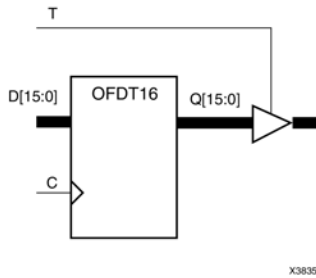
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OFDT16

Macro: 16-Bit D Flip-Flop with Active-Low 3-State Output Buffers



Introduction

This design element is a multiple D flip-flop whose output are enabled by 3-state buffers.

The data outputs (Q) of the flip-flops are connected to the inputs of output buffers (OBUFT). The outputs of the OBUFTs (O) are connected to OPADs or IOPADs. The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-Low enable inputs (T) are Low, the data on the flip-flop outputs (Q) appears on the (O) outputs. When (T) is High, outputs are high impedance (Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs
T	D	C	O
1	X	X	Z
0	D	↑	D

Design Entry Method

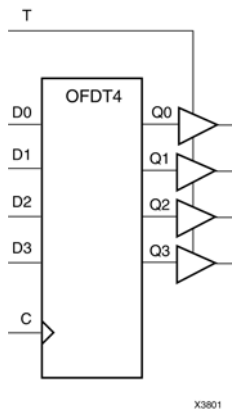
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OFDT4

Macro: 4-Bit D Flip-Flop with Active-Low 3-State Output Buffers



Introduction

This design element is a multiple D flip-flop whose output are enabled by 3-state buffers.

The data outputs (Q) of the flip-flops are connected to the inputs of output buffers (OBUFT). The outputs of the OBUFTs (O) are connected to OPADs or IOPADs. The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-Low enable inputs (T) are Low, the data on the flip-flop outputs (Q) appears on the (O) outputs. When (T) is High, outputs are high impedance (Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
T	D	C	O
1	X	X	Z
0	D	↑	D

Design Entry Method

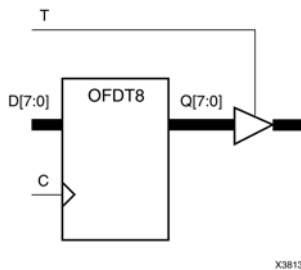
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OFDT8

Macro: 8-Bit D Flip-Flop with Active-Low 3-State Output Buffers



Introduction

This design element is a multiple D flip-flop whose output are enabled by 3-state buffers.

The data outputs (Q) of the flip-flops are connected to the inputs of output buffers (OBUFT). The outputs of the OBUFTs (O) are connected to OPADs or IOPADs. The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-Low enable inputs (T) are Low, the data on the flip-flop outputs (Q) appears on the (O) outputs. When (T) is High, outputs are high impedance (Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs
T	D	C	O
1	X	X	Z
0	D	↑	D

Design Entry Method

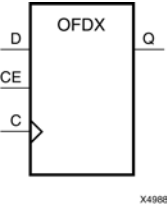
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OFDX

Macro: Output D Flip-Flop with Clock Enable



Introduction

This design element is a single output D flip-flop. The (Q) output is connected to OPAD or IOPAD. The data on the (D) input is loaded into the flip-flop during the Low-to-High clock (C) transition and appears on the (Q) output. When (CE) is Low, the flip-flop output does not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
CE	D	C	Q
1	Dn	↑	Dn
0	X	X	No change

Design Entry Method

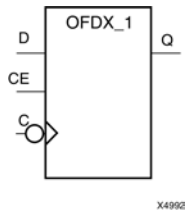
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OFDX_1

Macro: Output D Flip-Flop with Inverted Clock and Clock Enable



Introduction

The design element is located in an input/output block (IOB). The output (Q) of the (D) flip-flop is connected to an OPAD or an IOPAD. The data on the (D) input is loaded into the flip-flop during the High-to-Low clock (C) transition and appears on the (Q) output. When the (CE) pin is Low, the output (Q) does not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
CE	D	C	Q
1	D	↓	D
0	X	X	No Change

Design Entry Method

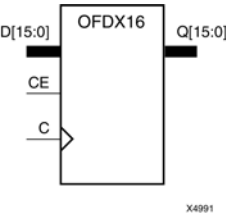
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OFDX16

Macro: 16-Bit Output D Flip-Flop with Clock Enable



Introduction

This design element is a multiple output D flip-flop. The (Q) output is connected to OPAD or IOPAD. The data on the (D) input is loaded into the flip-flop during the Low-to-High clock (C) transition and appears on the (Q) output. When (CE) is Low, the flip-flop output does not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs			Outputs
CE	D	C	Q
1	Dn	↑	Dn
0	X	X	No change

Design Entry Method

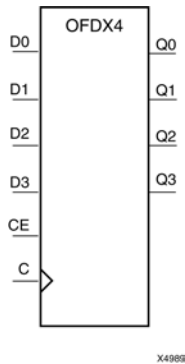
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OFDX4

Macro: 4-Bit Output D Flip-Flop with Clock Enable



Introduction

This design element is a multiple output D flip-flop. The (Q) output is connected to OPAD or IOPAD. The data on the (D) input is loaded into the flip-flop during the Low-to-High clock (C) transition and appears on the (Q) output. When (CE) is Low, the flip-flop output does not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs
CE	D	C	Q
1	Dn	↑	Dn
0	X	X	No change

Design Entry Method

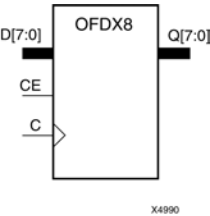
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OFDX8

Macro: 8-Bit Output D Flip-Flop with Clock Enable



Introduction

This design element is a multiple output D flip-flop. The (Q) output is connected to OPAD or IOPAD. The data on the (D) input is loaded into the flip-flop during the Low-to-High clock (C) transition and appears on the (Q) output. When (CE) is Low, the flip-flop output does not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs			Outputs
CE	D	C	Q
1	Dn	↑	Dn
0	X	X	No change

Design Entry Method

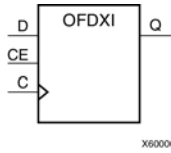
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OFDXI

Macro: Output D Flip-Flop with Clock Enable (Asynchronous Preset)



Introduction

The design element is contained in an input/output block (IOB). The output (Q) of the D flip-flop is connected to an OPAD or an IOPAD. The data on the (D) input is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). When (CE) is Low, the output does not change.

This flip-flop is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs
CE	D	C	Q
1	D	↑	D
0	X	X	No Change

Design Entry Method

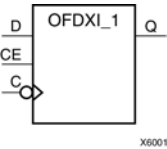
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OFDXI_1

Macro: Output D Flip-Flop with Inverted Clock and Clock Enable (Asynchronous Preset)



Introduction

The design element is located in an input/output block (IOB). The D flip-flop output (Q) is connected to an OPAD or an IOPAD. The data on the D input is loaded into the flip-flop during the High-to-Low clock (C) transition and appears on the Q output. When CE is Low, the output (Q) does not change.

This flip-flop is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
CE	D	C	Q
1	D	↓	D
0	X	X	No Change

Design Entry Method

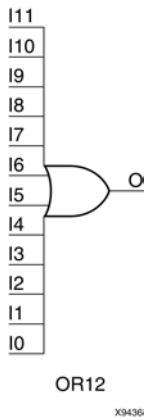
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OR12

Macro: 12-Input OR Gate with Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

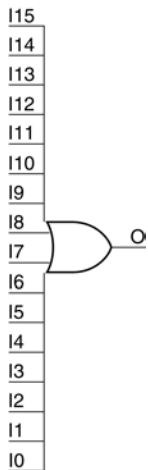
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OR16

Macro: 16-Input OR Gate with Non-Inverted Inputs



OR16

X9437

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

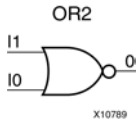
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OR2

Primitive: 2-Input OR Gate with Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

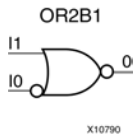
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OR2B1

Primitive: 2-Input OR Gate with 1 Inverted and 1 Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

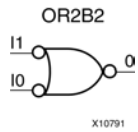
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OR2B2

Primitive: 2-Input OR Gate with Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

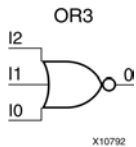
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OR3

Primitive: 3-Input OR Gate with Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

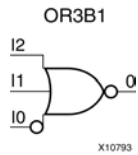
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OR3B1

Primitive: 3-Input OR Gate with 1 Inverted and 2 Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

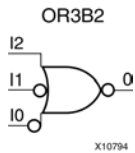
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OR3B2

Primitive: 3-Input OR Gate with 2 Inverted and 1 Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

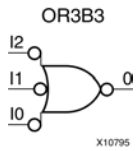
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OR3B3

Primitive: 3-Input OR Gate with Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

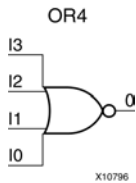
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OR4

Primitive: 4-Input OR Gate with Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

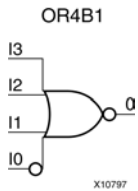
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OR4B1

Primitive: 4-Input OR Gate with 1 Inverted and 3 Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

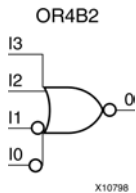
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OR4B2

Primitive: 4-Input OR Gate with 2 Inverted and 2 Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

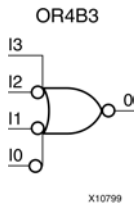
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OR4B3

Primitive: 4-Input OR Gate with 3 Inverted and 1 Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

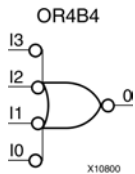
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OR4B4

Primitive: 4-Input OR Gate with Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

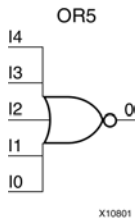
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OR5

Primitive: 5-Input OR Gate with Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

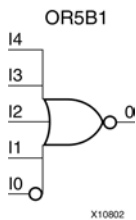
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OR5B1

Primitive: 5-Input OR Gate with 1 Inverted and 4 Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

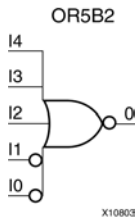
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OR5B2

Primitive: 5-Input OR Gate with 2 Inverted and 3 Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

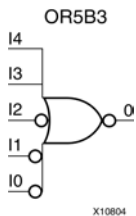
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OR5B3

Primitive: 5-Input OR Gate with 3 Inverted and 2 Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

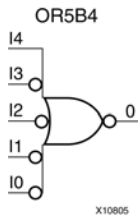
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OR5B4

Primitive: 5-Input OR Gate with 4 Inverted and 1 Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

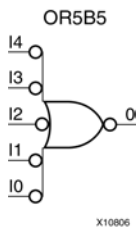
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OR5B5

Primitive: 5-Input OR Gate with Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

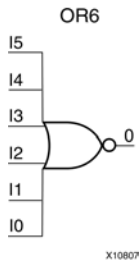
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OR6

Macro: 6-Input OR Gate with Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

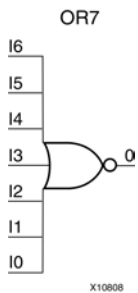
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OR7

Macro: 7-Input OR Gate with Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

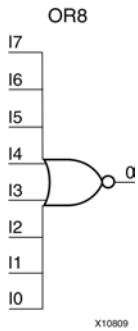
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OR8

Macro: 8-Input OR Gate with Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

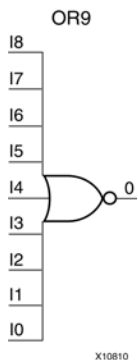
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OR9

Macro: 9-Input OR Gate with Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

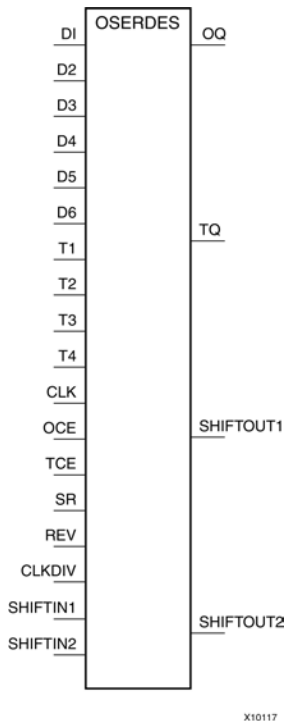
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

OSERDES

Primitive: Dedicated IOB Output Serializer



Introduction

Use the OSERDES primitive to easily implement a source synchronous interface. This device helps you by saving logic resources that would otherwise be implemented in the FPGA fabric. It also avoids additional timing complexities that you might encounter when you are designing circuitry in the FPGA fabric. This element contains multiple clock inputs to accommodate various applications, and will work in conjunction with SelectIO™ features.

Port Descriptions

Port	Type	Width	Function
OQ	Output	1	Data Path Output - This port is the data output of the OSERDES module. This port connects the output of the data parallel-to-serial converter to the data input of the IOB pad. In addition, this output port can also be configured to bypass all the submodules within the OSERDES module.
SHIFTOUT1-2	Output	1 (each)	Carry Out for data input expansion. Connect to SHIFTIN1/2 of master.
TQ	Output	1	3-State Path Output - This port is the 3-state output of the OSERDES module. This port connects the output of the 3-state parallel-to-serial converter to the control input of the IOB pad.
CLK	Input	1	High Speed Clock Input - This clock input is used to drive the parallel-to-serial converters. The possible source for the CLK port is from one of the following clock resources: <ul style="list-style-type: none"> Ten global clock lines in a clock region Four regional clock lines Four clock capable I/Os (within adjacent clock region)

Port	Type	Width	Function
			<ul style="list-style-type: none"> Fabric (through bypass)
CLKDIV	Input	1	Divided High Speed Clock Input - This clock input is used to drive the parallel-to-serial converter. This clock must be a divided down version of the clock connected to the CLK port. One of the following clock resources can be used as a source for CLKDIV: <ul style="list-style-type: none"> Ten global clock lines in a clock region Four regional clock lines
D1-D6	Input	1	Parallel Data Inputs - Ports D1 to D6 are the location in which all incoming parallel data enters the OSERDES module. This port is connected to the FPGA fabric, and can be configured from 2 to 6 bits. In the extended width mode, this port can be expanded up to 10 bits.
OCE	Input	1	Parallel to serial converter (data) clock enable - This port is used to enables the output of the data parallel-to-serial converter when asserted High.
SR	Input	1	Set/Reset Input - The set/reset (SR) pin forces the storage element into the state specified by the SRVAL attribute. SRVAL = "1" forces a logic 1. SRVAL = "0" forces a logic "0." The reset condition predominates over the set condition.
SHIFTIN1-2	Input	1 (each)	Carry Input for Data Input Expansion. Connect to SHIFTOUT1/2 of slave.
T1 - T4	Input	1 (each)	Parallel 3-State Inputs - Ports T1 to T4 are the location in which all parallel 3-state signals enters the OSERDES module. This port is connected to the FPGA fabric, and can be configured from 1 to 4 bits. This feature is not supported in the extended width mode.
TCE	Input	1	Parallel to serial converter (3-state) clock enable - This port is used to enable the output of the 3-state signal parallel-to-serial converter when asserted High.

Design Entry Method

This design element can be used in schematics.

The data parallel-to-serial converter in the OSERDES module takes in 2 to 6 bits of parallel data and converts them into serial data. Data input widths larger than 6 (7, 8, and 10) are achievable by cascading two OSERDES modules for data width expansion. In order to do this, one OSERDES must be set into a MASTER mode, while another is set into SLAVE mode. You must connect the SHIFTOUT of "slave" and SHIFTIN of "master" ports together. The "slave" only uses D3 to D6 ports as its input. The parallel-to-serial converter is available for both SDR and DDR modes.

This module is designed such that the data input at D1 port is the first output bit. This module is controlled by CLK and CLKDIV clocks. The following table describes the relationship between CLK and CLKDIV for both SDR and DDR mode.

SDR Data Width	DDR Data Width	CLK	CLKDIV
2	4	2X	X
3	6	3X	X
4	8	4X	X
5	10	5X	X
6	-	6X	X
7	-	7X	X
8	-	8X	X

Output of this block is connected to the data input of an IOB pad of the FPGA. This IOB pad can be configured to a desired standard using SelectIO.

Parallel-to-Serial Converter (3-state)

The 3-state parallel-to-serial converter in the OSERDES module takes in up to 4 bits of parallel 3-state signals and converts them into serial 3-state signal. Unlike the data parallel-to-serial converter, the 3-state parallel-to-serial converter is not extendable to more than 4-bit, 3-state signals. This module is primarily controlled by CLK and CLKDIV clocks. In order to use this module, the following attributes must be declared: DATA_RATE_TQ and TRISTATE_WIDTH. In certain cases, you can also need to declare DATA_RATE_OQ and DATA_WIDTH. The following table lists the attributes needed for the desired functionality.

Mode of Operation	DATA_RATE_TQ	TRISTATE_WIDTH
4-bit DDR*	DDR	4
1-bit SDR	SDR	1
Buffer	BUF	1

Output of this block is connected to the 3-state input of an IOB pad of the FPGA. This IOB pad can be configured to a desired standard using SelectIO.

Width Expansion

It is possible to use this element to transmit parallel data widths larger than six. However, the 3-state output is not expandable. In order to use this feature, *two* of these elements need to be instantiated, and the two must be an adjacent master and slave pair. The attribute MODE must be set to either "MASTER" or "SLAVE" in order to differentiate the modes of the OSERDES pair. In addition, you must connect the SHIFTIN ports of the MASTER to the SHIFTOUT ports of the SLAVE. This feature supports data widths of 7, 8, and 10 for SDR and DDR mode. The table below lists the data width availability for SDR and DDR mode.

Mode	Widths
SDR Data Widths	2,3,4,5,6,7,8
DDR Data Widths	4,6,8,10

Available Attributes

Attribute	Type	Allowed Values	Default	Description
DATA_RATE_OQ	String	"SDR", "DDR"	"DDR"	Defines whether the data changes at every clock edge or every positive clock edge with respect to CLK.
DATA_RATE_TQ	String	"BUF", "SDR", "DDR"	"DDR"	Defines whether the 3-state changes at every clock edge, every positive clock edge, or buffer configuration with respect to CLK.
DATA_WIDTH	Integer	2, 3, 4, 5, 6, 7, 8, or 10	4	If DATA_RATE_OQ = DDR, value is limited to 4, 6, 8, or 10. If DATA_RATE_OQ = SDR, value is limited to 2, 3, 4, 5, 6, 7, or 8.
INIT_OQ	Binary	0, 1	0	Defines the initial value of OQ output
INIT_TQ	Binary	0, 1	0	Defines the initial value of TQ output
SERDES_MODE	String	"MASTER", "SLAVE"	"MASTER"	Defines whether the OSERDES module is a master or slave when width expansion is used.
SRVAL_OQ	Binary	0, 1	0	Defines the value of OQ output when reset is invoked.

Attribute	Type	Allowed Values	Default	Description
SRVAL_TQ	Binary	0, 1	0	Defines the value of TQ output when reset is invoked.
TRISTATE_WIDTH	Integer	1, 2, 4	4	If DATA_RATE_TQ = DDR, value is limited to 2 or 4. The value can only be set to 1 when DATA_RATE_TQ = SDR or BUF.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

Primitive: PCI Express





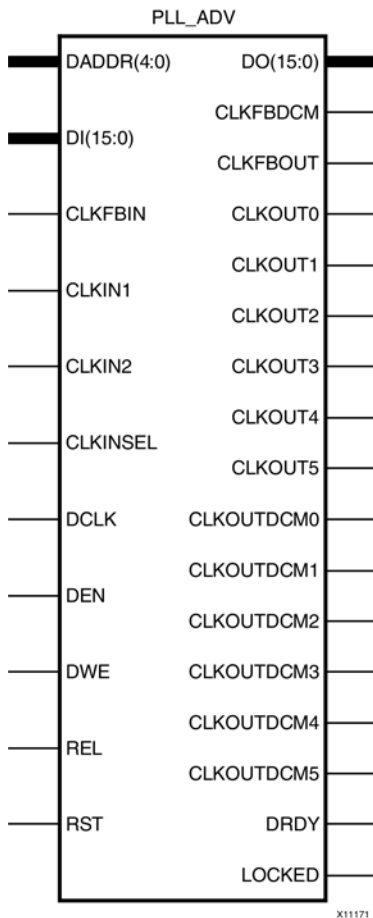
This design element is an Integrated Endpoint block embedded in Virtex®-5 devices. It leverages the PCI EXPRESS® (PCIe®) functionality that implements the next-generation evolution of the older PCI™ and PCI-X™ parallel bus standards. It is a high-performance, general-purpose interconnect architecture, designed for a wide range of computing and communications platforms. It is a packet-based, point-to-point serial interface that is backward compatible with PCI and PCI-X configurations, device drivers, and application software.

For More Information

- Virtex-5 Libraries Guide for Schematic Designs**
UG622 (v 11.3) September 16, 2009

PLL_ADV

Primitive: Advanced Phase Locked Loop Clock Circuit



Introduction

This design element is an embedded Phase Locked Loop Clock Circuit which provides added capabilities for clock synthesis and management within the FPGA as well as for circuits external to the FPGA. The PLL circuit allows the clock to be multiplexed, phase matched, phase shifted, multiplied, and divided as well as other features such as duty cycle modification and jitter filtering. The PLL can be used in conjunction with or in place of a DCM (Digital Clock Manager) component to control the clocking of the FPGA and other associated circuitry.

Port Descriptions

Port	Type	Width	Function
CLKFBDCM	Output	1	PLL Feedback used to compensate if the PLL is driving the DCM.
CLKFBIN	Input	1	Feedback clock input. Connection of this port needs to match the feedback mode attribute setting.
CLKFBOUT	Output	1	Dedicated PLL feedback output used to determine how the PLL compensates clock network delay. User configurable clock output that can be a divided version of the VCO phase outputs (user controllable) from 1 (bypassed) to 128. The phase relationship relative to the input clock and output clocks is guaranteed by the design.

Port	Type	Width	Function
CLKINSEL	Input	1	Signal from core routing that controls the state of the input mux, high = CLKIN1, low = CLKIN2
CLKIN1	Input	1	Input clock
CLKIN2	Input	1	Secondary clock input to facilitate allowing customers to dynamically switch the reference clock to the PLL.
CLKOUTDCM0	Output	1	User configurable clock that can only connect to the DCM within the same CMT as the PLL.
CLKOUTDCM1 - CLKOUTDCM5	Output	1	User configurable clock output that can be a divided version of the VCO phase outputs (user controllable) from 1 (bypassed) to 128. The phase relationship relative to the input clock and output clocks is guaranteed by the design.
CLKOUT0 - CLKOUT5	Output	1	User configurable clock output that can be a divided version of the VCO phase outputs (user controllable) from 1 (bypassed) to 128. The phase relationship relative to the input clock and output clocks is guaranteed by the design.
DADDR[4:0]	Input	5	Provides a reconfiguration address for the dynamic reconfiguration. When not used, all bits must be assigned zeros.
DCLK	Input	1	Reference clock for the dynamic reconfiguration port.
DEN	Input	1	Provides the enable control signal to access the dynamic reconfiguration feature. When the dynamic reconfiguration feature is not used, DEN must be tied low. When DEN is tied low, the DO outputs reflect the status signals.
DI[15:0]	Input	16	Provides reconfiguration data. When not used, all bits must be set to zeros.
DO[15:0]	Output	16	Provides PLL status or data output when using dynamic reconfiguration. For the DO bus to represent the PLL status, the following connections are required: DEN must be tied to GND. DWE must be tied to GND. DADDR bus must be all zeros. DI bus must be all zeros.
DRDY	Output	1	Provides the response to the DEN signal for the PLL dynamic reconfiguration feature.
DWE	Input	1	Provides the write enable control signal to write the DI data into the DADDR address. When not used, it must be tied low.
LOCKED	Output	1	Synchronous output from the PLL that provides the user with an indication the PLL has achieved phase alignment within a pre-defined window and frequency matching within a predefined ppm range.
REL	Input	1	Unused.
RST	Input	1	Reset.

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Type	Allowed_Values	Default	Description
BANDWIDTH	String	"OPTIMIZED", "HIGH", "LOW"	"OPTIMIZED"	<p>PLL bandwidth control, sets the PLL bandwidth.</p> <ul style="list-style-type: none"> HIGH sets the PLL programming algorithm to the highest setting possible while maintaining good PLL performance (i.e. low jitter, low jitter peaking, maximum phase margin). LOW sets the PLL algorithm to the lowest setting possible while maintaining good PLL performance.
CLKFBOUT_ DESKEW_ ADJUST	String	"NONE", "1", "2", "3", "4", "5", "6", "7", "8", "9", "10", "11", "12", "13", "14", "15", "16", "17", "18", "19", "20", "21", "22", "23", "24", "25", "26", "27", "28", "29", "30", "31"	"NONE"	See appropriate user guide.

Attribute	Type	Allowed_Values	Default	Description
CLKFBOUT_MULT	Integer	1 to 64	1	Counter multiply value, always configured for 50% duty cycle.
CLKFBOUT_PHASE	1 significant digit Float	0.0 to 360.0	0.0	Counter output phase relative to the output clock.
CLK_FEEDBACK	String	"CLKFBOUT", "CLKOUT0"	"CLKFBOUT"	Clock source to drive CLKFB_IN.
CLKIN1_PERIOD - CLKIN2_PERIOD	String	0 bit String	"0"	The reference clock frequency is required for properly configuring the LOCK detect circuit and checking to make sure the VCO is operating within the allowed range. If no value is specified, a warning will be issued stating it was not provided so no error checking is done. Real in nanoseconds, with 0.001 ns resolution.
CLKOUT0_DESKEW_ ADJUST - CLKOUT5_DESKEW_ ADJUST	String	"NONE", "1", "2", "3", "4", "5", "6", "7", "8", "9", "10", "11", "12", "13", "14", "15", "16", "17", "18", "19", "20", "21", "22", "23", "24", "25", "26", "27", "28", "29", "30", "31"	"NONE"	For backward compatibility. Not used for Spartan®-6.
CLKOUT0_DIVIDE - CLKOUT5_DIVIDE	Integer	1 to 128	1	Counter divide value
CLKOUT0_DUTY_ CYCLE - CLKOUT5_DUTY_ CYCLE	2 significant digit Float	0.01 to 0.99	0.50	Counter output duty cycle
CLKOUT0_PHASE - CLKOUT5_PHASE	1 significant digit Float	0.0 to 360.0	0.0	Counter output phase relative to the output clock.

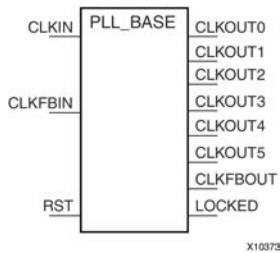
Attribute	Type	Allowed_Values	Default	Description
COMPENSATION	String	"SYSTEM_SYNCHRONOUS", "SOURCE_SYNCHRONOUS"	"SYSTEM_SYNCHRONOUS"	Specifies the PLL phase compensation for the incoming clock. <ul style="list-style-type: none"> SYSTEM_SYNCHRONOUS - attempts to compensate all clock delay for 0 hold time. SOURCE_SYNCHRONOUS - Used when a clock is provided with data and thus phased with the clock.
DIVCLK_DIVIDE	Integer	1 to 52	1	Counter divide value, always configured for 50% duty cycle.
EN_REL	Boolean	FALSE, TRUE	FALSE	For backward compatibility. Not used for Spartan-6.
PLL_PMCD_MODE	Boolean	FALSE, TRUE	FALSE	For backward compatibility. Not used for Spartan-6.
REF_JITTER	3 significant digit Float	0.000 to 1.000	0.100	The reference clock jitter is specified in terms of the UI which is a percentage of the reference clock. The number provided should be the maximum peak to peak value our part can expect on the input clock. Default is 0.1UI or equivalent UI based on the value of the REF_CLK_FREQ, DIVCLK_DIVIDE, and REF_CLK_JITTER_MAX (in the PLL_SPEED_FILE.xls). This parameter should support out to three decimal places.
RESET_ON_LOSS_OF_LOCK	Boolean	FALSE, TRUE	FALSE	For backward compatibility. Not used for Spartan-6.
RST_DEASSERT_CLK	String	"CLKIN1", "CLKFBIN"	"CLKIN1"	For backward compatibility. Not used for Spartan-6.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

PLL_BASE

Primitive: Basic Phase Locked Loop Clock Circuit



Introduction

This design element is a direct sub-set of the PLL_ADV design element, an embedded Phase Locked Loop clock circuit that provides added capabilities for clock synthesis and management both within the FPGA and in circuits external to the FPGA. The PLL_BASE is provided in order to ease the integration for most PLL clocking circuits. However, this primitive does not contain all of the functionality that the PLL can possibly provide. This component allows the input clock to be phase shifted, multiplied and divided, and supports other features, such as modification of the duty cycle and jitter filtering.

Port Descriptions

Port	Direction	Width	Function
Clock Outputs/Inputs			
CLKOUT0-5	Output	1	One of six phase controlled output clocks from the PLL.
CLKFBOUT	Output	1	Dedicated PLL feedback output used to determine how the PLL compensates clock network delay. Depending on the type of compensation desired, this output might or might not need to be connected.
CLKIN	Input	1	Clock source input to the PLL. This pin can be driven by a dedicated clock pin to the FPGA, a DCM output clock pin, or a BUFG output.
CLKFBIN	Input	1	Clock feedback input. This pin should only be sourced from the CLKFBOUT port.
Status Outputs/Control Inputs			
LOCKED	Output	1	Synchronous output from the PLL that provides you with an indication the PLL has achieved phase alignment and is ready for operation.
RST	Input	1	Asynchronous reset of the PLL.

Design Entry Method

This design element can be used in schematics.

Available Attributes

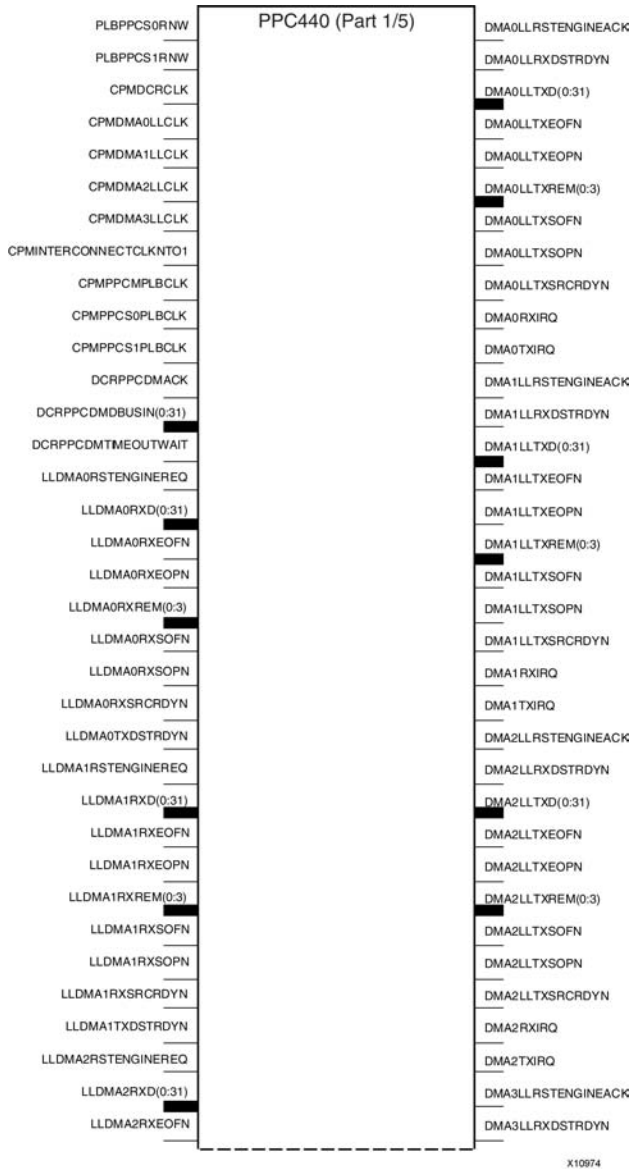
Attribute	Type	Allowed Values	Default	Description
COMPENSATION	String	"SYSTEM_SYNCHRONOUS", "SOURCE_SYNCHRONOUS"	"SYSTEM_SYNCHRONOUS"	Specifies the PLL phase compensation for the incoming clock. SYSTEM_SYNCHRONOUS attempts to compensate all clock delay while SOURCE_SYNCHRONOUS is used when a clock is provided with data and thus phased with the clock.
BANDWIDTH	String	"HIGH", "LOW", "OPTIMIZED"	"OPTIMIZED"	Specifies the PLL programming algorithm affecting the jitter, phase margin and other characteristics of the PLL.
CLKOUT0_DIVIDE, CLKOUT1_DIVIDE, CLKOUT2_DIVIDE, CLKOUT3_DIVIDE, CLKOUT4_DIVIDE, CLKOUT5_DIVIDE	Integer	1 to 128	1	Specifies the amount to divide the associated CLKOUT clock output if a different frequency is desired. This number in combination with the FBCLKOUT_MULT value determines the output frequency.
CLKOUT0_PHASE, CLKOUT1_PHASE, CLKOUT2_PHASE, CLKOUT3_PHASE, CLKOUT4_PHASE, CLKOUT5_PHASE	Real	0.01 to 360.0	0.0	Allows specification of the output phase relationship of the associated CLKOUT clock output in number of degrees offset (i.e. 90 indicates a 90 degree or ¼ cycle offset phase offset while 180 indicates a 180 degree offset or ½ cycle phase offset).
CLKOUT0_DUTY_CYCLE, CLKOUT1_DUTY_CYCLE, CLKOUT2_DUTY_CYCLE, CLKOUT3_DUTY_CYCLE, CLKOUT4_DUTY_CYCLE, CLKOUT5_DUTY_CYCLE,	Real	0.01 to 0.99	0.50	Specifies the Duty Cycle of the associated CLKOUT clock output in percentage (i.e. 0.50 generates a 50% duty cycle).
CLKFBOUT_MULT	Integer	1 to 64	1	Specifies the amount to multiply all CLKOUT clock outputs if a different frequency is desired. This number in combination with the associated CLKOUT#_DIVIDE value determines the output frequency.
DIVCLK_DIVIDE	Integer	1 to 52	1	Specifies the division ratio for all output clocks.
CLKFBOUT_PHASE	Real	0.0 to 360	0.0	Specifies the phase offset in degrees of the clock feedback output.
REF_JITTER	Real	0.000 to 0.999	0.100	The reference clock jitter is specified in terms of the UI which is a percentage of the reference clock. The number provided should be the maximum peak to peak value on the input clock.
CLKIN_PERIOD	Real	1.000 to 52.630	0.000	Specified the input period in ns to the PLL CLKIN input.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

PPC440

Primitive: Power PC 440 CPU Core

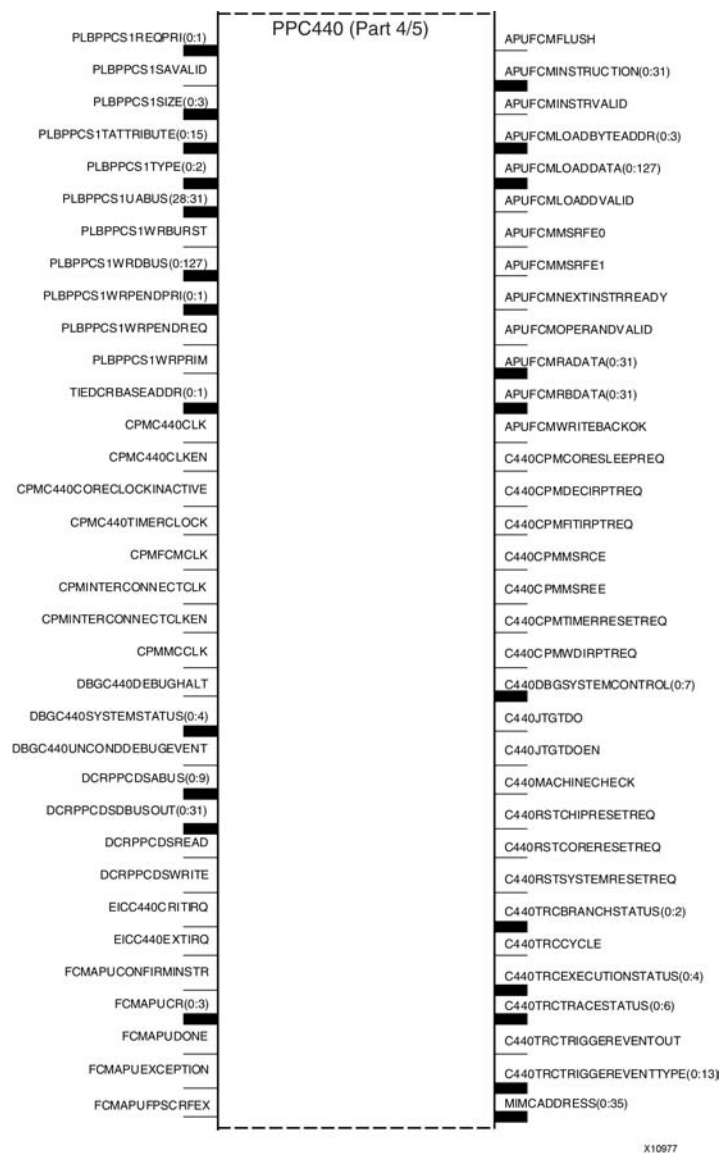


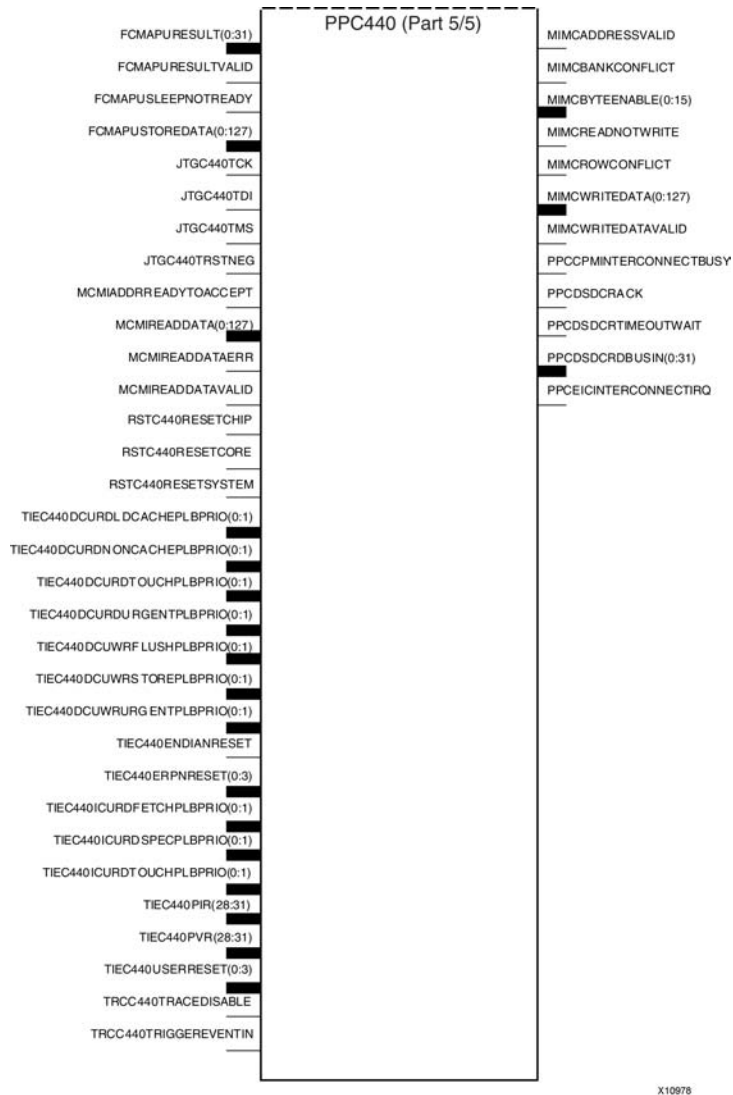
PPC440 (Part 2/5)		
LLDMA2RXEOPN		DMA3LLTXD(0:31)
LLDMA2RXREM(0:3)		DMA3LLTXEOFN
LLDMA2RXSOFN		DMA3LLTXEOPN
LLDMA2RXSOPN		DMA3LLTXREM(0:3)
LLDMA2RXSRCRDYN		DMA3LLTXSOFN
LLDMA2TXDSTRDYN		DMA3LLTXSOPN
LLDMA3RSTENGINEREQ		DMA3LLTXSRCRDYN
LLDMA3RXD(0:31)		DMA3RXIRQ
LLDMA3RXEOFN		DMA3TXIRQ
LLDMA3RXEOPN		PPCDMDCRABUS(0:9)
LLDMA3RXREM(0:3)		PPCDMDCRDBUSOUT(0:31)
LLDMA3RXSOFN		PPCDMDCRRE AD
LLDMA3RXSOPN		PPCDMDCRUABUS(20:21)
LLDMA3RXSRCRDYN		PPCDMDCRWRITE
LLDMA3TXDSTRDYN		PPCMPLBABORT
PLBPPCMADDRACK		PPCMPLBABUS(0:31)
PLBPPCMMBUSY		PPCMPLBBE(0:15)
PLBPPCMMIQ		PPCMPLBBSLOCK
PLBPPCMRDERR		PPCMPLBLOCKERR
PLBPPCMWRERR		PPCMPLBPRIORITY(0:1)
PLBPPCMRDBTERM		PPCMPLBRDBURST
PLBPPCMRDACK		PPCMPLBREQUEST
PLBPPCMRDBBUS(0:127)		PPCMPLBRNW
PLBPPCMRDPENDPRI(0:1)		PPCMPLBSIZE(0:3)
PLBPPCMRDPENDREQ		PPCMPLBTATTRIBUTE(0:15)
PLBPPCMRDWDADDR(0:3)		PPCMPLBTTYPE(0:2)
PLBPPCMREARBITRATE		PPCMPLBUABUS(28:31)
PLBPPCMREQPRI(0:1)		PPCMPLBWBURST
PLBPPCMSIZE(0:1)		PPCMPLBWRDBUS(0:127)
PLBPPCMTIMEOUT		PPCS0PLBADDRACK
PLBPPCMWRBTERM		PPCS0PLBMBUSY(0:3)
PLBPPCMWRDACK		PPCS0PLBMIRQ(0:3)
PLBPPCMWRDPENDPRI(0:1)		PPCS0PLBMRDERR(0:3)
PLBPPCMWRDPENDREQ		PPCS0PLBMWRERR(0:3)

X10975

PPC440 (Part 3/5)		
PLBPPCS0ABORT		PPCS0PLBRDBTERM
PLBPPCS0ABUS(0:31)		PPCS0PLBRDCOMP
PLBPPCS0BE(0:15)		PPCS0PLBRDDACK
PLBPPCS0BUSLOCK		PPCS0PLBRDDBUS(0:127)
PLBPPCS0LOCKERR		PPCS0PLBRDWDADDR(0:3)
PLBPPCS0MASTERID(0:1)		PPCS0PLBREARBITRATE
PLBPPCS0MSIZE(0:1)		PPCS0PLBSSIZE(0:1)
PLBPPCS0PAVALID		PPCS0PLBWAIT
PLBPPCS0RDBURST		PPCS0PLBWRBTERM
PLBPPCS0RDPENDPRI(0:1)		PPCS0PLBWRCOMP
PLBPPCS0RDPENDREQ		PPCS0PLBWRDACK
PLBPPCS0RDPRIM		PPCS1PLBADDRACK
PLBPPCS0REQPRI(0:1)		PPCS1PLBMBUSY(0:3)
PLBPPCS0SAVALID		PPCS1PLBMIRQ(0:3)
PLBPPCS0SIZE(0:3)		PPCS1PLBMRDERR(0:3)
PLBPPCS0TATTRIBUTE(0:15)		PPCS1PLBMRERR(0:3)
PLBPPCS0TYPE(0:2)		PPCS1PLBRDBTERM
PLBPPCS0UABUS(28:31)		PPCS1PLBRDCOMP
PLBPPCS0WRBURST		PPCS1PLBRDDACK
PLBPPCS0WRDDBUS(0:127)		PPCS1PLBRDDBUS(0:127)
PLBPPCS0WRPENDPRI(0:1)		PPCS1PLBRDWDADDR(0:3)
PLBPPCS0WRPENDREQ		PPCS1PLBREARBITRATE
PLBPPCS0WRPRIM		PPCS1PLBSSIZE(0:1)
PLBPPCS1ABORT		PPCS1PLBWAIT
PLBPPCS1ABUS(0:31)		PPCS1PLBWRBTERM
PLBPPCS1BE(0:15)		PPCS1PLBWRCOMP
PLBPPCS1BUSLOCK		PPCS1PLBWRDACK
PLBPPCS1LOCKERR		APUFMDECFPUOP
PLBPPCS1MASTERID(0:1)		APUFMDECLDSTXFERSIZE(0:2)
PLBPPCS1MSIZE(0:1)		APUFMDECLDLOAD
PLBPPCS1PAVALID		APUFMDECNONAUTON
PLBPPCS1RDBURST		APUFMDECSTORE
PLBPPCS1RDPENDPRI(0:1)		APUFMDECUDI(0:3)
PLBPPCS1RDPENDREQ		APUFMDECUDIVALID
PLBPPCS1RDPRIM		APUFMENDIAN

X10976





Introduction

This design element is a dual issue, superscalar processor that provides significant performance improvement over the older PowerPC® 405 while implementing the same instruction set architecture.

Design Entry Method

This design element can be used in schematics.

For More Information

- See the [IBM PPC440x5 CPU Core User's Manual](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).
- See the [Virtex-5 FPGA User Guide](#).

PULLDOWN

Primitive: Resistor to GND for Input Pads, Open-Drain, and 3-State Outputs

PULLDOWN



Introduction

This resistor element is connected to input, output, or bidirectional pads to guarantee a logic Low level for nodes that might float.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Pulldown output (connect directly to top level port)

Design Entry Method

This design element can be used in schematics.

This element can be connected to a net in the following locations on a top-level schematic file:

- A net connected to an input IO Marker.
- A net connected to both an output IO Marker and 3-statable IO element, such as an OBUFT.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

PULLUP

Primitive: Resistor to VCC for Input PADS, Open-Drain, and 3-State Outputs



Introduction

This design element allows for an input, 3-state output or bi-directional port to be driven to a weak high value when not being driven by an internal or external source. This element establishes a High logic level for open-drain elements and macros when all the drivers are off.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Pullup output (connect directly to top level port)

Design Entry Method

This design element can be used in schematics.

This element can be connected to a net in the following locations on a top-level schematic file:

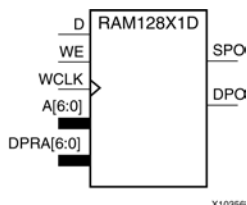
- A net connected to an input IO Marker
- A net connected to both an output IO Marker and 3-statable IO element, such as an OBUFT.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

RAM128X1D

Primitive: 128-Deep by 1-Wide Dual Port Random Access Memory (Select RAM)



Introduction

This design element is a 128-bit deep by 1-bit wide random access memory and has a read/write port that writes the value on the D input data pin when the write enable (WE) is high to the location specified by the A address bus. This happens shortly after the rising edge of the WCLK and that same value is reflected in the data output SPO. When WE is low, an asynchronous read is initiated in which the contents of the memory location specified by the A address bus is output asynchronously to the SPO output. The read port can perform asynchronous read access of the memory by changing the value of the address bus DPRA, and by outputting that value to the DPO data output.

Port Descriptions

Port	Direction	Width	Function
SPO	Output	1	Read/Write port data output addressed by A
DPO	Output	1	Read port data output addressed by DPRA
D	Input	1	Write data input addressed by A
A	Input	7	Read/Write port address bus
DPRA	Input	7	Read port address bus
WE	Input	1	Write Enable
WCLK	Input	1	Write clock (reads are asynchronous)

If instantiated, the following connections should be made to this component:

- Tie the WCLK input to the desired clock source, the D input to the data source to be stored and the DPO output to an FDCE D input or other appropriate data destination.
- Optionally, the SPO output can also be connected to the appropriate data destination or else left unconnected.
- The WE clock enable pin should be connected to the proper write enable source in the design.
- The 7-bit A bus should be connected to the source for the read/write addressing and the 7-bit DPRA bus should be connected to the appropriate read address connections.
- An optional INIT attribute consisting of a 128-bit Hexadecimal value can be specified to indicate the initial contents of the RAM.

If left unspecified, the initial contents default to all zeros.

Design Entry Method

This design element can be used in schematics.

Available Attributes

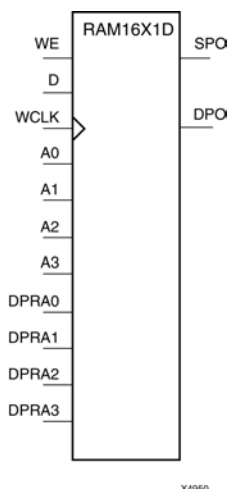
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 128-Bit Value	All zeros	Specifies the initial contents of the RAM.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

RAM16X1D

Primitive: 16-Deep by 1-Wide Static Dual Port Synchronous RAM



Introduction

This element is a 16-word by 1-bit static dual port random access memory with synchronous write capability. The device has two address ports: the read address (DPRA3:DPRA0) and the write address (A3:A0). These two address ports are asynchronous. The read address controls the location of the data driven out of the output pin (DPO), and the write address controls the destination of a valid write transaction. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected.

When WE is High, any positive transition on (WCLK) loads the data on the data input (D) into the word selected by the 4-bit write address. For predictable performance, write address and data inputs must be stable before a Low-to-High (WCLK) transition. This RAM block assumes an active-High (WCLK). (WCLK) can be active-High or active-Low. Any inverter placed on the (WCLK) input net is absorbed into the block.

The SPO output reflects the data in the memory cell addressed by A3:A0. The DPO output reflects the data in the memory cell addressed by DPRA3:DPRA0.

Note The write process is not affected by the address on the read address port.

You can use the INIT attribute to directly specify an initial value. The value must be a hexadecimal number, for example, INIT=ABAC. If the INIT attribute is not specified, the RAM is initialized with all zeros.

Logic Table

Mode selection is shown in the following logic table:

Inputs			Outputs	
WE (mode)	WCLK	D	SPO	DPO
0 (read)	X	X	data_a	data_d
1 (read)	0	X	data_a	data_d
1 (read)	1	X	data_a	data_d
1 (write)	↑	D	D	data_d
1 (read)	↓	X	data_a	data_d
data_a = word addressed by bits A3-A0				
data_d = word addressed by bits DPRA3-DPRA0				

Design Entry Method

This design element can be used in schematics.

Available Attributes

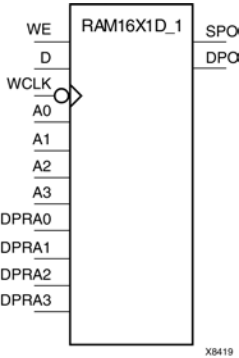
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros.	Initializes RAMs, registers, and look-up tables.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

RAM16X1D_1

Primitive: 16-Deep by 1-Wide Static Dual Port Synchronous RAM with Negative-Edge Clock



Introduction

This is a 16-word by 1-bit static dual port random access memory with synchronous write capability and negative-edge clock. The device has two separate address ports: the read address (DPRA3:DPRA0) and the write address (A3:A0). These two address ports are asynchronous. The read address controls the location of the data driven out of the output pin (DPO), and the write address controls the destination of a valid write transaction.

When the write enable (WE) is set to Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When (WE) is High, any negative transition on (WCLK) loads the data on the data input (D) into the word selected by the 4-bit write address. For predictable performance, write address and data inputs must be stable before a High-to-Low WCLK transition. This RAM block assumes an active-High (WCLK). (WCLK) can be active-High or active-Low. Any inverter placed on the (WCLK) input net is absorbed into the block.

You can initialize RAM16X1D_1 during configuration using the INIT attribute.

The SPO output reflects the data in the memory cell addressed by A3:A0. The DPO output reflects the data in the memory cell addressed by DPRA3:DPRA0.

Note The write process is not affected by the address on the read address port.

Logic Table

Mode selection is shown in the following logic table:

Inputs			Outputs	
WE (mode)	WCLK	D	SPO	DPO
0 (read)	X	X	data_a	data_d
1 (read)	0	X	data_a	data_d
1 (read)	1	X	data_a	data_d
1 (write)	↓	D	D	data_d
1 (read)	↑	X	data_a	data_d
data_a = word addressed by bits A3:A0				
data_d = word addressed by bits DPRA3:DPRA0				

Port Descriptions

Port	Direction	Width	Function
DPO	Output	1	Read-only 1-Bit data output
SPO	Output	1	R/W 1-Bit data output
A0	Input	1	R/W address[0] input
A1	Input	1	R/W address[1] input
A2	Input	1	R/W address[2] input
A3	Input	1	R/W address[3] input
D	Input	1	Write 1-Bit data input
DPRA0	Input	1	Read-only address[0] input
DPRA1	Input	1	Read-only address[1] input
DPRA2	Input	1	Read-only address[2] input
DPRA3	Input	1	Read-only address[3] input
WCLK	Input	1	Write clock input
WE	Input	1	Write enable input

Design Entry Method

This design element can be used in schematics.

Available Attributes

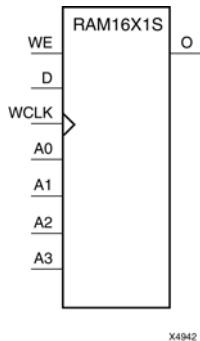
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Initializes RAMs, registers, and look-up tables.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

RAM16X1S

Primitive: 16-Deep by 1-Wide Static Synchronous RAM



Introduction

This element is a 16-word by 1-bit static random access memory with synchronous write capability. When the write enable (WE) is set Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is set High, any positive transition on WCLK loads the data on the data input (D) into the word selected by the 4-bit address (A3:A0). This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins. You can initialize RAM16X1S during configuration using the INIT attribute.

Logic Table

Inputs			Outputs
WE(mode)	WCLK	D	O
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D	D
1 (read)	↓	X	Data
Data = word addressed by bits A3:A0			

Design Entry Method

This design element can be used in schematics.

Available Attributes

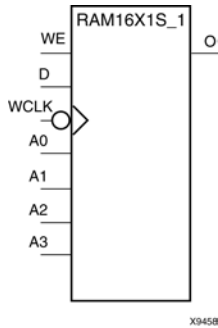
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Specifies initial contents of the RAM.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

RAM16X1S_1

Primitive: 16-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock



Introduction

This element is a 16-word by 1-bit static random access memory with synchronous write capability and negative-edge clock. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When (WE) is High, any negative transition on (WCLK) loads the data on the data input (D) into the word selected by the 4-bit address (A3:A0). For predictable performance, address and data inputs must be stable before a High-to-Low WCLK transition. This RAM block assumes an active-Low (WCLK). However, (WCLK) can be active-High or active-Low. Any inverter placed on the (WCLK) input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins.

You can initialize this element during configuration using the INIT attribute.

Logic Table

Inputs			Outputs
WE(mode)	WCLK	D	O
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↓	D	D
1 (read)	↑	X	Data
Data = word addressed by bits A3:A0			

Design Entry Method

This design element can be used in schematics.

Available Attributes

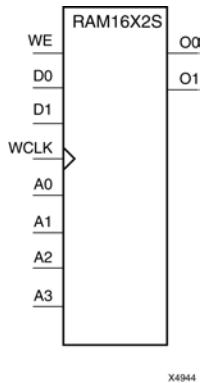
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Specifies initial contents of the RAM.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

RAM16X2S

Primitive: 16-Deep by 2-Wide Static Synchronous RAM



Introduction

This element is a 16-word by 2-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D1:D0) into the word selected by the 4-bit address (A3:A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pins (O1:O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

You can use the INIT_xx properties to specify the initial contents of a wide RAM. INIT_00 initializes the RAM cells corresponding to the O0 output, INIT_01 initializes the cells corresponding to the O1 output, etc. For example, a RAM16X2S instance is initialized by INIT_00 and INIT_01 containing 4 hex characters each. A RAM16X8S instance is initialized by eight properties INIT_00 through INIT_07 containing 4 hex characters each. A RAM64x2S instance is completely initialized by two properties INIT_00 and INIT_01 containing 16 hex characters each.

Except for Virtex-4 devices, the initial contents of this element cannot be specified directly.

Logic Table

Inputs			Outputs
WE (mode)	WCLK	D1:D0	O1:O0
0 (read)	X	X	Data
1(read)	0	X	Data
1(read)	1	X	Data
1(write)	↑	D1:D0	D1:D0
1(read)	↓	X	Data
Data = word addressed by bits A3:A0			

Design Entry Method

This design element can be used in schematics.

Available Attributes

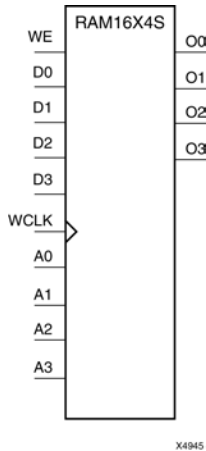
Attribute	Type	Allowed Values	Default	Description
INIT_00 to INIT_01	Hexadecimal	Any 16-Bit Value	All zeros	Initializes RAMs, registers, and look-up tables.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

RAM16X4S

Primitive: 16-Deep by 4-Wide Static Synchronous RAM



Introduction

This element is a 16-word by 4-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D3:D0) into the word selected by the 4-bit address (A3:A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pins (O3:O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

Logic Table

Inputs			Outputs
WE (mode)	WCLK	D3:D0	O3:O0
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D3:D0	D3:D0
1 (read)	↓	X	Data
Data = word addressed by bits A3:A0.			

Design Entry Method

This design element can be used in schematics.

Available Attributes

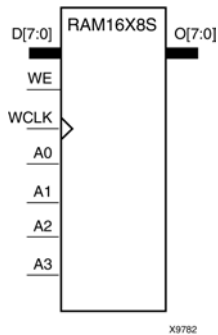
Attribute	Type	Allowed Values	Default	Description
INIT_00 to INIT_03	Hexadecimal	Any 16-Bit Value	All zeros	INIT for bit 0 of RAM

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

RAM16X8S

Primitive: 16-Deep by 8-Wide Static Synchronous RAM



Introduction

This element is a 16-word by 8-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on data inputs (D7:D0) into the word selected by the 4-bit address (A3:A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pins (O7:O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

Logic Table

Inputs			Outputs
WE (mode)	WCLK	D7:D0	O7:O0
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D7:D0	D7:D0
1 (read)	↓	X	Data
Data = word addressed by bits A3–A0			

Design Entry Method

This design element can be used in schematics.

Available Attributes

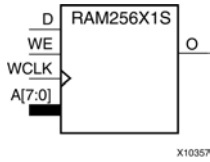
Attribute	Type	Allowed Values	Default	Description
INIT_00 to INIT_07	Hexadecimal	Any 16-Bit Value	All zeros	Initializes RAMs, registers, and look-up tables.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

RAM256X1S

Primitive: 256-Deep by 1-Wide Random Access Memory (Select RAM)



Introduction

This design element is a 256-bit deep by 1-bit wide random access memory with synchronous write and asynchronous read capability. This RAM is implemented using the LUT resources of the device (also known as Select RAM), and does not consume any of the block RAM resources of the device. If a synchronous read capability is preferred, a register can be attached to the output and placed in the same slice as long as the same clock is used for both the RAM and the register. The RAM256X1S has an active, High write enable, WE, so that when that signal is High, and a rising edge occurs on the WCLK pin, a write is performed recording the value of the D input data pin into the memory array. The output O displays the contents of the memory location addressed by A, regardless of the WE value. When a write is performed, the output is updated to the new value shortly after the write completes.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Read/Write port data output addressed by A
D	Input	1	Write data input addressed by A
A	Input	8	Read/Write port address bus
WE	Input	1	Write Enable
WCLK	Input	1	Write clock (reads are asynchronous)

Design Entry Method

If instantiated, the following connections should be made to this component:

- Tie the WCLK input to the desired clock source, the D input to the data source to be stored, and the O output to an FDCE D input or other appropriate data destination.
- The WE clock enable pin should be connected to the proper write enable source in the design.
- The 8-bit A bus should be connected to the source for the read/write.
- An optional INIT attribute consisting of a 256-bit Hexadecimal value can be specified to indicate the initial contents of the RAM.

If left unspecified, the initial contents default to all zeros.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 256-Bit Value	All zeros	Specifies the initial contents of the RAM.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

RAM32M

Primitive: 32-Deep by 8-bit Wide Multi Port Random Access Memory (Select RAM)



Introduction

This design element is a 32-bit deep by 8-bit wide, multi-port, random access memory with synchronous write and asynchronous independent, 2-bit, wide-read capability. This RAM is implemented using the LUT resources of the device known as SelectRAM™, and does not consume any of the Block RAM resources of the device. The RAM32M is implemented in a single slice and consists of one 8-bit write, 2-bit read port and three separate 2-bit read ports from the same memory. This configuration allows for byte-wide write and independent 2-bit read access RAM. If the DIA, DIB, DIC and DID inputs are all tied to the same data inputs, the RAM can become a 1 read/write port, 3 independent read port, 32x2 quad port memory. If DID is grounded, DOD is not used, while ADDRA, ADDRb and ADDRc are tied to the same address, the RAM becomes a 32x6 simple dual port RAM. If ADDRd is tied to ADDRA, ADDRb, and ADDRc, then the RAM is a 32x8 single port RAM. There are several other possible configurations for this RAM.

Port Descriptions

Port	Direction	Width	Function
DOA	Output	2	Read port data outputs addressed by ADDRA
DOB	Output	2	Read port data outputs addressed by ADDRb
DOC	Output	2	Read port data outputs addressed by ADDRc
DOD	Output	2	Read/Write port data outputs addressed by ADDRd
DIA	Input	2	Write data inputs addressed by ADDRd (read output is addressed by ADDRA)
DIB	Input	2	Write data inputs addressed by ADDRd (read output is addressed by ADDRb)
DIC	Input	2	Write data inputs addressed by ADDRd (read output is addressed by ADDRc)
DID	Input	2	Write data inputs addressed by ADDRd
ADDRA	Input	5	Read address bus A
ADDRb	Input	5	Read address bus B
ADDRc	Input	5	Read address bus C
ADDRd	Input	5	8-bit data write port, 2-bit data read port address bus D
WE	Input	1	Write Enable
WCLK	Input	1	Write clock (reads are asynchronous)

Design Entry Method

This design element can be used in schematics.

This element can be inferred by some synthesis tools by describing a RAM with a synchronous write and asynchronous read capability. Consult your synthesis tool documentation for details on RAM inference capabilities and coding examples. Xilinx suggests that you instantiate RAM32Ms if you have a need to implicitly specify the RAM function, or if you need to manually place or relationally place the component. If a synchronous read capability is desired, the RAM32M outputs can be connected to an FDRSE (FDCPE is asynchronous set/reset is necessary) in order to improve the output timing of the function. However, this is not necessary for the proper operation of the RAM.

If you want to have the data clocked on the negative edge of a clock, an inverter can be described on the clock input to this component. This inverter will be absorbed into the block, giving you the ability to write to the RAM on falling clock edges.

If instantiated, the following connections should be made to this component. Tie the WCLK input to the desired clock source, the DIA, DIB, DIC and DID inputs to the data source to be stored and the DOA, DOB, DOC and DOD outputs to an FDCE D input or other appropriate data destination or left unconnected if not used. The WE clock enable pin should be connected to the proper write enable source in the design. The 5-bit ADDR bus should be connected to the source for the read/write addressing and the 5-bit ADDRA, ADDRb and ADDRc buses should be connected to the appropriate read address connections. The optional INIT_A, INIT_B, INIT_C and INIT_D attributes consisting of a 64-bit hexadecimal values that specifies each port's initial memory contents can be specified. The INIT value correlates to the RAM addressing by the following equation: $ADDRy[z] = INIT_y[2*z+1:2*z]$. For instance, if the RAM ADDRc port is addressed to 00001, then the INIT_C[3:2] values would be the initial values shown on the DOC port before the first write occurs at that address. If left unspecified, the initial contents will default to all zeros.

Available Attributes

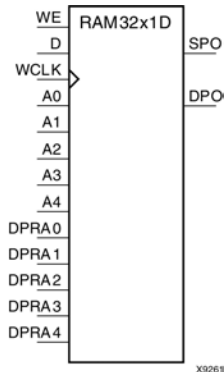
Attribute	Type	Allowed Values	Default	Description
INIT_A	Hexadecimal	Any 64-Bit Value	All zeros	Specifies the initial contents of the RAM on the A port.
INIT_B	Hexadecimal	Any 64-Bit Value	All zeros	Specifies the initial contents of the RAM on the B port.
INIT_C	Hexadecimal	Any 64-Bit Value	All zeros	Specifies the initial contents of the RAM on the C port.
INIT_D	Hexadecimal	Any 64-Bit Value	All zeros	Specifies the initial contents of the RAM on the D port.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

RAM32X1D

Primitive: 32-Deep by 1-Wide Static Dual Port Synchronous RAM



Introduction

The design element is a 32-word by 1-bit static dual port random access memory with synchronous write capability. The device has two separate address ports: the read address (DPRA4:DPRA0) and the write address (A4:A0). These two address ports are completely asynchronous. The read address controls the location of the data driven out of the output pin (DPO), and the write address controls the destination of a valid write transaction. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D) into the word selected by the 5-bit write address. For predictable performance, write address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block. You can initialize RAM32X1D during configuration using the INIT attribute. Mode selection is shown in the following logic table.

The SPO output reflects the data in the memory cell addressed by A4:A0. The DPO output reflects the data in the memory cell addressed by DPRA4:DPRA0. The write process is not affected by the address on the read address port.

Logic Table

Inputs			Outputs	
WE (Mode)	WCLK	D	SPO	DPO
0 (read)	X	X	data_a	data_d
1 (read)	0	X	data_a	data_d
1 (read)	1	X	data_a	data_d
1 (write)	↑	D	D	data_d
1 (read)	↓	X	data_a	data_d

Design Entry Method

This design element can be used in schematics.

Available Attributes

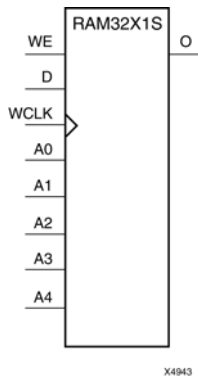
Attribute	Type	Allowed Values	Default	Descriptions
INIT	Hexadecimal	Any 32-Bit Value	All Zeros	Initializes ROMs, RAMs, registers, and look-up tables.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

RAM32X1S

Primitive: 32-Deep by 1-Wide Static Synchronous RAM



Introduction

The design element is a 32-word by 1-bit static random access memory with synchronous write capability. When the write enable is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When (WE) is High, any positive transition on (WCLK) loads the data on the data input (D) into the word selected by the 5-bit address (A4-A0). For predictable performance, address and data inputs must be stable before a Low-to-High (WCLK) transition. This RAM block assumes an active-High (WCLK). However, (WCLK) can be active-High or active-Low. Any inverter placed on the (WCLK) input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins. You can initialize RAM32X1S during configuration using the INIT attribute.

Logic Table

Inputs			Outputs
WE (Mode)	WCLK	D	O
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↓	D	D
1 (read)	↑	X	Data

Design Entry Method

This design element can be used in schematics.

Available Attributes

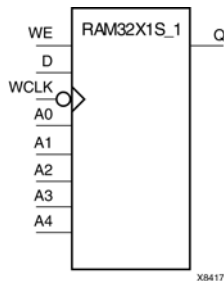
Attribute	Type	Allowed Values	Default	Descriptions
INIT	Hexadecimal	Any 32-Bit Value	All zeros	Specifies initial contents of the RAM.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

RAM32X1S_1

Primitive: 32-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock



Introduction

The design element is a 32-word by 1-bit static random access memory with synchronous write capability. When the write enable is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When (WE) is High, any negative transition on (WCLK) loads the data on the data input (D) into the word selected by the 5-bit address (A4:A0). For predictable performance, address and data inputs must be stable before a High-to-Low (WCLK) transition. This RAM block assumes an active-Low (WCLK). However, (WCLK) can be active-High or active-Low. Any inverter placed on the (WCLK) input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins. You can initialize RAM32X1S_1 during configuration using the INIT attribute.

Logic Table

Inputs			Outputs
WE (Mode)	WCLK	D	O
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↓	D	D
1 (read)	↑	X	Data
Data = word addressed by bits A4:A0			

Design Entry Method

This design element can be used in schematics.

Available Attributes

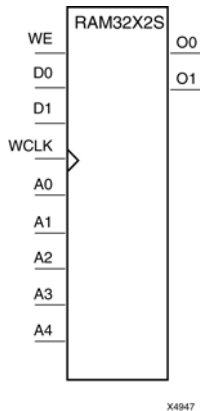
Attribute	Type	Allowed Values	Default	Descriptions
INIT	Hexadecimal	Any 32-Bit Value	0	Initializes RAMs, registers, and look-up tables.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

RAM32X2S

Primitive: 32-Deep by 2-Wide Static Synchronous RAM



Introduction

The design element is a 32-word by 2-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When (WE) is High, any positive transition on (WCLK) loads the data on the data input (D1-D0) into the word selected by the 5-bit address (A4-A0). For predictable performance, address and data inputs must be stable before a Low-to-High (WCLK) transition. This RAM block assumes an active-High (WCLK). However, (WCLK) can be active-High or active-Low. Any inverter placed on the (WCLK) input net is absorbed into the block. The signal output on the data output pins (O1-O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

You can use the INIT_00 and INIT_01 properties to specify the initial contents of RAM32X2S.

Logic Table

Inputs			Outputs
WE (Mode)	WCLK	D	O0-O1
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D1:D0	D1:D0
1 (read)	↓	X	Data
Data = word addressed by bits A4:A0			

Design Entry Method

This design element can be used in schematics.

Available Attributes

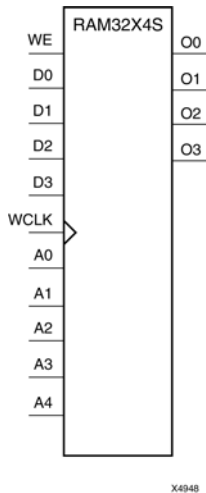
Attribute	Type	Allowed Values	Default	Descriptions
INIT_00	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 0 of RAM.
INIT_01	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 1 of RAM.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

RAM32X4S

Primitive: 32-Deep by 4-Wide Static Synchronous RAM



Introduction

This design element is a 32-word by 4-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data inputs (D3-D0) into the word selected by the 5-bit address (A4:A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pins (O3-O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

Logic Table

Inputs			Outputs
WE	WCLK	D3-D0	O3-O0
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D3:D0	D3:D0
1 (read)	↓	X	Data
Data = word addressed by bits A4:A0			

Design Entry Method

This design element can be used in schematics.

Available Attributes

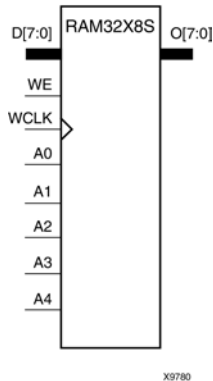
Attribute	Type	Allowed Values	Default	Description
INIT_00	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 0 of RAM.
INIT_01	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 1 of RAM.
INIT_02	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 2 of RAM.
INIT_03	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 3 of RAM.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

RAM32X8S

Primitive: 32-Deep by 8-Wide Static Synchronous RAM



Introduction

This design element is a 32-word by 8-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data inputs (D7:D0) into the word selected by the 5-bit address (A4:A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pins (O7:O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

Logic Table

Inputs			Outputs
WE (mode)	WCLK	D7:D0	O7:O0
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D7:D0	D7:D0
1 (read)	↓	X	Data
Data = word addressed by bits A4:A0			

Design Entry Method

This design element can be used in schematics.

Available Attributes

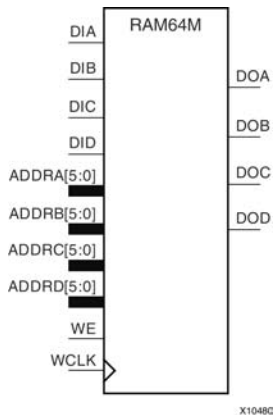
Attribute	Type	Allowed Values	Default	Description
INIT_00	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 0 of RAM.
INIT_01	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 1 of RAM.
INIT_02	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 2 of RAM.
INIT_03	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 3 of RAM.
INIT_04	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 4 of RAM.
INIT_05	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 5 of RAM.
INIT_06	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 6 of RAM.
INIT_07	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 7 of RAM.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

RAM64M

Primitive: 64-Deep by 4-bit Wide Multi Port Random Access Memory (Select RAM)



Introduction

This design element is a 64-bit deep by 4-bit wide, multi-port, random access memory with synchronous write and asynchronous independent bit wide read capability. This RAM is implemented using the LUT resources of the device (also known as SelectRAM™) and does not consume any of the block RAM resources of the device. The RAM64M component is implemented in a single slice, and consists of one 4-bit write, 1-bit read port, and three separate 1-bit read ports from the same memory allowing for 4-bit write and independent bit read access RAM. If the DIA, DIB, DIC and DID inputs are all tied to the same data inputs, the RAM can become a 1 read/write port, 3 independent read port 64x1 quad port memory. If DID is grounded, DOD is not used. While ADDRA, ADDRb and ADDRc are tied to the same address the RAM becomes a 64x3 simple dual port RAM. If ADDRd is tied to ADDRA, ADDRb, and ADDRc; then the RAM is a 64x4 single port RAM. There are several other possible configurations for this RAM.

Port Descriptions

Port	Direction	Width	Function
DOA	Output	1	Read port data outputs addressed by ADDRA
DOB	Output	1	Read port data outputs addressed by ADDR B
DOC	Output	1	Read port data outputs addressed by ADDR C
DOD	Output	1	Read/Write port data outputs addressed by ADDR D
DIA	Input	1	Write data inputs addressed by ADDR D (read output is addressed by ADDRA)
DIB	Input	1	Write data inputs addressed by ADDR D (read output is addressed by ADDR B)
DIC	Input	1	Write data inputs addressed by ADDR D (read output is addressed by ADDR C)
DID	Input	1	Write data inputs addressed by ADDR D
ADDRA	Input	6	Read address bus A
ADDR B	Input	6	Read address bus B
ADDR C	Input	6	Read address bus C
ADDR D	Input	6	4-bit data write port, 1-bit data read port address bus D
WE	Input	1	Write Enable
WCLK	Input	1	Write clock (reads are asynchronous)

Design Entry Method

This design element can be used in schematics.

This element can be inferred by some synthesis tools by describing a RAM with a synchronous write and asynchronous read capability. Consult your synthesis tool documentation for details on RAM inference capabilities and coding examples. Xilinx suggests that you instantiate RAM64Ms if you have a need to implicitly specify the RAM function, or if you need to manually place or relationally place the component. If a synchronous read capability is desired, the RAM64M outputs can be connected to an FDRSE (FDCPE is asynchronous set/reset is necessary) in order to improve the output timing of the function. However, this is not necessary for the proper operation of the RAM. If you want to have the data clocked on the negative edge of a clock, an inverter can be described on the clock input to this component. This inverter will be absorbed into the block giving the ability to write to the RAM on falling clock edges.

If instantiated, the following connections should be made to this component. Tie the WCLK input to the desired clock source, the DIA, DIB, DIC and DID inputs to the data source to be stored and the DOA, DOB, DOC and DOD outputs to an FDCE D input or other appropriate data destination or left unconnected if not used. The WE clock enable pin should be connected to the proper write enable source in the design. The 5-bit ADDR D bus should be connected to the source for the read/write addressing and the 5-bit ADDRA, ADDR B and ADDR C buses should be connected to the appropriate read address connections. The optional INIT_A, INIT_B, INIT_C and INIT_D attributes consisting of a 64-bit hexadecimal values that specifies each port's initial memory contents can be specified. The INIT value correlates to the RAM addressing by the following equation: $ADDRy[z] = INIT_y[z]$.

For instance, if the RAM ADDR C port is addressed to 00001, then the INIT_C[1] values would be the initial values shown on the DOC port before the first write occurs at that address. If left unspecified, the initial contents will default to all zeros.

Available Attributes

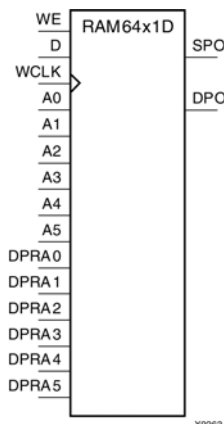
Attribute	Type	Allowed Values	Default	Description
INIT_A	Hexadecimal	Any 64-Bit Value	All zero	Specifies the initial contents of the RAM on the A port.
INIT_B	Hexadecimal	Any 64-Bit Value	All zero	Specifies the initial contents of the RAM on the B port.
INIT_C	Hexadecimal	Any 64-Bit Value	All zero	Specifies the initial contents of the RAM on the C port.
INIT_D	Hexadecimal	Any 64-Bit Value	All zero	Specifies the initial contents of the RAM on the D port.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

RAM64X1D

Primitive: 64-Deep by 1-Wide Dual Port Static Synchronous RAM



Introduction

This design element is a 64-word by 1-bit static dual port random access memory with synchronous write capability. The device has two separate address ports: the read address (DPRA5:DPRA0) and the write address (A5:A0). These two address ports are completely asynchronous. The read address controls the location of the data driven out of the output pin (DPO), and the write address controls the destination of a valid write transaction. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected.

When WE is High, any positive transition on WCLK loads the data on the data input (D) into the word selected by the 6-bit (A0:A5) write address. For predictable performance, write address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The SPO output reflects the data in the memory cell addressed by A5:A0. The DPO output reflects the data in the memory cell addressed by DPRA5:DPRA0.

Note The write process is not affected by the address on the read address port.

Logic Table

Inputs			Outputs	
WE (mode)	WCLK	D	SPO	DPO
0 (read)	X	X	data_a	data_d
1 (read)	0	X	data_a	data_d
1 (read)	1	X	data_a	data_d
1 (write)	↑	D	D	data_d
1 (read)	↓	X	data_a	data_d
data_a = word addressed by bits A5:A0				
data_d = word addressed by bits DPRA5:DPRA0				

Design Entry Method

This design element can be used in schematics.

Available Attributes

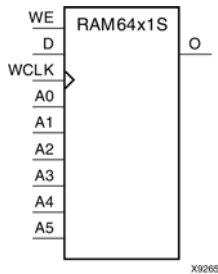
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 64-Bit Value	All zeros	Initializes RAMs, registers, and look-up tables.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

RAM64X1S

Primitive: 64-Deep by 1-Wide Static Synchronous RAM



Introduction

This design element is a 64-word by 1-bit static random access memory (RAM) with synchronous write capability. When the write enable is set Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is set High, any positive transition on WCLK loads the data on the data input (D) into the word selected by the 6-bit address (A5:A0). This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins.

You can initialize this element during configuration using the INIT attribute.

Logic Table

Mode selection is shown in the following logic table

Inputs			Outputs
WE (mode)	WCLK	D	O
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D	D
1 (read)	↓	X	Data
Data = word addressed by bits A5:A0			

Design Entry Method

This design element can be used in schematics.

Available Attributes

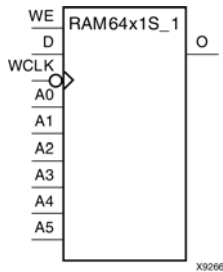
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 64-Bit Value	All zeros	Initializes ROMs, RAMs, registers, and look-up tables.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

RAM64X1S_1

Primitive: 64-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock



Introduction

This design element is a 64-word by 1-bit static random access memory with synchronous write capability. When the write enable is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When (WE) is High, any negative transition on (WCLK) loads the data on the data input (D) into the word selected by the 6-bit address (A5:A0). For predictable performance, address and data inputs must be stable before a High-to-Low (WCLK) transition. This RAM block assumes an active-Low (WCLK). However, (WCLK) can be active-High or active-Low. Any inverter placed on the (WCLK) input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins.

You can initialize this element during configuration using the INIT attribute.

Logic Table

Inputs			Outputs
WE (mode)	WCLK	D	O
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↓	D	D
1 (read)	↑	X	Data
Data = word addressed by bits A5:A0			

Design Entry Method

This design element can be used in schematics.

Available Attributes

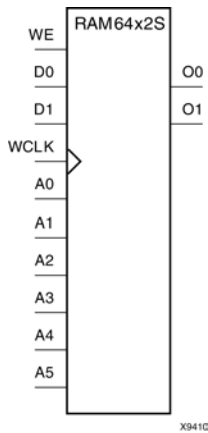
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 64-Bit Value	All zeros	Initializes ROMs, RAMs, registers, and look-up tables.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

RAM64X2S

Primitive: 64-Deep by 2-Wide Static Synchronous RAM



Introduction

This design element is a 64-word by 2-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D1:D0) into the word selected by the 6-bit address (A5:A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pins (O1:O0) is the data that is stored in the RAM at the location defined by the values on the address pins. You can use the INIT_00 and INIT_01 properties to specify the initial contents of this design element.

Logic Table

Inputs			Outputs
WE (mode)	WCLK	D0:D1	O0:O1
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D1:D0	D1:D0
1 (read)	↓	X	Data
Data = word addressed by bits A5:A0			

Design Entry Method

This design element can be used in schematics.

Available Attributes

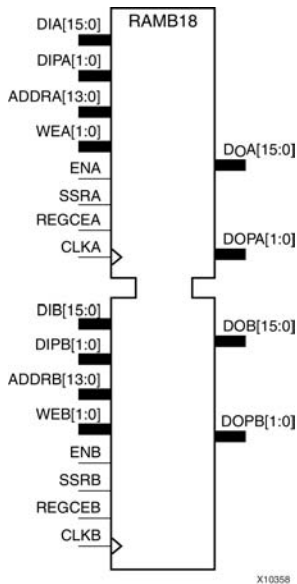
Attribute	Type	Allowed Values	Default	Description
INIT_00	Hexadecimal	Any 64-Bit Value	All zeros	Initializes RAMs, registers, and look-up tables.
INIT_01	Hexadecimal	Any 64-Bit Value	All zeros	Initializes RAMs, registers, and look-up tables.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

RAMB18

Primitive: 18K-bit Configurable Synchronous True Dual Port Block RAM



Introduction

Virtex®-5 and above devices contain several block RAM memories which can be configured as FIFOs, automatic error correction RAM, or general-purpose 36kb or 18kb RAM/ROM memories. These block RAM memories offer fast and flexible storage of large amounts of on-chip data. The RAMB18 allows access to the block RAM in the 18kb configuration. This element can be cascaded to create a larger ram. This element can be configured and used as a 1-bit wide by 16K deep to an 18-bit wide by 1029-bit deep true dual port RAM. Both read and write operations are fully synchronous to the supplied clock(s) to the component. However, the READ and WRITE ports can operate fully independent and asynchronous to each other accessing the same memory array. When configured in the wider data width modes, byte-enable write operations are possible, and an optional output register can be used to reduce the clock-to-out times of the RAM.

Port Descriptions

Port	Direction	Width	Function
DOA, DOB	Output	1, 2, 4, 8, 16	Port A/B data output bus.
DOPA, DOPB	Output	0, 1, 2	Port A/B parity data output bus.
DIA, DIB	Input	1, 2, 4, 8, 16	Port A/B data input bus.
DIPA, DIPB	Input	0, 1, 2	Port A/B parity data input bus.
ADDRA, ADDR[13:0]	Input	14	Port A/B address input bus.
WEA	Input	2	Port A byte-wide write enable.
WEB	Input	2	Port B byte-wide write enable.
ENA, ENB	Input	1	Port A/B enable
SSRA, SSRB	Input	1	Port A/B output registers synchronous set/reset. Active high will synchronous preset/reset to the associated port to the value specified for SRVAL_A/SRVAL_B.

Port	Direction	Width	Function
REGCEA, REGCEB	Input	1	Port A/B output register clock enable input
CLKA, CLKB	Input	1	Port A/B clock input.

Design Entry Method

This design element can be used in schematics.

The following table shows the necessary data, address and write enable connections for the variable width ports for each DATA_WIDTH value for either Port A or Port B. If a different width is used for the read and write on the same port, use the deeper of the two in order to select address connections.

All data and address ports not necessary for a particular configuration should either be left unconnected or grounded with the following exceptions.

DATA_WIDTH Value	DI, DIP Connections	ADDR Connections	WE Connections	DO, DOP Connections
1	DI[0]	ADDR[14:0]	Connect WE[1:0] to single user WE signal	DO[0]
2	DI[1:0]	ADDR[14:1]	Connect WE[1:0] to single user WE signal	DO[1:0]
4	DI[3:0]	ADDR[14:2]	Connect WE[1:0] to single user WE signal	DO[3:0]
9	DI[7:0], DIP[0]	ADDR[14:3]	Connect WE[1:0] to single user WE signal	DO[7:0], DOP[0]
18	DI[15:0], DIP[1:0]	ADDR[14:4]	Connect WE[0] and WE[1] to user WE signal.	DO[15:0], DOP[1:0]

Available Attributes

Attribute	Type	Allowed Values	Default	Description
DOA_REG, DOB_REG	Integer	0, 1	0	A value of 1 enables the output registers the RAM enabling quicker clock-to-out from the RAM at the expense of an added clock cycle of read latency. A value of 0 allows a read in one clock cycle but will result in slower clock-to-out timing.
INIT_A	Hexadecimal	Any 18-Bit Value	All zeros	Specifies the initial value on the Port A output after configuration.
INIT_B	Hexadecimal	Any 18-Bit Value	All zeros	Specifies the initial value on the Port B output after configuration.
READ_WIDTH_A	Integer	0, 1, 2, 4, 9, or 18	0	Specifies the desired data width for a read on Port A including parity bits. The 0 signifies that the port is not used.
READ_WIDTH_B	Integer	0, 1, 2, 4, 9, or 18	0	Specifies the desired data width for a read on Port B including parity bits. The 0 signifies that the port is not used.

Attribute	Type	Allowed Values	Default	Description
SIM_COLLISION_CHECK	String	"ALL", "WARNING_ONLY", "GENERATE_X_ONLY" or "NONE"	"ALL"	<p>Allows modification of the simulation behavior if a memory collision occurs. The output is affected as follows:</p> <ul style="list-style-type: none"> "ALL" - Warning produced and affected outputs/memory location go unknown (X). "WARNING_ONLY" - Warning produced and affected outputs/memory retain last value. "GENERATE_X_ONLY" - No warning. However, affected outputs/memory go unknown (X). "NONE" - No warning and affected outputs/memory retain last value. <p>Note Setting this to a value other than "ALL" can allow problems in the design go unnoticed during simulation. Care should be taken when changing the value of this attribute. Please see the <i>Synthesis and Simulation Design Guide</i> for more information.</p>
SIM_MODE	String	"SAFE" or "FAST" .	"SAFE"	This is a simulation only attribute. It will direct the simulation model to run in performance-oriented mode when set to "FAST." Please see the <i>Synthesis and Simulation Design Guide</i> for more information.
SRVAL_A	Hexadecimal	Any 18-Bit Value	All zeros	Specifies the output value of Port A upon the assertion of the synchronous reset (SSRA) signal.
SRVAL_B	Hexadecimal	Any 18-Bit Value	All zeros	Specifies the output value of Port B upon the assertion of the synchronous reset (SSRB) signal.
WRITE_MODE_A, WRITE_MODE_B	String	"WRITE_FIRST", "READ_FIRST", or "NO_CHANGE"	WRITE_FIRST	<p>Specifies output behavior of the port being written to:</p> <ul style="list-style-type: none"> "WRITE_FIRST" – written value appears on output port of the RAM READ_FIRST - previous RAM contents for that memory location appear on the output port NO_CHANGE – previous value on the output port remains the same.
WRITE_WIDTH_A	Integer	0,1, 2, 4, 9, or 18	0	Specifies the desired data width for a write to Port A including parity bits. The 0 signifies that the port is not used.
WRITE_WIDTH_B	Integer	0,1, 2, 4, 9, or 18	0	Specifies the desired data width for a write to Port B including parity bits. The 0 signifies that the port is not used.
INIT_00 to INIT_3F	Hexadecimal	Any 256-Bit Value	All zeros	Allows specification of the initial contents of the 16kb data memory array.
INITP_00 to INITP_07	Hexadecimal	Any 256-Bit Value	All zeroes	Allows specification of the initial contents of the 2kb parity data memory array.

Mapping of INIT_A, INIT_B, SRVAL_A, SRVAL_B

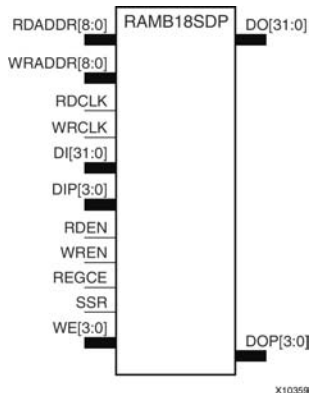
The INIT_A, INIT_B, SRVAL_A and SRVAL_B attributes are all 18-bit attributes. However, if the READ_WIDTH is set to a value less than 18 for the particular port only a subset of the bits are used.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

RAMB18SDP

Primitive: 36-bit by 512 Deep, 18kb Synchronous Simple Dual Port Block RAM



Introduction

This design element is one of several block RAM memories that can be configured as FIFOs, automatic error correction RAM, or general-purpose, 36kb or 18kb RAM/ROM memories. These Block RAM memories offer fast and flexible storage of large amounts of on-chip data. The RAMB18SDP gives you access to the block RAM in the 18kb configuration. This component is set to a 36-bit wide by 512 deep simple dual port RAM. Both read and write operations are fully synchronous to the supplied clock(s) to the component. However, the READ and WRITE ports can operate fully independently and asynchronously to each other, accessing the same memory array. Byte-enable write operations are possible, and an optional output register can be used to reduce the clock-to-out times of the RAM.

Note This element, must be configured so that read and write ports have the same width.

Port Descriptions

Port	Direction	Width	Function
DO	Output	32	Data output bus addressed by RDADDR.
DOP	Output	4	Data parity output bus addressed by RDADDR.
DI	Input	32	Data input bus addressed by WRADDR.
DIP	Input	4	Data parity input bus addressed by WRADDR.
WRDDRA, RDDDRB	Input	9	Write/Read address input buses.
WE	Input	4	Write enable.
WREN, RDEN	Input	1	Write/Read enable
SSR	Input	1	Output registers synchronous reset.
REGCE	Input	1	Output register clock enable input (valid only when DO_REG=1).
WRCLK, RDCLK	Input	1	Write/Read clock input.

Design Entry Method

This design element can be used in schematics.

Available Attributes

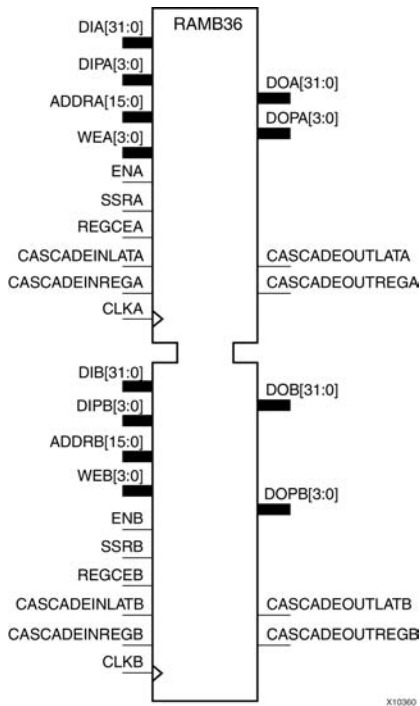
Attribute(s)	Type	Allowed Values	Default	Description
DO_REG	Integer	0, 1	0	A value of 1 enables the output registers to the RAM, enabling quicker clock-to-out from the RAM at the expense of an added clock cycle of read latency. A value of 0 allows a read in one clock cycle, but will have slower clock-to-out timing.
INIT	Hexadecimal	Any 36-Bit Value	All zeros	Specifies the initial value on the output after configuration.
SIM_COLLISION_CHECK	String	"ALL", "WARNING_ONLY", "GENERATE_X_ONLY" or "NONE"	"ALL"	<p>Allows modification of the simulation behavior if a memory collision occurs. The output is affected as follows:</p> <ul style="list-style-type: none"> "ALL" - Warning produced and affected outputs/memory location go unknown (X). "WARNING_ONLY" - Warning produced and affected outputs/memory retain last value. "GENERATE_X_ONLY" - No warning. However, affected outputs/memory go unknown (X). "NONE" - No warning and affected outputs/memory retain last value. <p>Note Setting this to a value other than "ALL" can allow problems in the design go unnoticed during simulation. Care should be taken when changing the value of this attribute. Please see the <i>Synthesis and Simulation Design Guide</i> for more information.</p>
SIM_MODE	String	"SAFE" or "FAST"	"SAFE"	This is a simulation only attribute. It will direct the simulation model to run in performance-oriented mode when set to "FAST." Please see the <i>Synthesis and Simulation Design Guide</i> for more information.
SRVAL	Hexadecimal	Any 36-Bit Value	All zeros	Specifies the output value of on the DO port upon the assertion of the synchronous reset (SSR) signal.
INIT_00 to INIT_3F	Hexadecimal	Any 256-Bit Value	All zeros	Allows specification of the initial contents of the 16kb data memory array.
INITP_00 to INITP_07	Hexadecimal	Any 256-Bit Value	All zeros	Allows specification of the initial contents of the 2kb parity data memory array.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

RAMB36

Primitive: 36kb Configurable Synchronous True Dual Port Block RAM



Introduction

This design element is one of several block RAM memories that can be configured as FIFOs, automatic error correction RAM, or general-purpose, 36kb or 18kb RAM/ROM memories. These block RAM memories offer fast and flexible storage of large amounts of on-chip data. This element allows access to the block RAM in the 36kb configuration. This component can be configured and used as a 1-bit wide by 32K deep to a 36-bit wide by 1K deep true dual port RAM. Both read and write operations are fully synchronous to the supplied clock(s) to the component. However, Port A and Port B can operate fully independently and asynchronously to each other accessing the same memory array. When configured in the wider data width modes, byte-enable write operations are possible and an option output register can be used to reduce the clock-to-out times of the RAM at the expense of an extra clock cycle of latency.

This design element should be used for Simple Dual Port 72-bit wide, 512 deep, optional ECC scrub functionality. This element can be created using cascaded RAMB18s.

The following possible combination of elements can be placed in RAMB36:

- RAMB18/RAMB18
- RAMB18/FIFO18
- RAMB18SDP/RAMB18SDP
- RAMB18SDP/FIFO18_36

Port Descriptions

Port	Direction	Width	Function
DOA	Output	1, 2, 4, 8, 16, 32	Port A data output bus.
DOB	Output	1, 2, 4, 8, 16, 32	Port B data output bus.
DOPA, DOPB	Output	0, 1, 2, 4	Port A/B parity data output bus.
CASCADEOUTLATA, CASCADEOUTLATB	Output	1	Outputs for ports A and B used to cascade two BlockRAMs to create a 64K deep by 1 wide memory (connects to the lower CASCADEINLATA/B of another RAMB36, leave unconnected if not building a 64Kx1 RAM or if RAM_EXTENSION_A/B are not set to "LOWER").
CASCADEOUTREGA, CASCADEOUTREGB	Output	1	Outputs for ports A and B used to cascade two BlockRAMs to create a 64K deep by 1 wide memory (connects to the lower CASCADEINREGA/B of another RAMB36, leave unconnected if not building a 64Kx1 RAM or if RAM_EXTENSION_A/B are not set to "LOWER").
CASCADEINLATA, CASCADEINLATB	Input	1	Inputs for ports A and B used to cascade two BlockRAMs to create a 64K deep by 1 wide memory (connects to the upper CASCADEOUTLATA/B of another RAMB36, leave unconnected if not building a 64Kx1 RAM or if RAM_EXTENSION_A/B are not set to "UPPER").
CASCADEINREGA, CASCADEINREGB	Input	1	Inputs for ports A and B used to cascade two BlockRAMs to create a 64K deep by 1 wide memory (connects to the upper CASCADEOUTREGA/B of another RAMB36, leave unconnected if not building a 64Kx1 RAM or if RAM_EXTENSION_A/B are not set to "UPPER").
DIA	Input	1, 2, 4, 8, 16, 32	Port A data input bus.
DIB	Input	1, 2, 4, 8, 16, 32	Port B data input bus.
DIPA, DIPB	Input	0, 1, 2, 4	Port A/B parity data input bus.
ADDRA, ADDRb	Input	16	Port A/B address input bus; 16 for CASC mode.
WEA	Input	4	Port A byte-wide write enable
WEB	Input	4	Port B byte-wide write enable.
ENA, ENB	Input	1	Port A/B enable. Active high is enabled, while a low value will disable reads or writes to the associated port.
SSRA, SSRB	Input	1	Port A/B output registers synchronous set/reset. Active high will synchronous preset/reset to the associated port to the value specified for SRVAL_A/SRVAL_B.
REGCEA, REGCEB	Input	1	Port A/B output register clock enable input. Active high will clock enable the output registers to the associated port.

Design Entry Method

This design element can be used in schematics.

The following table shows the necessary data, address and write enable connections for the variable width ports for each DATA_WIDTH value for either Port A or Port B. If a different width is used for the read and write on the same port, use the deeper of the two in order to select address connections.

All data and address ports not necessary for a particular configuration should either be left unconnected or grounded with the following exceptions.

- The address bit 15 is only used in cascadable block RAM. For noncascading block RAM, connect High.
- ADDR pins must be 16-bits wide. However, valid addresses for non-cascadable block RAM are only found on pin 14 to (15 - address width). The remaining pins, including pin 15, should be tied High.

DATA_WIDTH Value	DI, DIP Connections	ADDR Connections	WE Connections	DO, DOP Connections
1 (with cascade)	DI[0]	ADDR[15:0]	Connect WE[3:0] to single user WE signal	DO[0]
1 (without cascade)	DI[0]	ADDR[14:0]	Connect WE[3:0] to single user WE signal	DO[0]
2	DI[1:0]	ADDR[14:1]	Connect WE[3:0] to single user WE signal	DO[1:0]
4	DI[3:0]	ADDR[14:2]	Connect WE[3:0] to single user WE signal	DO[3:0]
9	DI[7:0], DIP[0]	ADDR[14:3]	Connect WE[3:0] to single user WE signal	DO[7:0], DOP[0]
18	DI[15:0], DIP[1:0]	ADDR[14:4]	Connect WE[0] and WE[2] to user WE[0] and WE[1] and WE[3] to user WE[1]	DO[15:0], DOP[1:0]
36	DI[31:0], DIP[3:0]	ADDR[14:5]	Connect each WE[3:0] signal to the associated byte write enable/	DO[31:0], DOP[3:0]

Available Attributes

Attribute	Type	Allowed Values	Default	Description
DOA_REG, DOB_REG	Integer	0, 1	0	A value of 1 enables to the output registers to the RAM enabling quicker clock-to-out from the RAM at the expense of an added clock cycle of read latency. A value of 0 allows a read in one clock cycle, but will result in slower clock to out timing.
INIT_A	Hexadecimal	Any 36-Bit Value	All zeros	Specifies the initial value on the output of Port A of the RAMB36 after configuration.
INIT_B	Hexadecimal	Any 36-Bit Value	All zeros	Specifies the initial value on the output of Port B of the RAMB36 after configuration.
READ_WIDTH_A	Integer	0, 1, 4, 9, 18 or 36	0	Specifies the desired data width for a read on Port A, including parity bits. This value must be 0 if the Port B is not used. Otherwise, it should be set to the desired port width.

Attribute	Type	Allowed Values	Default	Description
READ_WIDTH_B	Integer	0, 1, 4, 9, 18 or 36	0	Specifies the desired data width for a read on Port B including parity bits. This value must be 0 if the Port B is not used. Otherwise, it should be set to the desired port width.
SIM_COLLISION_CHECK	String	"ALL", "WARNING_ONLY", "GENERATE_X_ONLY" or "NONE"	"ALL"	<p>Allows modification of the simulation behavior if a memory collision occurs. The output is affected as follows:</p> <ul style="list-style-type: none"> "ALL" - Warning produced and affected outputs/memory location go unknown (X). "WARNING_ONLY" - Warning produced and affected outputs/memory retain last value. "GENERATE_X_ONLY" - No warning. However, affected outputs/memory go unknown (X). "NONE" - No warning and affected outputs/memory retain last value. <p>Note Setting this to a value other than "ALL" can allow problems in the design go unnoticed during simulation. Care should be taken when changing the value of this attribute. Please see the <i>Synthesis and Simulation Design Guide</i> for more information.</p>
SIM_MODE	String	"SAFE" or "FAST"	"SAFE"	This is a simulation only attribute. It will direct the simulation model to run in performance-oriented mode when set to "FAST." Please see the <i>Synthesis and Simulation Design Guide</i> for more information.
SRVAL_A	Hexadecimal	Any 36-Bit Value	All zeros	Specifies the output value of the RAM upon the assertion of the Port A synchronous reset (SSRA) signal.
SRVAL_B	Hexadecimal	Any 36-Bit Value	All zeros	Specifies the output value of the RAM upon the assertion of the Port B synchronous reset (SSRB) signal.
WRITE_MODE_A, WRITE_MODE_B	String	"WRITE_FIRST", "READ_FIRST" or "NO_CHANGE"	"WRITE_FIRST"	<p>Specifies output behavior of the port being written to:</p> <ul style="list-style-type: none"> "WRITE_FIRST" = written value appears on output port of the RAM "READ_FIRST" = previous RAM contents for that memory location appear on the output port "NO_CHANGE" = previous value on the output port remains the same.

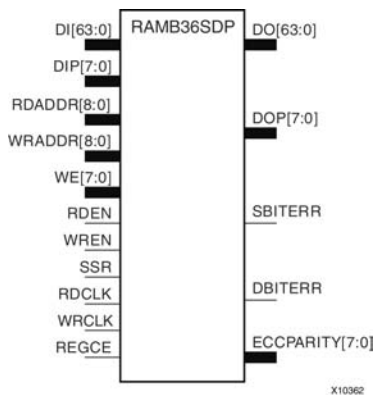
Attribute	Type	Allowed Values	Default	Description
WRITE_WIDTH_A	Integer	0, 1, 2, 4, 9, 18 or 36	0	Specifies the desired data width for a write to Port B including parity bits. This value must be 0 if the port is not used. Otherwise should be set to the desired write width.
WRITE_WIDTH_B	Integer	0, 1, 2, 4, 9, 18 or 36	0	Specifies the desired data width for a write to Port B including parity bits. This value must be 0 if the port is not used. Otherwise should be set to the desired write width.
RAM_EXTENTION_A, RAM_EXTENTION_B	String	"UPPER", "LOWER" or "NONE"	"NONE"	If not cascading two BlockRAMs to form a 72K x 1 RAM set to NONE". If cascading RAMs, set to either "UPPER" or "LOWER" to indicate relative RAM location for proper configuration of the RAM.
INIT_00 to INIT_7F	Hexadecimal	Any 256-Bit Value	All zeros	Allows specification of the initial contents of the 72kb data memory array.
INITP_00 to INITP_0F	Hexadecimal	Any 256-Bit Value	All zeros	Allows specification of the initial contents of the 4kb parity data memory array.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

RAMB36SDP

Primitive: 72-bit by 512 Deep, 36kb Synchronous Simple Dual Port Block RAM with ECC (Error Correction Circuitry)



Introduction

This design element is one of several Block RAM memories that can be configured as FIFOs, automatic error correction RAM, or general-purpose, 36kb or 18kb RAM/ROM memories. These Block RAM memories offer fast and flexible storage of large amounts of on-chip data. The RAMB36SDP gives you access to the block RAM in the 36kb configuration. This component is set to a 72-bit wide by 512 deep simple dual port RAM. Both read and write operations are fully synchronous to the supplied clock(s) to the component. However, READ and WRITE ports can operate fully independently and asynchronously to each other accessing the same memory array. Byte-enable write operations are possible, and an optional output register can be used to reduce the clock-to-out times of the RAM. Error detection and correction circuitry can also be enabled to uncover and rectify possible memory corruptions.

Note This element, must be configured so that read and write ports have the same width.

Port Descriptions

Port	Direction	Width	Function
DO	Output	64	Data output bus addressed by RDADDR.
DOP	Output	8	Data parity output bus addressed by RDADDR.
SBITERR	Output	1	Status output from ECC function to indicate a single bit error was detected. EN_ECC_READ needs to be TRUE in order to use this functionality.
DBITERR	Output	1	Status output from ECC function to indicate a double bit error was detected. EN_ECC_READ needs to be TRUE in order to use this functionality.
ECCPARITY	Output	8	8-bit data generated by the ECC encoder used by the ECC decoder for memory error detection and correction.
DI	Input	64	Data input bus addressed by WRADDR.
DIP	Input	8	Data parity input bus addressed by WRADDR.
WRADDR, RDADDR	Input	9	Write/Read address input buses.
WE	Input	8	Write enable
WREN, RDEN	Input	1	Write/Read enable

Port	Direction	Width	Function
SSR	Input	1	Output registers synchronous reset.
REGCE	Input	1	Output register clock enable input (valid only when DO_REG=1)
WRCLK, RDCLK	Input	1	Write/Read clock input.

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
DO_REG	Integer	0, 1	0	A value of 1 enables to the output registers to the RAM enabling quicker clock-to-out from the RAM at the expense of an added clock cycle of read latency. A value of 0 allows a read in one clock cycle but will have slower clock to out timing.
INIT	Hexadecimal	Any 72-Bit Value	All zeros	Specifies the initial value on the output after configuration.
EN_ECC_READ	Boolean	TRUE or FALSE	FALSE	Enable the ECC decoder circuitry.
EN_ECC_WRITE	Boolean	TRUE or FALSE	FALSE	Enable the ECC encoder circuitry.
EN_ECC_SCRUB	Boolean	TRUE or FALSE	FALSE	Enable ECC scrubbing of RAM contents
SIM_COLLISION_CHECK	String	"ALL", "WARNING_ONLY", "GENERATE_X_ONLY" or "NONE"	"ALL"	<p>Allows modification of the simulation behavior if a memory collision occurs. The output is affected as follows:</p> <ul style="list-style-type: none"> "ALL" - Warning produced and affected outputs/memory location go unknown (X). "WARNING_ONLY" - Warning produced and affected outputs/memory retain last value. "GENERATE_X_ONLY" - No warning. However, affected outputs/memory go unknown (X). "NONE" - No warning and affected outputs/memory retain last value. <p>Note Setting this to a value other than "ALL" can allow problems in the design go unnoticed during simulation. Care should be taken when changing the value of this attribute. Please see the <i>Synthesis and Simulation Design Guide</i> for more information.</p>
SIM_MODE	String	"SAFE" or "FAST"	"SAFE"	This is a simulation only attribute. It will direct the simulation model to run in performance-oriented mode when set to "FAST." Please see the <i>Synthesis and Simulation Design Guide</i> for more information.
SRVAL	Hexadecimal	Any 72-Bit Value	All zeroes	Specifies the output value of on the DO port upon the assertion of the synchronous reset (SSR) signal.

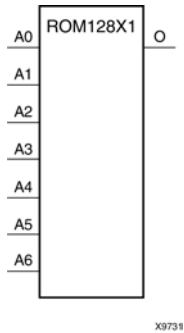
Attribute	Type	Allowed Values	Default	Description
INIT_00 to INIT_3F	Hexadecimal	Any 256-Bit Value	All zeroes	Allows specification of the initial contents of the 16kb data memory array.
INITP_00 to INITP_07	Hexadecimal	Any 256-Bit Value	All zeroes	Allows specification of the initial contents of the 2kb parity data memory array.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

ROM128X1

Primitive: 128-Deep by 1-Wide ROM



Introduction

This design element is a 128-word by 1-bit read-only memory. The data output (O) reflects the word selected by the 7-bit address (A6:A0). The ROM is initialized to a known value during configuration with the INIT=value parameter. The value consists of 32 hexadecimal digits that are written into the ROM from the most-significant digit A=FH to the least-significant digit A=0H. An error occurs if the INIT=value is not specified.

Logic Table

Input				Output
I0	I1	I2	I3	O
0	0	0	0	INIT(0)
0	0	0	1	INIT(1)
0	0	1	0	INIT(2)
0	0	1	1	INIT(3)
0	1	0	0	INIT(4)
0	1	0	1	INIT(5)
0	1	1	0	INIT(6)
0	1	1	1	INIT(7)
1	0	0	0	INIT(8)
1	0	0	1	INIT(9)
1	0	1	0	INIT(10)
1	0	1	1	INIT(11)
1	1	0	0	INIT(12)
1	1	0	1	INIT(13)
1	1	1	0	INIT(14)
1	1	1	1	INIT(15)

Design Entry Method

This design element can be used in schematics.

Available Attributes

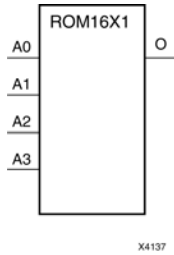
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 128-Bit Value	All zeros	Specifies the contents of the ROM.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

ROM16X1

Primitive: 16-Deep by 1-Wide ROM



Introduction

This design element is a 16-word by 1-bit read-only memory. The data output (O) reflects the word selected by the 4-bit address (A3:A0). The ROM is initialized to a known value during configuration with the INIT=value parameter. The value consists of four hexadecimal digits that are written into the ROM from the most-significant digit A=FH to the least-significant digit A=0H. For example, the INIT=10A7 parameter produces the data stream: 0001 0000 1010 0111. An error occurs if the INIT=value is not specified.

Logic Table

Input				Output
I0	I1	I2	I3	O
0	0	0	0	INIT(0)
0	0	0	1	INIT(1)
0	0	1	0	INIT(2)
0	0	1	1	INIT(3)
0	1	0	0	INIT(4)
0	1	0	1	INIT(5)
0	1	1	0	INIT(6)
0	1	1	1	INIT(7)
1	0	0	0	INIT(8)
1	0	0	1	INIT(9)
1	0	1	0	INIT(10)
1	0	1	1	INIT(11)
1	1	0	0	INIT(12)
1	1	0	1	INIT(13)
1	1	1	0	INIT(14)
1	1	1	1	INIT(15)

Design Entry Method

This design element can be used in schematics.

Available Attributes

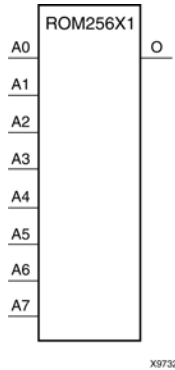
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Specifies the contents of the ROM.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

ROM256X1

Primitive: 256-Deep by 1-Wide ROM



Introduction

This design element is a 256-word by 1-bit read-only memory. The data output (O) reflects the word selected by the 8-bit address (A7:A0). The ROM is initialized to a known value during configuration with the INIT=value parameter. The value consists of 64 hexadecimal digits that are written into the ROM from the most-significant digit A=FH to the least-significant digit A=0H.

An error occurs if the INIT=value is not specified.

Logic Table

Input				Output
I0	I1	I2	I3	O
0	0	0	0	INIT(0)
0	0	0	1	INIT(1)
0	0	1	0	INIT(2)
0	0	1	1	INIT(3)
0	1	0	0	INIT(4)
0	1	0	1	INIT(5)
0	1	1	0	INIT(6)
0	1	1	1	INIT(7)
1	0	0	0	INIT(8)
1	0	0	1	INIT(9)
1	0	1	0	INIT(10)
1	0	1	1	INIT(11)
1	1	0	0	INIT(12)
1	1	0	1	INIT(13)
1	1	1	0	INIT(14)
1	1	1	1	INIT(15)

Design Entry Method

This design element can be used in schematics.

Available Attributes

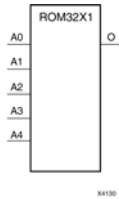
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 256-Bit Value	All zeros	Specifies the contents of the ROM.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

ROM32X1

Primitive: 32-Deep by 1-Wide ROM



Introduction

This design element is a 32-word by 1-bit read-only memory. The data output (O) reflects the word selected by the 5-bit address (A4:A0). The ROM is initialized to a known value during configuration with the INIT=value parameter. The value consists of eight hexadecimal digits that are written into the ROM from the most-significant digit A=1FH to the least-significant digit A=00H.

For example, the INIT=10A78F39 parameter produces the data stream: 0001 0000 1010 0111 1000 1111 0011 1001. An error occurs if the INIT=value is not specified.

Logic Table

Input				Output
I0	I1	I2	I3	O
0	0	0	0	INIT(0)
0	0	0	1	INIT(1)
0	0	1	0	INIT(2)
0	0	1	1	INIT(3)
0	1	0	0	INIT(4)
0	1	0	1	INIT(5)
0	1	1	0	INIT(6)
0	1	1	1	INIT(7)
1	0	0	0	INIT(8)
1	0	0	1	INIT(9)
1	0	1	0	INIT(10)
1	0	1	1	INIT(11)
1	1	0	0	INIT(12)
1	1	0	1	INIT(13)
1	1	1	0	INIT(14)
1	1	1	1	INIT(15)

Design Entry Method

This design element can be used in schematics.

Available Attributes

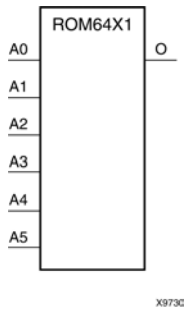
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 32-Bit Value	All zeros	Specifies the contents of the ROM.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

ROM64X1

Primitive: 64-Deep by 1-Wide ROM



Introduction

This design element is a 64-word by 1-bit read-only memory. The data output (O) reflects the word selected by the 6-bit address (A5:A0). The ROM is initialized to a known value during configuration with the INIT=value parameter. The value consists of 16 hexadecimal digits that are written into the ROM from the most-significant digit A=FH to the least-significant digit A=0H. An error occurs if the INIT=value is not specified.

Logic Table

Input				Output
I0	I1	I2	I3	O
0	0	0	0	INIT(0)
0	0	0	1	INIT(1)
0	0	1	0	INIT(2)
0	0	1	1	INIT(3)
0	1	0	0	INIT(4)
0	1	0	1	INIT(5)
0	1	1	0	INIT(6)
0	1	1	1	INIT(7)
1	0	0	0	INIT(8)
1	0	0	1	INIT(9)
1	0	1	0	INIT(10)
1	0	1	1	INIT(11)
1	1	0	0	INIT(12)
1	1	0	1	INIT(13)
1	1	1	0	INIT(14)
1	1	1	1	INIT(15)

Design Entry Method

This design element can be used in schematics.

Available Attributes

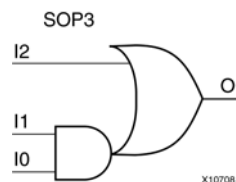
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 64-Bit Value	All zeros	Specifies the contents of the ROM.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SOP3

Macro: 3-Input Sum of Products



Introduction

Three input Sum of Products (SOP) macros provide common logic functions by OR gating the output of one AND function with one direct input. Variations of inverting and non-inverting inputs are available.

Design Entry Method

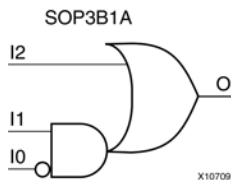
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SOP3B1A

Macro: 3-Input Sum of Products with One Inverted Input (Option A)



Introduction

Three input Sum of Products (SOP) macros provide common logic functions by OR gating the output of one AND function with one direct input. Variations of inverting and non-inverting inputs are available.

Design Entry Method

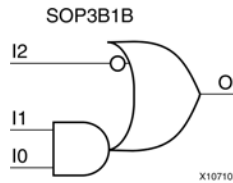
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SOP3B1B

Macro: 3-Input Sum of Products with One Inverted Input (Option B)



Introduction

Three input Sum of Products (SOP) macros provide common logic functions by OR gating the output of one AND function with one direct input. Variations of inverting and non-inverting inputs are available.

Design Entry Method

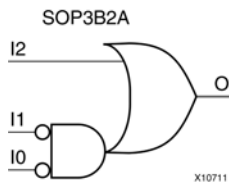
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SOP3B2A

Macro: 3-Input Sum of Products with Two Inverted Inputs (Option A)



Introduction

Three input Sum of Products (SOP) macros provide common logic functions by OR gating the output of one AND function with one direct input. Variations of inverting and non-inverting inputs are available.

Design Entry Method

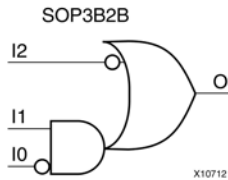
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SOP3B2B

Macro: 3-Input Sum of Products with Two Inverted Inputs (Option B)



Introduction

Three input Sum of Products (SOP) macros provide common logic functions by OR gating the output of one AND function with one direct input. Variations of inverting and non-inverting inputs are available.

Design Entry Method

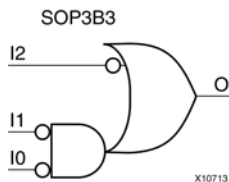
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SOP3B3

Macro: 3-Input Sum of Products with Inverted Inputs



Introduction

Three input Sum of Products (SOP) macros provide common logic functions by OR gating the output of one AND function with one direct input. Variations of inverting and non-inverting inputs are available.

Design Entry Method

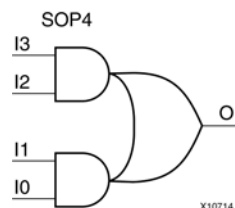
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SOP4

Macro: 4-Input Sum of Products



Introduction

Four input Sum of Products (SOP) macros provide common logic functions by OR gating the outputs of two AND functions. Variations of inverting and non-inverting inputs are available.

Design Entry Method

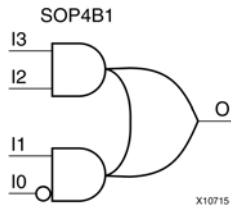
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SOP4B1

Macro: 4-Input Sum of Products with One Inverted Input



Introduction

Four input Sum of Products (SOP) macros provide common logic functions by OR gating the outputs of two AND functions. Variations of inverting and non-inverting inputs are available.

Design Entry Method

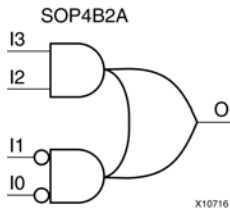
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SOP4B2A

Macro: 4-Input Sum of Products with Two Inverted Inputs (Option A)



Introduction

Four input Sum of Products (SOP) macros provide common logic functions by OR gating the outputs of two AND functions. Variations of inverting and non-inverting inputs are available.

Design Entry Method

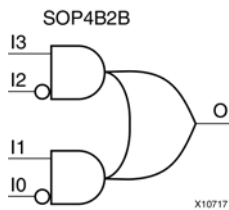
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SOP4B2B

Macro: 4-Input Sum of Products with Two Inverted Inputs (Option B)



Introduction

Four input Sum of Products (SOP) macros provide common logic functions by OR gating the outputs of two AND functions. Variations of inverting and non-inverting inputs are available.

Design Entry Method

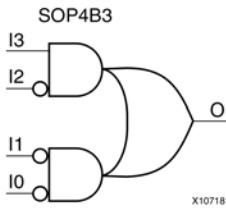
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SOP4B3

Macro: 4-Input Sum of Products with Three Inverted Inputs



Introduction

Four input Sum of Products (SOP) macros provide common logic functions by OR gating the outputs of two AND functions. Variations of inverting and non-inverting inputs are available.

Design Entry Method

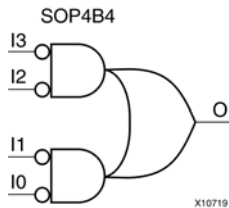
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SOP4B4

Macro: 4-Input Sum of Products with Inverted Inputs



Introduction

Four input Sum of Products (SOP) macros provide common logic functions by OR gating the outputs of two AND functions. Variations of inverting and non-inverting inputs are available.

Design Entry Method

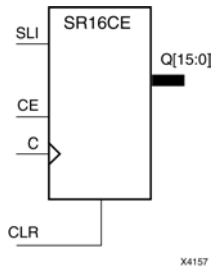
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SR16CE

Macro: 16-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a shift register with a shift-left serial input (SLI), parallel outputs (Q), and clock enable (CE) and asynchronous clear (CLR) inputs. The (CLR) input, when High, overrides all other inputs and resets the data outputs (Q) Low. When (CE) is High and (CLR) is Low, the data on the SLI input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent Low-to-High clock transitions, when (CE) is High and (CLR) is Low, data shifts to the next highest bit position as new data is loaded into (Q0) (SLI→Q0, Q0→Q1, Q1→Q2, and so forth). The register ignores clock transitions when (CE) is Low.

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), and (CLR) in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs				Outputs	
CLR	CE	SLI	C	Q0	Qz : Q1
1	X	X	X	0	0
0	0	X	X	No Change	No Change
0	1	SLI	↑	SLI	qn-1
z = bit width - 1					
qn-1 = state of referenced output one setup time prior to active clock transition					

Design Entry Method

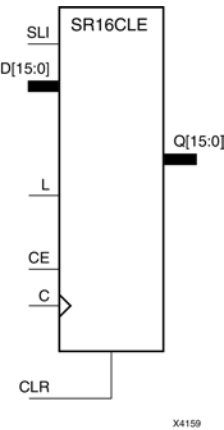
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SR16CLE

Macro: 16-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a shift register with a shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and asynchronous clear (CLR) . The register ignores clock transitions when (L) and (CE) are Low. The asynchronous (CLR), when High, overrides all other inputs and resets the data outputs (Q) Low. When (L) is High and (CLR) is Low, data on the Dn -D0 inputs is loaded into the corresponding Qn -(Q0) bits of the register.

When (CE) is High and (L) and (CLR) are Low, data on the SLI input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent clock transitions, when (CE) is High and (L) and (CLR) are Low, the data shifts to the next highest bit position as new data is loaded into (Q)0 (for example, SLI→Q0, Q0→Q1, and Q1→Q2).

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), (L), and (CLR) inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs						Outputs	
CLR	L	CE	SLI	Dn : D0	C	Q0	Qz : Q1
1	X	X	X	X	X	0	0
0	1	X	X	Dn : D0	↑	D0	Dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	0	X	X	X	No Change	No Change
z = bitwidth -1							

qn-1 = state of referenced output one setup time prior to active clock transition

Design Entry Method

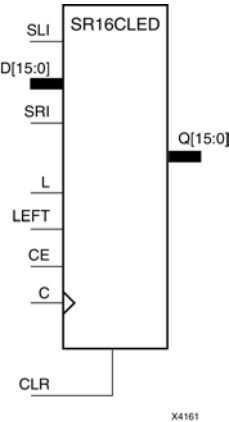
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SR16CLED

Macro: 16-Bit Shift Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q), and four control inputs: clock enable (CE), load enable (L), shift left/right (LEFT), and asynchronous clear (CLR). The register ignores clock transitions when (CE) and (L) are Low. The asynchronous clear, when High, overrides all other inputs and resets the data outputs (Qn) Low.

When (L) is High and (CLR) is Low, the data on the (D) inputs is loaded into the corresponding (Q) bits of the register. When (CE) is High and (L) and (CLR) are Low, data is shifted right or left, depending on the state of the LEFT input. If LEFT is High, data on the SLI is loaded into (Q0) during the Low-to-High clock transition and shifted left (for example, to Q1 or Q2) during subsequent clock transitions. If LEFT is Low, data on the SRI is loaded into the last (Q) output during the Low-to-High clock transition and shifted right during subsequent clock transitions. The logic tables indicate the state of the (Q) outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs								Outputs		
CLR	L	CE	LEFT	SLI	SRI	D15 : D0	C	Q0	Q15	Q14 : Q1
1	X	X	X	X	X	X	X	0	0	0
0	1	X	X	X	X	D15 : D0	↑	D0	D15	Dn
0	0	0	X	X	X	X	X	No Change	No Change	No Change
0	0	1	1	SLI	X	X	↑	SLI	q14	qn-1
0	0	1	0	X	SRI	X	↑	q1	SRI	qn+1
qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition.										

Design Entry Method

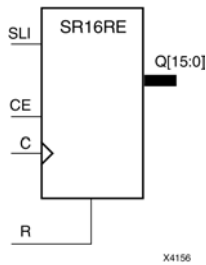
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SR16RE

Macro: 16-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset



Introduction

This design element is a shift register with shift-left serial input (SLI), parallel outputs (Qn), clock enable (CE), and synchronous reset (R) inputs. The R input, when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low.

When (CE) is High and (R) is Low, the data on the (SLI) is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent Low-to-High clock transitions, when (CE) is High and R is Low, data shifts to the next highest bit position as new data is loaded into (Q0) (for example, SLI→Q0, Q0→Q1, and Q1→Q2). The register ignores clock transitions when (CE) is Low.

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), and (R) in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs	
R	CE	SLI	C	Q0	Qz : Q1
1	X	X	↑	0	0
0	0	X	X	No Change	No Change
0	1	SLI	↑	SLI	qn-1
z = bitwidth -1					
qn-1 = state of referenced output one setup time prior to active clock transition					

Design Entry Method

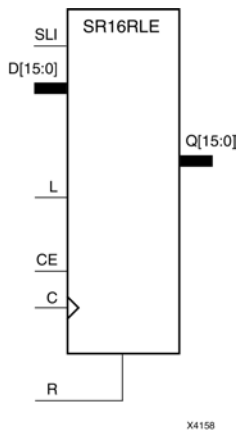
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SR16RLE

Macro: 16-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset



Introduction

This design element is a shift register with shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and synchronous reset (R). The register ignores clock transitions when (L) and (CE) are Low. The synchronous (R), when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When (L) is High and (R) is Low during the Low-to-High clock transition, data on the (D) inputs is loaded into the corresponding Q bits of the register.

When (CE) is High and (L) and (R) are Low, data on the (SLI) input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when (CE) is High and (L) and (R) are Low, the data shifts to the next highest bit position as new data is loaded into Q0.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, (CE), (L), and (R) inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs						Outputs	
R	L	CE	SLI	Dz : D0	C	Q0	Qz : Q1
1	X	X	X	X	↑	0	0
0	1	X	X	Dz : D0	↑	D0	Dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	0	X	X	X	No Change	No Change
z = bitwidth -1							
qn-1 = state of referenced output one setup time prior to active clock transition							

Design Entry Method

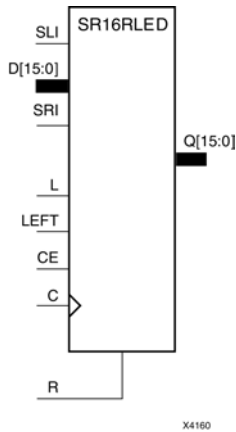
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SR16RLED

Macro: 16-Bit Shift Register with Clock Enable and Synchronous Reset



Introduction

This design element is a shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q) and four control inputs — clock enable (CE), load enable (L), shift left/right (LEFT), and synchronous reset (R). The register ignores clock transitions when (CE) and (L) are Low. The synchronous (R), when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When (L) is High and (R) is Low during the Low-to-High clock transition, the data on the (D) inputs is loaded into the corresponding (Q) bits of the register.

When (CE) is High and (L) and (R) are Low, data shifts right or left, depending on the state of the LEFT input. If LEFT is High, data on (SLI) is loaded into (Q0) during the Low-to-High clock transition and shifted left (for example, to Q1 and Q2) during subsequent clock transitions. If LEFT is Low, data on the (SRI) is loaded into the last (Q) output during the Low-to-High clock transition and shifted right) during subsequent clock transitions. The logic tables below indicates the state of the (Q) outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs								Outputs		
R	L	CE	LEFT	SLI	SRI	D15:D0	C	Q0	Q15	Q14:Q1
1	X	X	X	X	X	X	↑	0	0	0
0	1	X	X	X	X	D15:D0	↑	D0	D15	Dn
0	0	0	X	X	X	X	X	No Change	No Change	No Change
0	0	1	1	SLI	X	X	↑	SLI	q14	qn-1
0	0	1	0	X	SRI	X	↑	q1	SRI	qn+1
qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition										

Design Entry Method

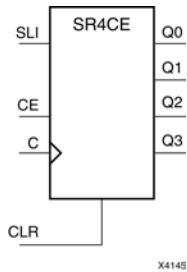
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SR4CE

Macro: 4-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a shift register with a shift-left serial input (SLI), parallel outputs (Q), and clock enable (CE) and asynchronous clear (CLR) inputs. The (CLR) input, when High, overrides all other inputs and resets the data outputs (Q) Low. When (CE) is High and (CLR) is Low, the data on the SLI input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent Low-to-High clock transitions, when (CE) is High and (CLR) is Low, data shifts to the next highest bit position as new data is loaded into (Q0) (SLI→Q0, Q0→Q1, Q1→Q2, and so forth). The register ignores clock transitions when (CE) is Low.

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), and (CLR) in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs	
CLR	CE	SLI	C	Q0	Qz : Q1
1	X	X	X	0	0
0	0	X	X	No Change	No Change
0	1	SLI	↑	SLI	qn-1
z = bit width - 1					
qn-1 = state of referenced output one setup time prior to active clock transition					

Design Entry Method

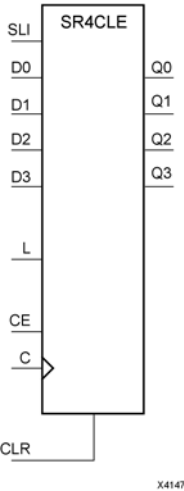
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SR4CLE

Macro: 4-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a shift register with a shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and asynchronous clear (CLR) . The register ignores clock transitions when (L) and (CE) are Low. The asynchronous (CLR), when High, overrides all other inputs and resets the data outputs (Q) Low. When (L) is High and (CLR) is Low, data on the Dn -D0 inputs is loaded into the corresponding Qn -(Q0) bits of the register.

When (CE) is High and (L) and (CLR) are Low, data on the SLI input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent clock transitions, when (CE) is High and (L) and (CLR) are Low, the data shifts to the next highest bit position as new data is loaded into (Q)0 (for example, SLI→Q0, Q0→Q1, and Q1→Q2).

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), (L), and (CLR) inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs						Outputs	
CLR	L	CE	SLI	Dn : D0	C	Q0	Qz : Q1
1	X	X	X	X	X	0	0
0	1	X	X	Dn : D0	↑	D0	Dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	0	X	X	X	No Change	No Change
z = bitwidth -1							

qn-1 = state of referenced output one setup time prior to active clock transition

Design Entry Method

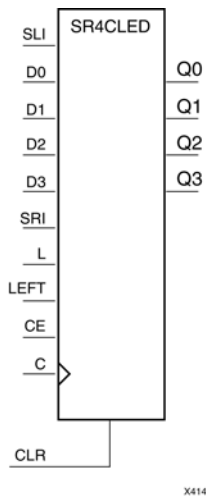
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SR4CLED

Macro: 4-Bit Shift Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q), and four control inputs: clock enable (CE), load enable (L), shift left/right (LEFT), and asynchronous clear (CLR). The register ignores clock transitions when (CE) and (L) are Low. The asynchronous clear, when High, overrides all other inputs and resets the data outputs (Qn) Low.

When (L) is High and (CLR) is Low, the data on the (D) inputs is loaded into the corresponding (Q) bits of the register. When (CE) is High and (L) and (CLR) are Low, data is shifted right or left, depending on the state of the LEFT input. If LEFT is High, data on the SLI is loaded into (Q0) during the Low-to-High clock transition and shifted left (for example, to Q1 or Q2) during subsequent clock transitions. If LEFT is Low, data on the SRI is loaded into the last (Q) output during the Low-to-High clock transition and shifted right during subsequent clock transitions. The logic tables indicate the state of the (Q) outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs								Outputs		
CLR	L	CE	LEFT	SLI	SRI	D3 : D0	C	Q0	Q3	Q2 : Q1
1	X	X	X	X	X	X	X	0	0	0
0	1	X	X	X	X	D3– D0	↑	D0	D3	Dn
0	0	0	X	X	X	X	X	No Change	No Change	No Change
0	0	1	1	SLI	X	X	↑	SLI	q2	qn-1
0	0	1	0	X	SRI	X	↑	q1	SRI	qn+1

qn-1 and qn+1 = state of referenced output one setup time prior to active clock transition.

Design Entry Method

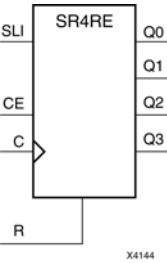
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SR4RE

Macro: 4-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset



Introduction

This design element is a shift register with shift-left serial input (SLI), parallel outputs (Qn), clock enable (CE), and synchronous reset (R) inputs. The R input, when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low.

When (CE) is High and (R) is Low, the data on the (SLI) is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent Low-to-High clock transitions, when (CE) is High and R is Low, data shifts to the next highest bit position as new data is loaded into (Q0) (for example, SLI→Q0, Q0→Q1, and Q1→Q2). The register ignores clock transitions when (CE) is Low.

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), and (R) in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs				Outputs	
R	CE	SLI	C	Q0	Qz : Q1
1	X	X	↑	0	0
0	0	X	X	No Change	No Change
0	1	SLI	↑	SLI	qn-1
z = bitwidth -1					
qn-1 = state of referenced output one setup time prior to active clock transition					

Design Entry Method

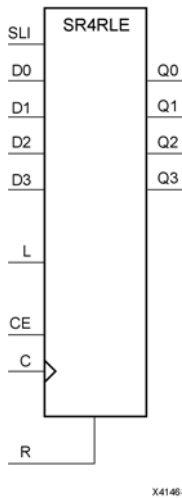
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SR4RLE

Macro: 4-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset



Introduction

This design element is a shift register with shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and synchronous reset (R). The register ignores clock transitions when (L) and (CE) are Low. The synchronous (R), when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When (L) is High and (R) is Low during the Low-to-High clock transition, data on the (D) inputs is loaded into the corresponding Q bits of the register.

When (CE) is High and (L) and (R) are Low, data on the (SLI) input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when (CE) is High and (L) and (R) are Low, the data shifts to the next highest bit position as new data is loaded into Q0.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, (CE), (L), and (R) inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs						Outputs	
R	L	CE	SLI	Dz : D0	C	Q0	Qz : Q1
1	X	X	X	X	↑	0	0
0	1	X	X	Dz : D0	↑	D0	Dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	0	X	X	X	No Change	No Change
z = bitwidth -1							
qn-1 = state of referenced output one setup time prior to active clock transition							

Design Entry Method

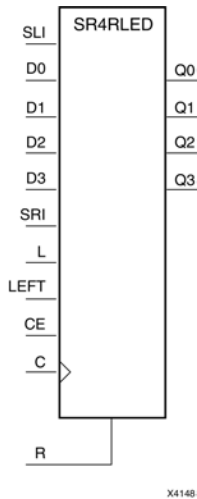
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SR4RLED

Macro: 4-Bit Shift Register with Clock Enable and Synchronous Reset



Introduction

This design element is a shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q) and four control inputs — clock enable (CE), load enable (L), shift left/right (LEFT), and synchronous reset (R). The register ignores clock transitions when (CE) and (L) are Low. The synchronous (R), when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When (L) is High and (R) is Low during the Low-to-High clock transition, the data on the (D) inputs is loaded into the corresponding (Q) bits of the register.

When (CE) is High and (L) and (R) are Low, data shifts right or left, depending on the state of the LEFT input. If LEFT is High, data on (SLI) is loaded into (Q0) during the Low-to-High clock transition and shifted left (for example, to Q1 and Q2) during subsequent clock transitions. If LEFT is Low, data on the (SRI) is loaded into the last (Q) output during the Low-to-High clock transition and shifted right) during subsequent clock transitions. The logic tables below indicates the state of the (Q) outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs								Outputs		
R	L	CE	LEFT	SLI	SRI	D3 : D0	C	Q0	Q3	Q2 : Q1
1	X	X	X	X	X	X	↑	0	0	0
0	1	X	X	X	X	D3 : D0	↑	D0	D3	Dn
0	0	0	X	X	X	X	X	No Change	No Change	No Change
0	0	1	1	SLI	X	X	↑	SLI	q2	qn-1
0	0	1	0	X	SRI	X	↑	q1	SRI	qn+1
qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition										

Design Entry Method

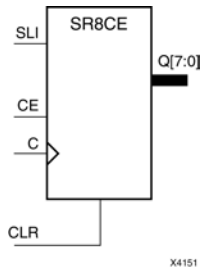
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SR8CE

Macro: 8-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a shift register with a shift-left serial input (SLI), parallel outputs (Q), and clock enable (CE) and asynchronous clear (CLR) inputs. The (CLR) input, when High, overrides all other inputs and resets the data outputs (Q) Low. When (CE) is High and (CLR) is Low, the data on the SLI input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent Low-to-High clock transitions, when (CE) is High and (CLR) is Low, data shifts to the next highest bit position as new data is loaded into (Q0) (SLI→Q0, Q0→Q1, Q1→Q2, and so forth). The register ignores clock transitions when (CE) is Low.

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), and (CLR) in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs				Outputs	
CLR	CE	SLI	C	Q0	Qz : Q1
1	X	X	X	0	0
0	0	X	X	No Change	No Change
0	1	SLI	↑	SLI	qn-1
z = bit width - 1					
qn-1 = state of referenced output one setup time prior to active clock transition					

Design Entry Method

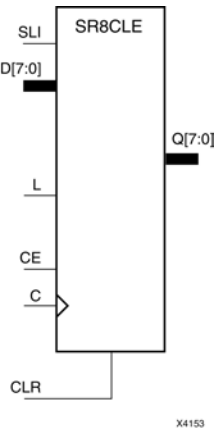
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SR8CLE

Macro: 8-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a shift register with a shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and asynchronous clear (CLR) . The register ignores clock transitions when (L) and (CE) are Low. The asynchronous (CLR), when High, overrides all other inputs and resets the data outputs (Q) Low. When (L) is High and (CLR) is Low, data on the Dn -D0 inputs is loaded into the corresponding Qn -(Q0) bits of the register.

When (CE) is High and (L) and (CLR) are Low, data on the SLI input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent clock transitions, when (CE) is High and (L) and (CLR) are Low, the data shifts to the next highest bit position as new data is loaded into (Q)0 (for example, SLI→Q0, Q0→Q1, and Q1→Q2).

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), (L), and (CLR) inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs						Outputs	
CLR	L	CE	SLI	Dn : D0	C	Q0	Qz : Q1
1	X	X	X	X	X	0	0
0	1	X	X	Dn : D0	↑	D0	Dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	0	X	X	X	No Change	No Change
z = bitwidth -1							

qn-1 = state of referenced output one setup time prior to active clock transition

Design Entry Method

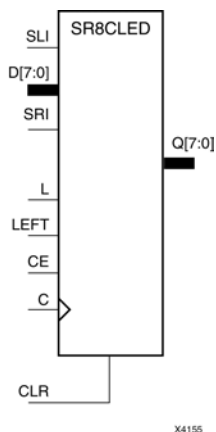
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SR8CLED

Macro: 8-Bit Shift Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q), and four control inputs: clock enable (CE), load enable (L), shift left/right (LEFT), and asynchronous clear (CLR). The register ignores clock transitions when (CE) and (L) are Low. The asynchronous clear, when High, overrides all other inputs and resets the data outputs (Qn) Low.

When (L) is High and (CLR) is Low, the data on the (D) inputs is loaded into the corresponding (Q) bits of the register. When (CE) is High and (L) and (CLR) are Low, data is shifted right or left, depending on the state of the LEFT input. If LEFT is High, data on the SLI is loaded into (Q0) during the Low-to-High clock transition and shifted left (for example, to Q1 or Q2) during subsequent clock transitions. If LEFT is Low, data on the SRI is loaded into the last (Q) output during the Low-to-High clock transition and shifted right during subsequent clock transitions. The logic tables indicate the state of the (Q) outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs								Outputs		
CLR	L	CE	LEFT	SLI	SRI	D7 : D0	C	Q0	Q7	Q6 : Q1
1	X	X	X	X	X	X	X	0	0	0
0	1	X	X	X	X	D7 : D0	↑	D0	D7	Dn
0	0	0	X	X	X	X	X	No Change	No Change	No Change
0	0	1	1	SLI	X	X	↑	SLI	q6	qn-1
0	0	1	0	X	SRI	X	↑	q1	SRI	qn+1
qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition.										

Design Entry Method

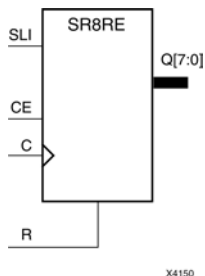
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SR8RE

Macro: 8-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset



Introduction

This design element is a shift register with shift-left serial input (SLI), parallel outputs (Qn), clock enable (CE), and synchronous reset (R) inputs. The R input, when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low.

When (CE) is High and (R) is Low, the data on the (SLI) is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent Low-to-High clock transitions, when (CE) is High and R is Low, data shifts to the next highest bit position as new data is loaded into (Q0) (for example, SLI→Q0, Q0→Q1, and Q1→Q2). The register ignores clock transitions when (CE) is Low.

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), and (R) in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs				Outputs	
R	CE	SLI	C	Q0	Qz : Q1
1	X	X	↑	0	0
0	0	X	X	No Change	No Change
0	1	SLI	↑	SLI	qn-1
z = bitwidth -1					
qn-1 = state of referenced output one setup time prior to active clock transition					

Design Entry Method

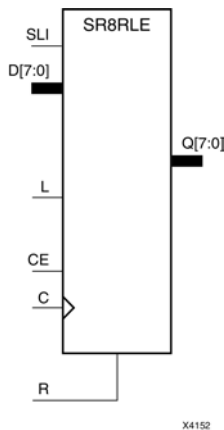
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SR8RLE

Macro: 8-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset



Introduction

This design element is a shift register with shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and synchronous reset (R). The register ignores clock transitions when (L) and (CE) are Low. The synchronous (R), when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When (L) is High and (R) is Low during the Low-to-High clock transition, data on the (D) inputs is loaded into the corresponding Q bits of the register.

When (CE) is High and (L) and (R) are Low, data on the (SLI) input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when (CE) is High and (L) and (R) are Low, the data shifts to the next highest bit position as new data is loaded into Q0.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, (CE), (L), and (R) inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs						Outputs	
R	L	CE	SLI	Dz : D0	C	Q0	Qz : Q1
1	X	X	X	X	↑	0	0
0	1	X	X	Dz : D0	↑	D0	Dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	0	X	X	X	No Change	No Change
z = bitwidth -1							
qn-1 = state of referenced output one setup time prior to active clock transition							

Design Entry Method

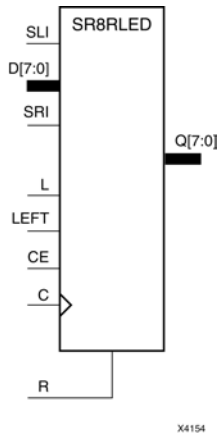
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SR8RLED

Macro: 8-Bit Shift Register with Clock Enable and Synchronous Reset



Introduction

This design element is a shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q) and four control inputs — clock enable (CE), load enable (L), shift left/right (LEFT), and synchronous reset (R). The register ignores clock transitions when (CE) and (L) are Low. The synchronous (R), when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When (L) is High and (R) is Low during the Low-to-High clock transition, the data on the (D) inputs is loaded into the corresponding (Q) bits of the register.

When (CE) is High and (L) and (R) are Low, data shifts right or left, depending on the state of the LEFT input. If LEFT is High, data on (SLI) is loaded into (Q0) during the Low-to-High clock transition and shifted left (for example, to Q1 and Q2) during subsequent clock transitions. If LEFT is Low, data on the (SRI) is loaded into the last (Q) output during the Low-to-High clock transition and shifted right) during subsequent clock transitions. The logic tables below indicates the state of the (Q) outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs								Outputs		
R	L	CE	LEFT	SLI	SRI	D7 : D0	C	Q0	Q7	Q6 : Q1
1	X	X	X	X	X	X	↑	0	0	0
0	1	X	X	X	X	D7 : D0	↑	D0	D7	Dn
0	0	0	X	X	X	X	X	No Change	No Change	No Change
0	0	1	1	SLI	X	X	↑	SLI	q6	qn-1
0	0	1	0	X	SRI	X	↑	q1	SRI	qn+1
qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition										

Design Entry Method

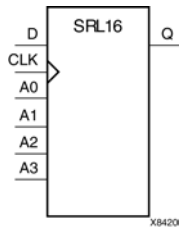
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SRL16

Primitive: 16-Bit Shift Register Look-Up Table (LUT)



Introduction

This design element is a shift register look-up table (LUT). The inputs A3, A2, A1, and A0 select the output length of the shift register.

The shift register can be of a fixed, static length or it can be dynamically adjusted.

- **To create a fixed-length shift register** -Drive the A3 through A0 inputs with static values. The length of the shift register can vary from 1 bit to 16 bits, as determined by the following formula: $\text{Length} = (8 \times A3) + (4 \times A2) + (2 \times A1) + A0 + 1$. If A3, A2, A1, and A0 are all zeros (0000), the shift register is one bit long. If they are all ones (1111), it is 16 bits long.
- **To change the length of the shift register dynamically** -Change the values driving the A3 through A0 inputs. For example, if A2, A1, and A0 are all ones (111) and A3 toggles between a one (1) and a zero (0), the length of the shift register changes from 16 bits to 8 bits. Internally, the length of the shift register is always 16 bits and the input lines A3 through A0 select which of the 16 bits reach the output.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

The data (D) is loaded into the first bit of the shift register during the Low-to-High clock (CLK) transition. During subsequent Low-to-High clock transitions data shifts to the next highest bit position while new data is loaded. The data appears on the Q output when the shift register length determined by the address inputs is reached.

Logic Table

Inputs			Output
A _m	CLK	D	Q
A _m	X	X	Q(A _m)
A _m	↑	D	Q(A _m - 1)
m = 0, 1, 2, 3			

Design Entry Method

This design element can be used in schematics.

Available Attributes

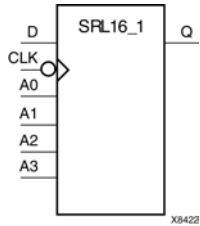
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Sets the initial value of Q output after configuration.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SRL16_1

Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Negative-Edge Clock



Introduction

This design element is a shift register look-up table (LUT). The inputs A3, A2, A1, and A0 select the output length of the shift register.

The shift register can be of a fixed, static length or it can be dynamically adjusted.

- **To create a fixed-length shift register** -Drive the A3 through A0 inputs with static values. The length of the shift register can vary from 1 bit to 16 bits, as determined by the following formula: $\text{Length} = (8 \times A3) + (4 \times A2) + (2 \times A1) + A0 + 1$. If A3, A2, A1, and A0 are all zeros (0000), the shift register is one bit long. If they are all ones (1111), it is 16 bits long.
- **To change the length of the shift register dynamically** -Change the values driving the A3 through A0 inputs. For example, if A2, A1, and A0 are all ones (111) and A3 toggles between a one (1) and a zero (0), the length of the shift register changes from 16 bits to 8 bits. Internally, the length of the shift register is always 16 bits and the input lines A3 through A0 select which of the 16 bits reach the output.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

The data (D) is loaded into the first bit of the shift register during the High-to-Low clock (CLK) transition. During subsequent High-to-Low clock transitions data shifts to the next highest bit position as new data is loaded. The data appears on the Q output when the shift register length determined by the address inputs is reached.

Logic Table

Inputs			Output
A _m	CLK	D	Q
A _m	X	X	Q(A _m)
A _m	↓	D	Q(A _m - 1)
m = 0, 1, 2, 3			

Design Entry Method

This design element can be used in schematics.

Available Attributes

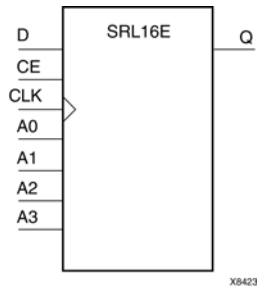
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Sets the initial value of Q output after configuration

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SRL16E

Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Clock Enable



Introduction

This design element is a shift register look-up table (LUT). The inputs A3, A2, A1, and A0 select the output length of the shift register.

The shift register can be of a fixed, static length or it can be dynamically adjusted.

- **To create a fixed-length shift register** -Drive the A3 through A0 inputs with static values. The length of the shift register can vary from 1 bit to 16 bits, as determined by the following formula: $\text{Length} = (8 \times A3) + (4 \times A2) + (2 \times A1) + A0 + 1$. If A3, A2, A1, and A0 are all zeros (0000), the shift register is one bit long. If they are all ones (1111), it is 16 bits long.
- **To change the length of the shift register dynamically** -Change the values driving the A3 through A0 inputs. For example, if A2, A1, and A0 are all ones (111) and A3 toggles between a one (1) and a zero (0), the length of the shift register changes from 16 bits to 8 bits. Internally, the length of the shift register is always 16 bits and the input lines A3 through A0 select which of the 16 bits reach the output.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

When CE is High, the data (D) is loaded into the first bit of the shift register during the Low-to-High clock (CLK) transition. During subsequent Low-to-High clock transitions, when CE is High, data shifts to the next highest bit position as new data is loaded. The data appears on the Q output when the shift register length determined by the address inputs is reached. When CE is Low, the register ignores clock transitions.

Logic Table

Inputs				Output
Am	CE	CLK	D	Q
Am	0	X	X	Q(Am)
Am	1	↑	D	Q(Am - 1)
m = 0, 1, 2, 3				

Port Descriptions

Port	Direction	Width	Function
Q	Output	1	Shift register data output
D	Input	1	Shift register data input
CLK	Input	1	Clock
CE	Input	1	Active high clock enable
A	Input	4	Dynamic depth selection of the SRL <ul style="list-style-type: none">A=0000 ==> 1-bit shift lengthA=1111 ==> 16-bit shift length

Design Entry Method

This design element can be used in schematics.

Available Attributes

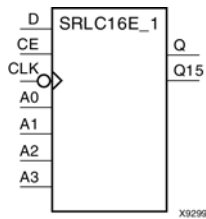
Attribute	Type	Allowed Values	Default	Description
INIT	Hexa-decimal	Any 16-Bit Value	All zeros	Sets the initial value of content and output of shift register after configuration.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SRL16E_1

Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Negative-Edge Clock and Clock Enable



Introduction

This design element is a shift register look-up table (LUT) with clock enable (CE). The inputs A3, A2, A1, and A0 select the output length of the shift register.

The shift register can be of a fixed, static length or it can be dynamically adjusted.

- **To create a fixed-length shift register** -Drive the A3 through A0 inputs with static values. The length of the shift register can vary from 1 bit to 16 bits, as determined by the following formula: $\text{Length} = (8 \times A3) + (4 \times A2) + (2 \times A1) + A0 + 1$. If A3, A2, A1, and A0 are all zeros (0000), the shift register is one bit long. If they are all ones (1111), it is 16 bits long.
- **To change the length of the shift register dynamically** -Change the values driving the A3 through A0 inputs. For example, if A2, A1, and A0 are all ones (111) and A3 toggles between a one (1) and a zero (0), the length of the shift register changes from 16 bits to 8 bits. Internally, the length of the shift register is always 16 bits and the input lines A3 through A0 select which of the 16 bits reach the output.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

When CE is High, the data (D) is loaded into the first bit of the shift register during the High-to-Low clock (CLK) transition. During subsequent High-to-Low clock transitions, when CE is High, data is shifted to the next highest bit position as new data is loaded. The data appears on the Q output when the shift register length determined by the address inputs is reached. When CE is Low, the register ignores clock transitions.

Logic Table

Inputs				Output
Am	CE	CLK	D	Q
Am	0	X	X	Q(Am)
Am	1	↓	D	Q(Am - 1)
m= 0, 1, 2, 3				

Design Entry Method

This design element can be used in schematics.

Available Attributes

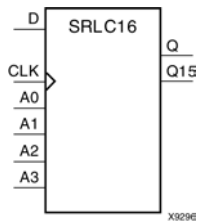
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Sets the initial value of content and output of shift register after configuration.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SRLC16

Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Carry



Introduction

This design element is a shift register look-up table (LUT) with Carry. The inputs A3, A2, A1, and A0 select the output length of the shift register.

The shift register can be of a fixed, static length or it can be dynamically adjusted.

- **To create a fixed-length shift register** -Drive the A3 through A0 inputs with static values. The length of the shift register can vary from 1 bit to 16 bits, as determined by the following formula: $\text{Length} = (8 \times A3) + (4 \times A2) + (2 \times A1) + A0 + 1$. If A3, A2, A1, and A0 are all zeros (0000), the shift register is one bit long. If they are all ones (1111), it is 16 bits long.
- **To change the length of the shift register dynamically** -Change the values driving the A3 through A0 inputs. For example, if A2, A1, and A0 are all ones (111) and A3 toggles between a one (1) and a zero (0), the length of the shift register changes from 16 bits to 8 bits. Internally, the length of the shift register is always 16 bits and the input lines A3 through A0 select which of the 16 bits reach the output.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

The data (D) is loaded into the first bit of the shift register during the Low-to-High clock (CLK) transition. During subsequent Low-to-High clock transitions data shifts to the next highest bit position as new data is loaded. The data appears on the Q output when the shift register length determined by the address inputs is reached.

Note The Q15 output is available for you in cascading to multiple shift register LUTs to create larger shift registers.

Logic Table

Inputs			Output
A _m	CLK	D	Q
A _m	X	X	Q(A _m)
A _m	↑	D	Q(A _m - 1)
m = 0, 1, 2, 3			

Design Entry Method

This design element can be used in schematics.

Available Attributes

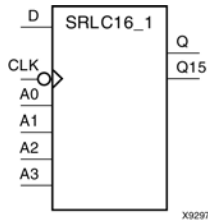
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Sets the initial value of content and output of shift register after configuration.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SRLC16_1

Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Carry and Negative-Edge Clock



Introduction

This design element is a shift register look-up table (LUT) with carry and a negative-edge clock. The inputs A3, A2, A1, and A0 select the output length of the shift register.

The shift register can be of a fixed, static length or it can be dynamically adjusted.

- **To create a fixed-length shift register** -Drive the A3 through A0 inputs with static values. The length of the shift register can vary from 1 bit to 16 bits, as determined by the following formula: $\text{Length} = (8 \times A3) + (4 \times A2) + (2 \times A1) + A0 + 1$. If A3, A2, A1, and A0 are all zeros (0000), the shift register is one bit long. If they are all ones (1111), it is 16 bits long.
- **To change the length of the shift register dynamically** -Change the values driving the A3 through A0 inputs. For example, if A2, A1, and A0 are all ones (111) and A3 toggles between a one (1) and a zero (0), the length of the shift register changes from 16 bits to 8 bits. Internally, the length of the shift register is always 16 bits and the input lines A3 through A0 select which of the 16 bits reach the output.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

Note The Q15 output is available for your use in cascading multiple shift register LUTs to create larger shift registers.

Logic Table

Inputs			Output	
Am	CLK	D	Q	Q15
Am	X	X	Q(Am)	No Change
Am	↓	D	Q(Am - 1)	Q14
m= 0, 1, 2, 3				

Design Entry Method

This design element can be used in schematics.

Available Attributes

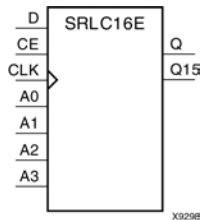
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Sets the initial value of content and output of shift register after configuration.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SRLC16E

Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Carry and Clock Enable



Introduction

This design element is a shift register look-up table (LUT) with carry and clock enable. The inputs A3, A2, A1, and A0 select the output length of the shift register.

The shift register can be of a fixed, static length or it can be dynamically adjusted.

- **To create a fixed-length shift register** -Drive the A3 through A0 inputs with static values. The length of the shift register can vary from 1 bit to 16 bits, as determined by the following formula: $\text{Length} = (8 \times A3) + (4 \times A2) + (2 \times A1) + A0 + 1$. If A3, A2, A1, and A0 are all zeros (0000), the shift register is one bit long. If they are all ones (1111), it is 16 bits long.
- **To change the length of the shift register dynamically** -Change the values driving the A3 through A0 inputs. For example, if A2, A1, and A0 are all ones (111) and A3 toggles between a one (1) and a zero (0), the length of the shift register changes from 16 bits to 8 bits. Internally, the length of the shift register is always 16 bits and the input lines A3 through A0 select which of the 16 bits reach the output.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

The data (D) is loaded into the first bit of the shift register during the Low-to-High clock (CLK) transition. When CE is High, during subsequent Low-to-High clock transitions, data shifts to the next highest bit position as new data is loaded. The data appears on the Q output when the shift register length determined by the address inputs is reached.

Note The Q15 output is available for you in cascading to multiple shift register LUTs to create larger shift registers.

Logic Table

Inputs				Output	
Am	CLK	CE	D	Q	Q15
Am	X	0	X	Q(Am)	Q(15)
Am	X	1	X	Q(Am)	Q(15)
Am	↑	1	D	Q(Am - 1)	Q15
m= 0, 1, 2, 3					

Design Entry Method

This design element can be used in schematics.

Available Attributes

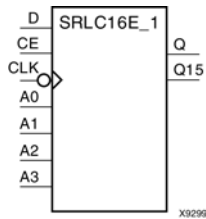
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Sets the initial value of content and output of shift register after configuration.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SRLC16E_1

Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Carry, Negative-Edge Clock, and Clock Enable



Introduction

This design element is a shift register look-up table (LUT) with carry, clock enable, and negative-edge clock. The inputs A3, A2, A1, and A0 select the output length of the shift register.

The shift register can be of a fixed, static length or it can be dynamically adjusted.

- **To create a fixed-length shift register** -Drive the A3 through A0 inputs with static values. The length of the shift register can vary from 1 bit to 16 bits, as determined by the following formula: $\text{Length} = (8 \times A3) + (4 \times A2) + (2 \times A1) + A0 + 1$. If A3, A2, A1, and A0 are all zeros (0000), the shift register is one bit long. If they are all ones (1111), it is 16 bits long.
- **To change the length of the shift register dynamically** -Change the values driving the A3 through A0 inputs. For example, if A2, A1, and A0 are all ones (111) and A3 toggles between a one (1) and a zero (0), the length of the shift register changes from 16 bits to 8 bits. Internally, the length of the shift register is always 16 bits and the input lines A3 through A0 select which of the 16 bits reach the output.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

When CE is High, the data (D) is loaded into the first bit of the shift register during the High-to-Low clock (CLK) transition. During subsequent High-to-Low clock transitions data shifts to the next highest bit position as new data is loaded when CE is High. The data appears on the Q output when the shift register length determined by the address inputs is reached.

Note The Q15 output is available for your use in cascading multiple shift register LUTs to create larger shift registers.

Logic Table

Inputs				Output	
Am	CE	CLK	D	Q	Q15
Am	0	X	X	Q(Am)	No Change
Am	1	X	X	Q(Am)	No Change
Am	1	↓	D	Q(Am -1)	Q14
m= 0, 1, 2, 3					

Design Entry Method

This design element can be used in schematics.

Available Attributes

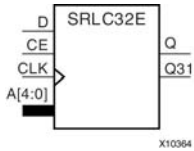
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Sets the initial value of content and output of shift register after configuration.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

SRLC32E

Primitive: 32 Clock Cycle, Variable Length Shift Register Look-Up Table (LUT) with Clock Enable



Introduction

This design element is a variable length, 1 to 32 clock cycle shift register implemented within a single look-up table (LUT). The shift register can be of a fixed length, static length, or it can be dynamically adjusted by changing the address lines to the component. This element also features an active, high-clock enable and a cascading feature in which multiple SRLC32Es can be cascaded in order to create greater shift lengths.

Port Descriptions

Port	Direction	Width	Function
Q	Output	1	Shift register data output
Q31	Output	1	Shift register cascaded output (connect to the D input of a subsequent SRLC32E)
D	Input	1	Shift register data input
CLK	Input	1	Clock
CE	Input	1	Active high clock enable
A	Input	5	Dynamic depth selection of the SRL A=00000 ==> 1-bit shift length A=11111 ==> 32-bit shift length

Design Entry Method

This design element can be used in schematics.

If instantiated, the following connections should be made to this component:

- Connect the CLK input to the desired clock source, the D input to the data source to be shifted/stored and the Q output to either an FDCPE or an FDRSE input or other appropriate data destination.
- The CE clock enable pin can be connected to a clock enable signal in the design or else tied to a logic one if not used.
- The 5-bit A bus can either be tied to a static value between 0 and 31 to signify a fixed 1 to 32 bit static shift length, or else it can be tied to the appropriate logic to enable a varying shift depth anywhere between 1 and 32 bits.
- If you want to create a longer shift length than 32, connect the Q31 output pin to the D input pin of a subsequent SRLC32E to cascade and create larger shift registers.
- It is not valid to connect the Q31 output to anything other than another SRLC32E.
- The selectable Q output is still available in the cascaded mode, if needed.
- An optional INIT attribute consisting of a 32-bit Hexadecimal value can be specified to indicate the initial shift pattern of the shift register.
- (INIT[0] will be the first value shifted out.)

Available Attributes

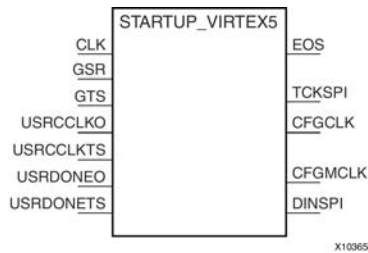
Attribute	Type	Allowed Values	Default	Description
INIT	Hexa-decimal	Any 32-Bit Value	All zeros	Specifies the initial shift pattern of the SRLC32E.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

STARTUP_VIRTEX5

Primitive: Virtex®-5 Configuration Start-Up Sequence Interface



Introduction

This design element is used to interface device pins and logic to the Global Set/Reset (GSR) signal, the Global Tristate (GTS) dedicated routing, the internal configuration signals, or the input pins for the SPI PROM if an SPI PROM is used to configure the device. This primitive can also be used to specify a different clock for the device startup sequence at the end of configuring the device, and to access the configuration clock to the internal logic.

Port Descriptions

Port	Direction	Width	Function
EOS	Output	1	Active high signal indicates the End Of Configuration.
CFGCLK	Output	1	Configuration main clock output
CFGMCLK	Output	1	Configuration internal oscillator clock output
USRCCLKO	Input	1	Internal user CCLK
USRCCLKTS	Input	1	Internal user CCLK tristate enable
USRDONEO	Input	1	Internal user DONE pin output control
USRDONETS	Input	1	User DONE tristate enable
TCK_SPI	Output	1	Internal access to the TCK configuration pin when using SPI PROM configuration
DIN_SPI	Output	1	Internal access to the DIN configuration pin when using SPI PROM configuration
GSR	Input	1	Active high Global Set/Reset (GSR) signal
GTS	Input	1	Active high Global Tristate (GTS) signal
CLK	Input	1	User start-up clock

Design Entry Method

This design element can be used in schematics.

If the dedicated Global Tristate (GTS) is to be used, connect the appropriate sourcing pin or logic to the GTS input pin of the primitive. In order to specify a clock for the startup sequence of configuration, connect a clock from the design to the CLK pin of this design element. CFGMCLK and CFGCLK allow access to the internal configuration clocks, while EOS signals the end of the configuration startup sequence.

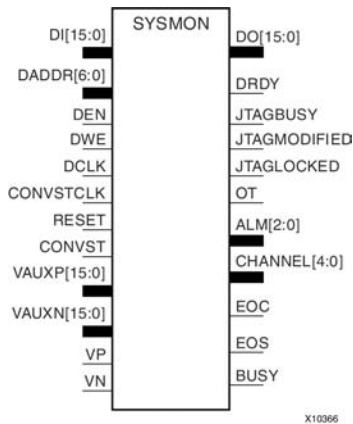
If you are configuring the device using a SPI PROM, and access to the SPI PROM is necessary after configuration, use the TCK_SPI and DIN_SPI pins of the component to gain access to the otherwise dedicated configuration input pins.

For More Information

- See the [Virtex-5 FPGA Configuration User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).
- See the [Virtex-5 FPGA User Guide](#).

SYSMON

Primitive: System Monitor



Introduction

This design element is built around a 10-bit, 200-kSPS (kilosamples per second) Analog-to-Digital Converter (ADC). When combined with a number of on-chip sensors, the ADC is used to measure FPGA physical operating parameters, including on-chip power supply voltages and die temperatures. Access to external voltages is provided through a dedicated analog-input pair (VP/VN) and 16 user-selectable analog inputs, known as auxiliary analog inputs (VAUXP[15:0], VAUXN[15:0]). The external analog inputs allow the ADC to monitor the physical environment of the board or enclosure.

Port Descriptions

Port	Type	Width	Function
ALM[2:0]	Output	3	3-bit output alarm for temp, Vccint and Vccaux
BUSY	Output	1	1-bit output ADC busy signal
CHANNEL[4:0]	Output	5	5-bit output channel selection
CONVST	Input	1	1-bit input convert start
CONVSTCLK	Input	1	1-bit input convert start clock
DADDR[6:0]	Input	7	7-bit input address bus for dynamic reconfig
DCLK	Input	1	1-bit input clock for dynamic reconfig
DEN	Input	1	1-bit input enable for dynamic reconfig
DI[15:0]	Input	16	16-bit input data bus for dynamic reconfig
DO[15:0]	Output	16	16-bit output data bus for dynamic reconfig
DRDY	Output	1	1-bit output data ready for dynamic reconfig
DWE	Input	1	1-bit input write enable for dynamic reconfig
EOC	Output	1	1-bit output end of conversion
EOS	Output	1	1-bit output end of sequence
JTAGBUSY	Output	1	1-bit output JTAG DRP busy
JTAGLOCKED	Output	1	1-bit output DRP port lock

Port	Type	Width	Function
JTAGMODIFIED	Output	1	1-bit output JTAG write to DRP
OT	Output	1	1-bit output over temperature alarm
RESET	Input	1	1-bit input active high reset
VAUXN[15:0]	Input	16	16-bit input N-side auxiliary analog input
VAUXP[15:0]	Input	16	16-bit input P-side auxiliary analog input
VN	Input	1	1-bit input N-side analog input
VP	Input	1	1-bit input P-side analog input

Design Entry Method

Connect all desired input and output ports and set the appropriate attributes for the desired behavior of this component. For simulation, provide a text file to give the analog and temperature to the model. The format for this file is as follows:

```
// Must use valid headers on all columns
// Comments can be added to the stimulus file using '///'
TIME TEMP VCCAUX VCCINT VP VN VAUXP[0] VAUXN[0]
00000 45 2.5 1.0 0.5 0.0 0.7 0.0
05000 85 2.45 1.1 0.3 0.0 0.2 0.0
// Time stamp data is in nano seconds (ns)
// Temperature is recorded in C (degrees centigrade)
// All other channels are recorded as V (Volts)
// Valid column headers are:
// TIME, TEMP, VCCAUX, VCCINT, VP, VN,
// VAUXP[0], VAUXN[0],.....VAUXP[15], VAUXN[15]
// External analog inputs are differential so VP = 0.5 and VN = 0.0 the
// input on channel VP/VN is 0.5 - 0.0 = 0.5V
```

Note When compiling the included code, please do not add any extraneous spaces to the text as this could cause compilation to fail.

This design element can be used in schematics.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT_40	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Configuration register 0
INIT_41	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Configuration register 1
INIT_42	Hexa-decimal	16'h0000 to 16'hffff	16'h0800	Configuration register 2
INIT_43	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Test register 0
INIT_44	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Test register 1
INIT_45	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Test register 2
INIT_46	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Test register 3
INIT_47	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Test register 4

Attribute	Type	Allowed_Values	Default	Description
INIT_48	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Sequence register 0
INIT_49	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Sequence register 1
INIT_4A	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Sequence register 2
INIT_4B	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Sequence register 3
INIT_4C	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Sequence register 4
INIT_4D	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Sequence register 5
INIT_4E	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Sequence register 6
INIT_4F	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Sequence register 7
INIT_50	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Alarm limit register 0
INIT_51	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Alarm limit register 1
INIT_52	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Alarm limit register 2
INIT_53	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Alarm limit register 3
INIT_54	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Alarm limit register 4
INIT_55	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Alarm limit register 5
INIT_56	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Alarm limit register 6
INIT_57	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Alarm limit register 7
SIM_DEVICE	String	"VIRTEX5", "VIRTEX6"	"VIRTEX5"	Allows the simulation model to reflect the reduction of the minimum divide ratio between the DRP clock (DCLK) and the lower frequency ADC clock (ADCCLOCK) from 8 to 2.
SIM_MONITOR_FILE	String	0 bit String	design.txt	Simulation analog entry file

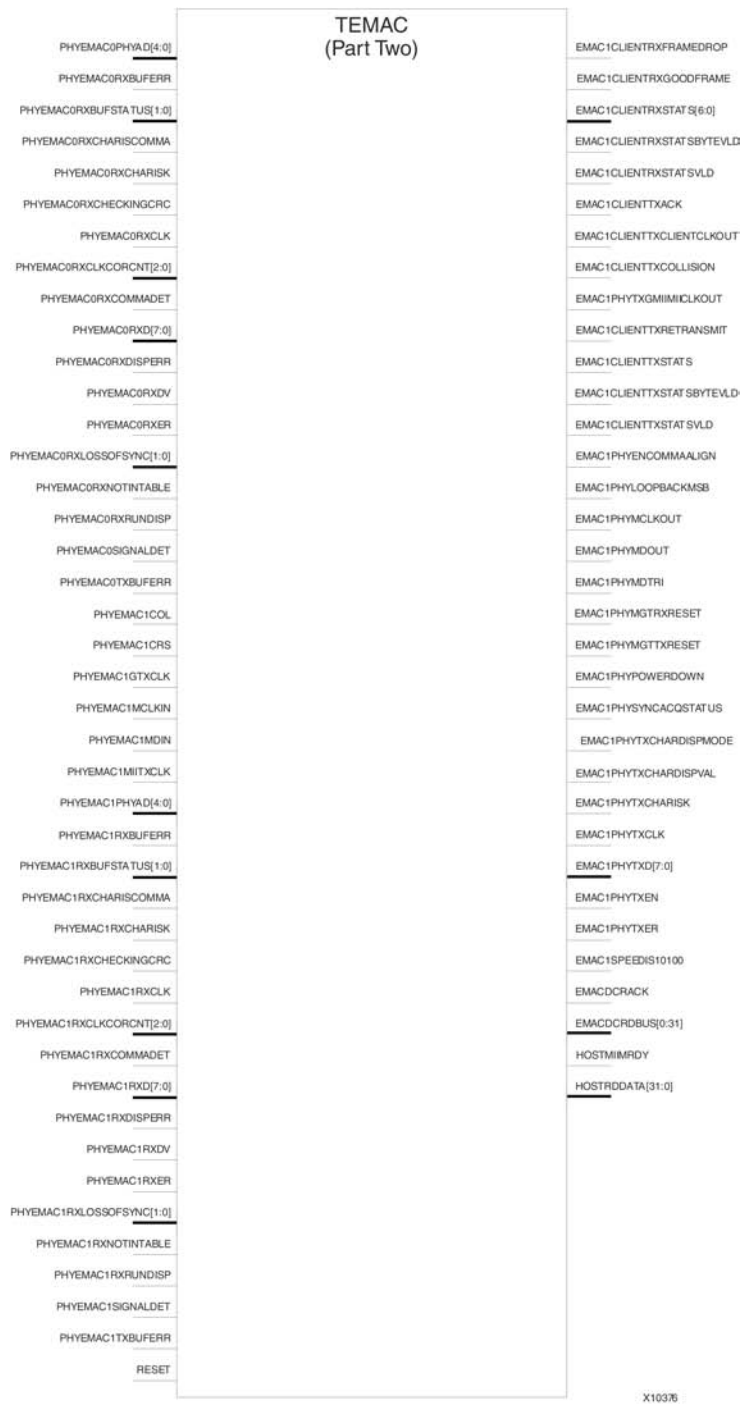
For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

TEMAC

Primitive: Tri-mode Ethernet Media Access Controller (MAC)





Introduction

This design element contains paired embedded Ethernet MACs that are independently configurable to meet all common Ethernet system connectivity needs.

Design Entry Method

This design element can be used in schematics.

For More Information

- See the [Virtex-5 Embedded Tri-Mode Ethernet MAC User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).
- See the [Virtex-5 FPGA User Guide](#).

USR_ACCESS_VIRTEX5

Primitive: Virtex-5 User Access Register



Introduction

This design element enables you to access a 32-bit register within the configuration logic. You will thus be able to read the data from the bitstream. One use case for this component is to allow data stored in bitstream storage source to be accessed by the FPGA design after configuration.

Port Descriptions

Port	Direction	Width	Function
DATA	Output	32	Configuration Output Data
DATAVALID	Output	1	Active high DATA port contains valid data.
CFGCLK	Output	1	Configuration Clock

Design Entry Method

This design element can be used in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

VCC

Primitive: VCC-Connection Signal Tag



Introduction

This design element serves as a signal tag, or parameter, that forces a net or input function to a logic High level. A net tied to this element cannot have any other source.

When the placement and routing software encounters a net or input function tied to this element, it removes any logic that is disabled by the Vcc signal, which is only implemented when the disabled logic cannot be removed.

Design Entry Method

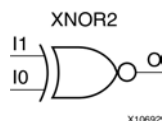
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

XNOR2

Primitive: 2-Input XNOR Gate with Non-Inverted Inputs



Introduction

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

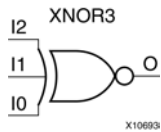
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

XNOR3

Primitive: 3-Input XNOR Gate with Non-Inverted Inputs



Introduction

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

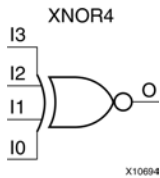
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

XNOR4

Primitive: 4-Input XNOR Gate with Non-Inverted Inputs



Introduction

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

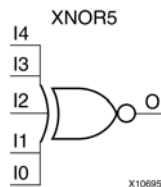
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

XNOR5

Primitive: 5-Input XNOR Gate with Non-Inverted Inputs



Introduction

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

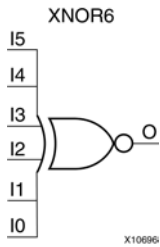
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

XNOR6

Macro: 6-Input XNOR Gate with Non-Inverted Inputs



Introduction

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

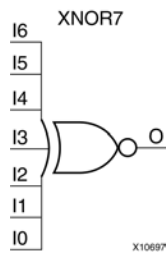
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

XNOR7

Macro: 7-Input XNOR Gate with Non-Inverted Inputs



Introduction

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

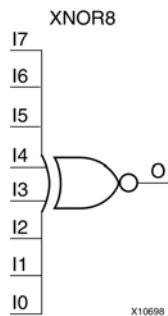
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

XNOR8

Macro: 8-Input XNOR Gate with Non-Inverted Inputs



Introduction

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

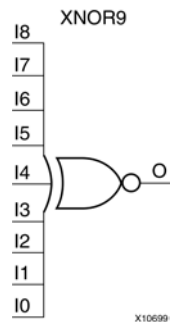
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

XNOR9

Macro: 9-Input XNOR Gate with Non-Inverted Inputs



Introduction

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

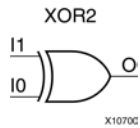
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

XOR2

Primitive: 2-Input XOR Gate with Non-Inverted Inputs



Introduction

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

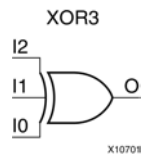
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

XOR3

Primitive: 3-Input XOR Gate with Non-Inverted Inputs



Introduction

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

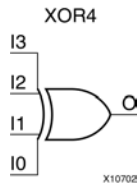
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

XOR4

Primitive: 4-Input XOR Gate with Non-Inverted Inputs



Introduction

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

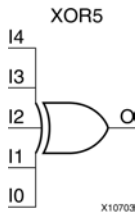
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

XOR5

Primitive: 5-Input XOR Gate with Non-Inverted Inputs



Introduction

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

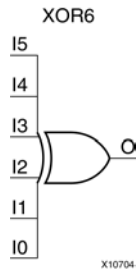
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

XOR6

Macro: 6-Input XOR Gate with Non-Inverted Inputs



Introduction

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

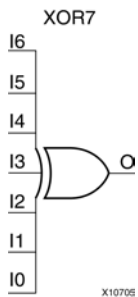
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

XOR7

Macro: 7-Input XOR Gate with Non-Inverted Inputs



Introduction

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

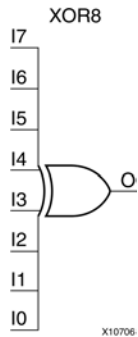
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

XOR8

Macro: 8-Input XOR Gate with Non-Inverted Inputs



Introduction

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

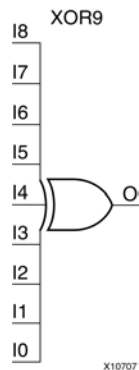
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

XOR9

Macro: 9-Input XOR Gate with Non-Inverted Inputs



Introduction

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

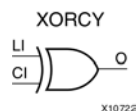
This design element is only for use in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).

XORCY

Primitive: XOR for Carry Logic with General Output



Introduction

This design element is a special XOR with general O output that generates faster and smaller arithmetic functions. The XORCY primitive is a dedicated XOR function within the carry-chain logic of the slice. It allows for fast and efficient creation of arithmetic (add/subtract) or wide logic functions (large AND/OR gate).

Logic Table

Input		Output
LI	CI	O
0	0	0
0	1	1
1	0	1
1	1	0

Design Entry Method

This design element can be used in schematics.

For More Information

- See the [Virtex-5 FPGA User Guide](#).
- See the [Virtex-5 FPGA Data Sheet DC and Switching Characteristics](#).