PlanAhead Software Tutorial

I/O Pin Planning

UG674 (v 13.1) March 1, 2011

XILINX®

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/01/2011	13.1	Update for the 13.1 release.

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PlanAhead Software Tutorial: I/O Pin Planning

Introduction

This tutorial introduces the Xilinx® PlanAhead™ software capabilities and benefits when performing I/O pin assignment for FPGA devices. It describes the procedure for creating and assigning I/O ports to physical package pins. The I/O Planner environment enables you to create, import, and configure the initial list of I/O ports. You can group the related ports into Interfaces and then assign them to package pins.

The capabilities include fully automatic pin placement or semi-automated interactive modes to allow controlled I/O port assignment. The I/O Planner environment shows the relationship of the physical package pins and banks with their corresponding I/O die pads. Intelligent decisions can be made to optimize the connectivity between the PCB and the FGPA device.

You can perform I/O pin assignment at various stages of the design cycle. You can perform I/O exploration and assignment with a pin planning project even before the design source files are available. You can import a Comma Separated Value (CSV) format file for I/O planning, or export it for use in PCB schematic symbol or Hardware Description Language (HDL) header generation.

The PlanAhead software also enables you to I/O pin plan in the elaborated Register Transfer Level (RTL) design or in the synthesized netlist design. The PlanAhead software performs more comprehensive I/O and clocking DRCs when using a netlist design. This tutorial covers both.

Not all commands or command options are covered in this tutorial. This tutorial uses the features contained in the PlanAhead software, which is bundled as a part of ISE® Design Suite version 13.

Tutorial Objectives

The objective of this tutorial is to familiarize you with the I/O pin planning process using the I/O Planner functionality in the PlanAhead software.

Getting Started

Software Requirements

The PlanAhead software is installed with ISE Design Suite software. Before starting the tutorial, be sure that the PlanAhead software is operational, and that the tutorial design data is installed.

For installation instructions and information, see the *ISE Design Suite: Installation and Licensing Guide (UG798)* cited in Appendix A, Additional Resources.

Hardware Requirements

Xilinx recommends a minimum of 2 GB of RAM when using the PlanAhead software on larger devices. For this tutorial, a smaller xc6vlx75t design is used, and the number of designs open at one time is limited. Although 1 GB is sufficient, it can impact performance.

Tutorial Design Description

The small sample design used in this tutorial includes:

- A RISC processor CPU core
- A pseudo FFT
- Four gigabit transceivers (GTs)
- Two USB interfaces

The design targets an xc6vlx75t device. A small design is used to:

- Allow the tutorial to be run with minimal hardware requirements
- Enable timely completion of the tutorials
- Minimize data size

Locating Tutorial Design Files

This tutorial uses the design data that is included with the example projects in the PlanAhead software. It is also available on the Xilinx website.

1. Download the `PlanAhead_Tutorial.zip` file from either:
   - The example projects area in the PlanAhead software installation: `<ISE_install_area>/PlanAhead/testcases/`
   - The Xilinx website: http://www.xilinx.com/support/documentation/dt_planahead_planahead13-1_tutorials.htm
2. Extract the zip file contents into any write-accessible location.

The unzipped PlanAhead_Tutorial data directory is referred to in this tutorial as the `<Extract_Dir>`.

The tutorial sample design data is modified while performing this tutorial. A new copy of the original `PlanAhead_Tutorial` data is required each time you run the tutorial.

Tutorial Steps

This tutorial consists of the following I/O pin planning steps:

Step 1: Creating an I/O Pin Planning Project

The PlanAhead software provides an I/O Pin Planning view layout that displays views more applicable to placing I/O Ports and clock logic. You can open the I/O planning layout without a design in order to analyze device resources. It is also available for an RTL, netlist or implemented design.

Creating a New Project, Opening the I/O Planner Environment, and Exploring the Views

1. Open the PlanAhead software and create the project_pinout I/O Pin Planning project.
   - On Windows, double-click the Xilinx PlanAhead 13 Desktop icon, or select **Start > Programs > Xilinx ISE Design Suite 13.x > PlanAhead > PlanAhead**.
   - On Linux, go to *<Extract_Dir>*/PlanAhead_Tutorial/Tutorial_Created_Data directory and type **PlanAhead**.
2. In the Getting Started page, select **Create New Project**.
3. Click **Next** to confirm the project creation and to display the Project Name page.
4. Type the Project name, **project_pinout**.
5. Enter the Project location:

   <Extract_Dir>/PlanAhead_Tutorial/Tutorial_Created_Data.

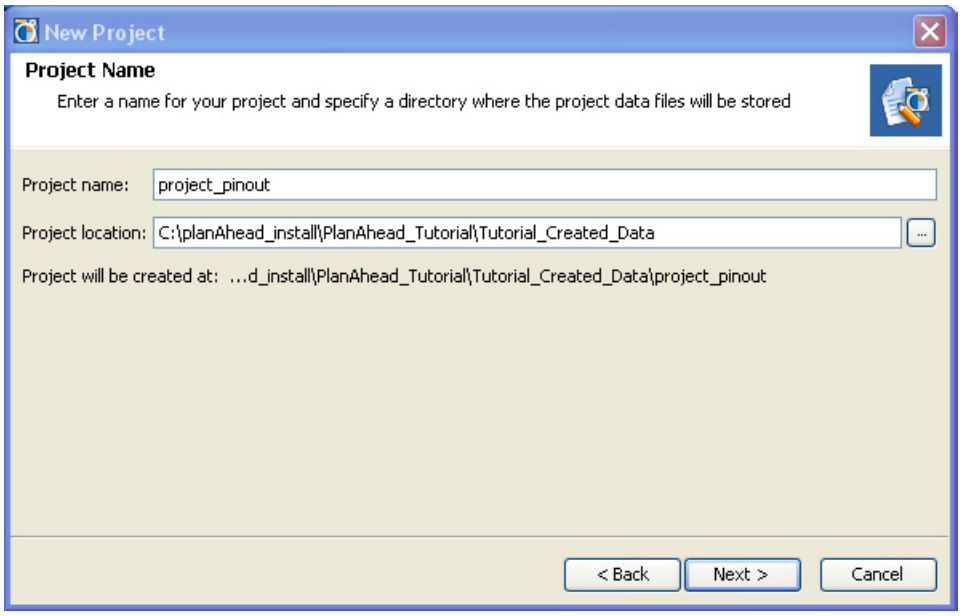

Figure 1: **Defining New Project Name and Location**

6. Click **Next** to open the Design Source page.
7. Select **Create an I/O Planning Project**.

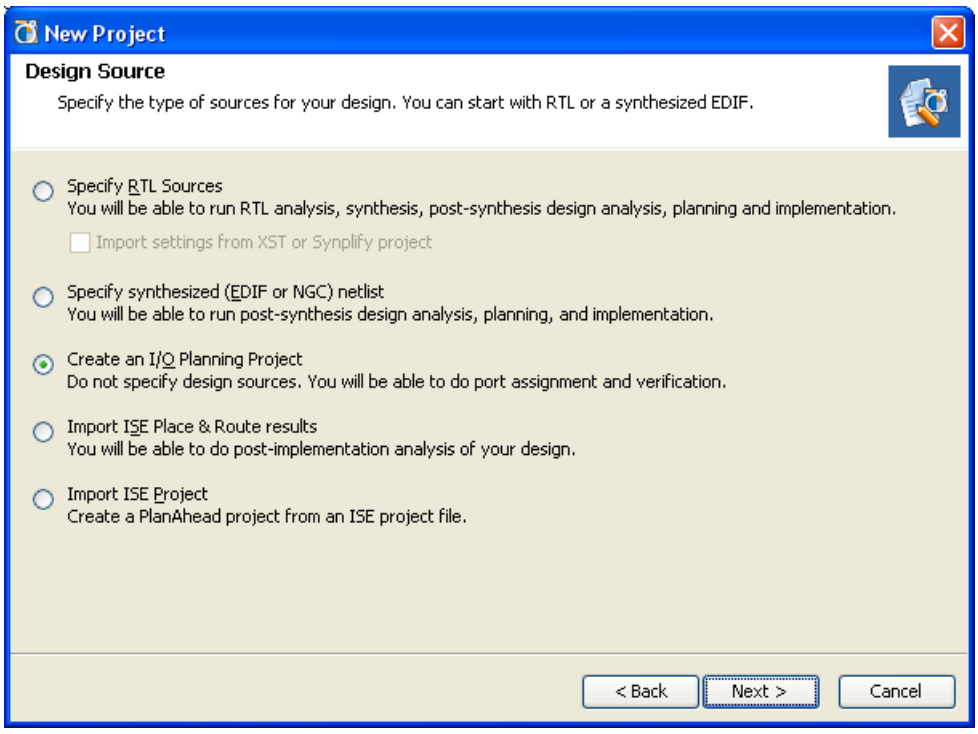

Figure 2: **Specifying an I/O Pin Planning Project**

8. Click **Next** to open the Import Ports page.
9. Select **Do not import I/O ports at this time**.

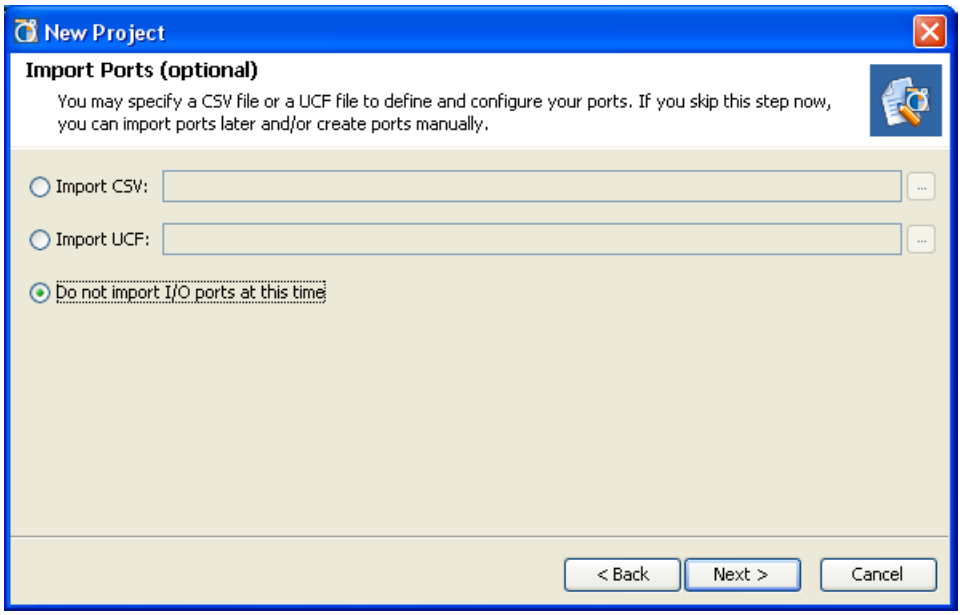

Figure 3: **Importing Ports**

10. Click **Next** to open the Default Part selector page.
11. In the Filter section, click the **Family** pull down menu and select **Virtex6**. Notice the list is filtered to show Virtex®-6 devices only.

12. Click the **Sub-Family** pull down menu and select **Virtex6 LXT**. Notice the list is filtered to show Virtex-6 LXT devices only.
13. In the Search field, type **`75T`**. Notice the 75T devices listed (see Figure 4).

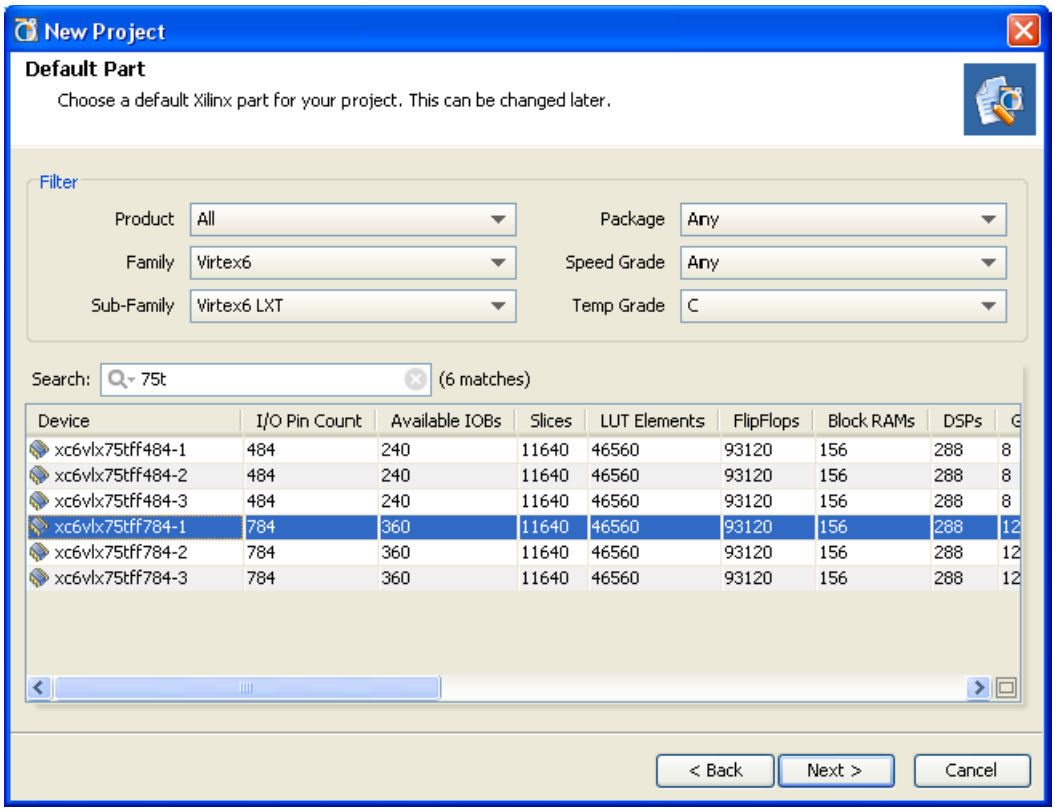

Figure 4: **Selecting a Family and Default Part**

14. Select the **xc6vlx75tff784-1** device and click **Next**.
15. Click **Finish** to create the project, as shown in Figure 5.

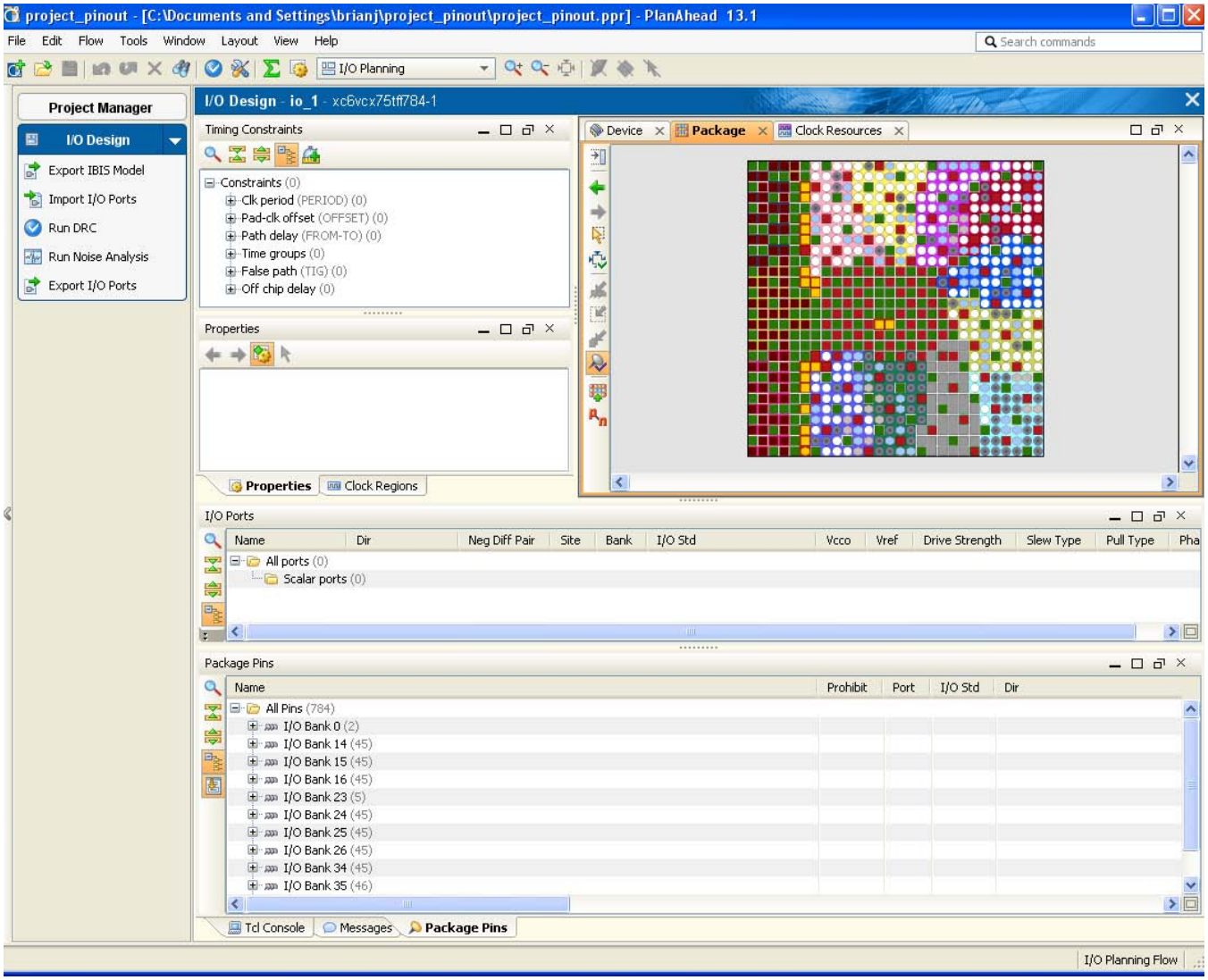

Figure 5: **I/O Pin Planning Environment**

16. Explore the various views in the I/O Planning layout. Many are empty as no I/O Ports have been defined yet.

Step 2: Examining Device I/O Resources

The PlanAhead software I/O pin planning environment lets you explore various device resources.

The different views graphically display and cross-select the location of various I/O, clock, and logic objects to help you make I/O and device-related design decisions. The Package Pins view and I/O Bank Properties view provide some I/O related information typically found in the device data sheets.

Next, you will:

- Select several I/O banks to show the package-to-die relationship
- View I/O bank properties
- Select and expand the I/O Bank 14 to view package pin specifications

Examining I/O Banks

1. In the Package Pins view, select **I/O Bank 14** as shown in Figure 6. To do so, double clicking a pin from the I/O bank. The first click selects the pin, and the second click selects the I/O bank that the pin is part of.

The I/O bank location is highlighted in the Package view.

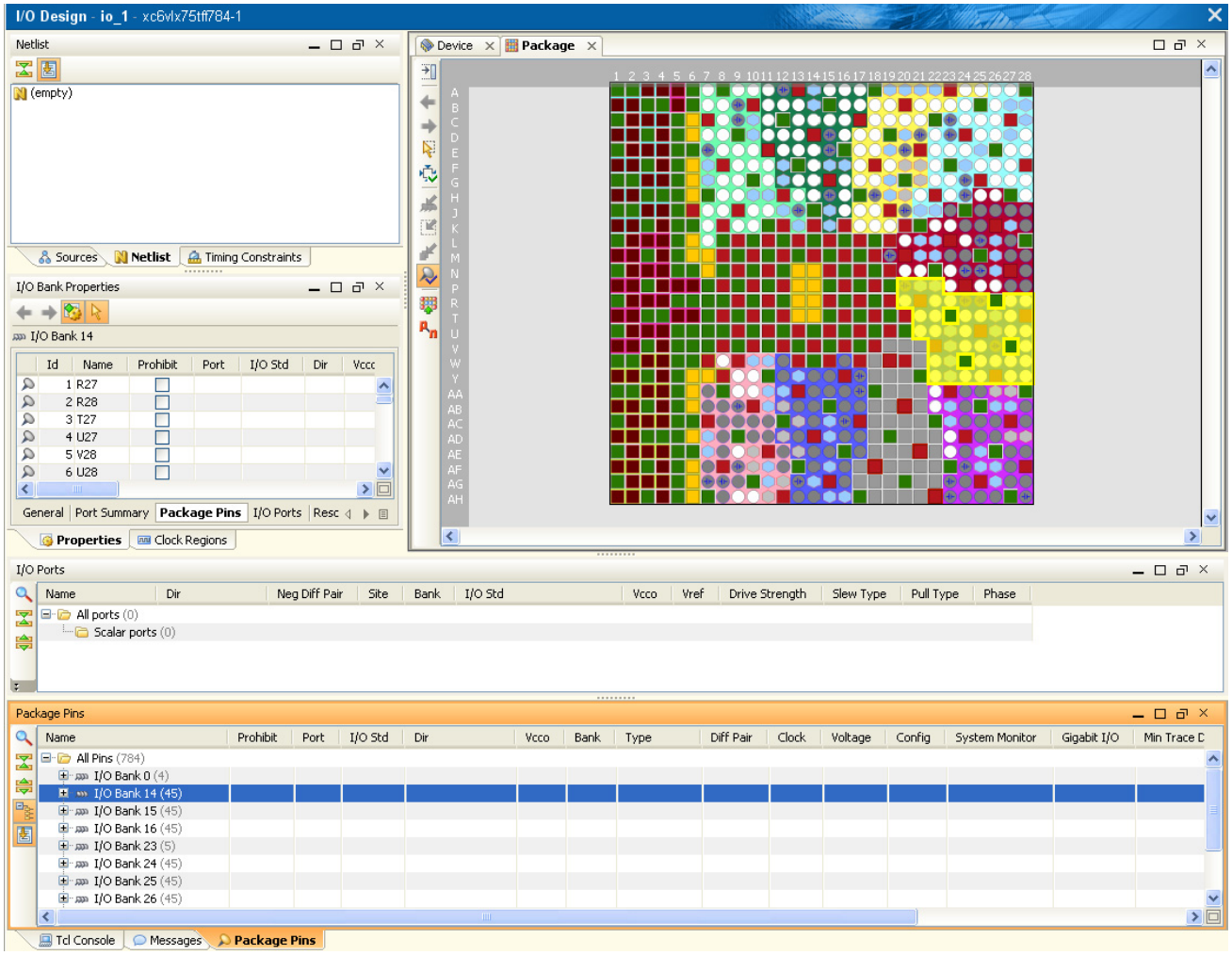

Figure 6: **Cross Highlighting I/Os and I/O Banks**

2. Click the **Device** view tab in the Workspace to view the I/O bank location on the die.

   Being able to visualize the I/O bank locations both internally and externally helps you plan for an optimal I/O port assignment.
3. Click the **Package** view in the Workspace to bring it into view.
4. Expand **I/O Bank 14** in the Package Pins view to display the package pin information for each pin in the I/O Bank. The internal package trace min and max delays are shown also. These are the routing delays between the pin on the package and the pad on the die.
5. Scroll down the list and select any I/O Bank.
6. Select the **General** tab in the I/O Bank Properties view.
7. Review the I/O count and voltages. This information is populated as I/O Ports are assigned to the I/O bank. This allows you to search for compatible I/O banks to place the remaining I/O Ports.
8. Select the various tabs in the I/O Bank Properties view.

9. Click the Maximize button in the Package Pins view banner.

   The Package Pins view is maximized.

10. Select the Expand All button in the Package Pins view.

    Scroll and view the pin information in the table.

11. Unselect the Group by I/O Bank button in the Package Pins view to expand and flatten the list.

Prohibiting Pins from I/O Assignment

You can prohibit I/O package pins from having I/O Ports assigned to them. In the following sequence, you will sort the Package Pins view by Voltage to select all VREF I/O pins, then use the Set Prohibits popup command to prohibit placement on those pins.

1. Click the **Voltage** column header twice and scroll to the top of the list to locate the VREF values.
2. Use the **Shift** key to select all VREF Voltage pins.
3. Right-click and select **Set Prohibit**.
4. In the Package Pins view header, click the Restore button .

   The Package Pins view is restored. The Package view now displays prohibited pins.

5. In the main toolbar, click Unselect All .
6. Zoom in to an area of the Package view to view the Prohibited pins marked with red Xs, as shown in Figure 7.

   To zoom, draw a rectangle in the Package view starting at the upper left of the zoom area and drag to the lower right zoom area.

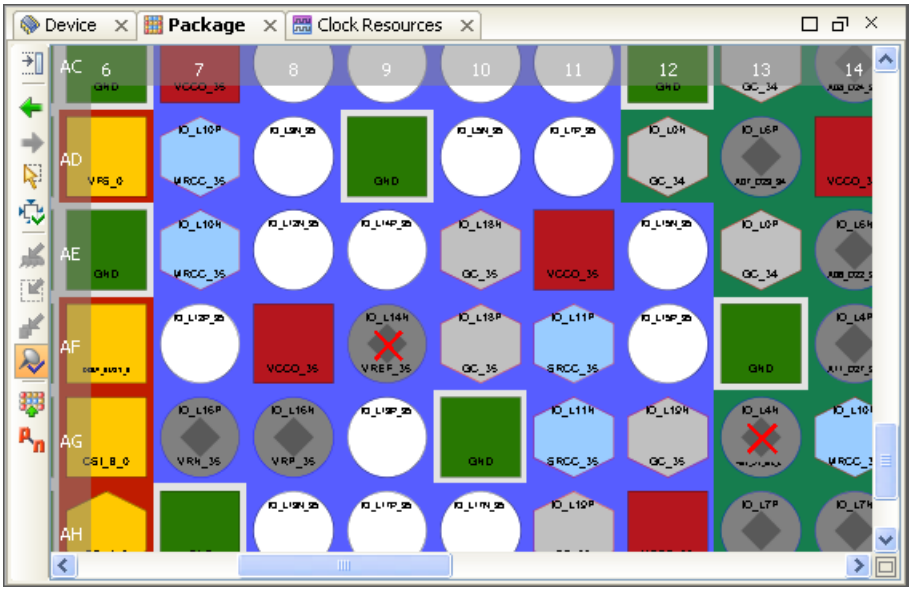

Figure 7: **Examining Prohibited VREF Package Pins**

7. Zoom Fit the Package view. Click and drag the cursor from the lower right to the upper left in a diagonal motion.
8. In the Package Pins view, click the Group by I/O Bank button  .
9. Click Collapse All  to return the tree table display to the default display structure.

The PlanAhead software has several tree table style views. There are search and filtering capabilities available in these views. See "Using Tree Table Style Views" in the Using the Viewing Environment chapter of the *PlanAhead User Guide (UG632)* cited in Appendix A, Additional Resources.

Step 3: Viewing Multi-function Pins and Setting the Device Configuration Mode

Viewing Multi-Function Pins

1. Expand the Package pins view.
2. Scroll over the columns in the list to view the multi-function pins displayed under the Type field.

Figure 8: **Viewing Multi-Function Pins**

3. Examine the following columns:
   - Device Configuration pins (Config)
   - System Monitor
   - Gigabit I/O

These logic objects can impact I/O assignment because many of them rely on multi-function pins and have fixed I/O requirements. If the design used in this tutorial contained these logic objects, this table would be filled out accordingly, allowing you to examine multi-function pins.

Setting Device Configuration Modes

The PlanAhead software allows you to set one or more device configuration options. Some configuration modes can have an impact on multi-function I/O pins also. The related pins are displayed in the Config column of the Package Pins view.

1. Select **Tools > I/O Planning > Set Configuration Modes**.

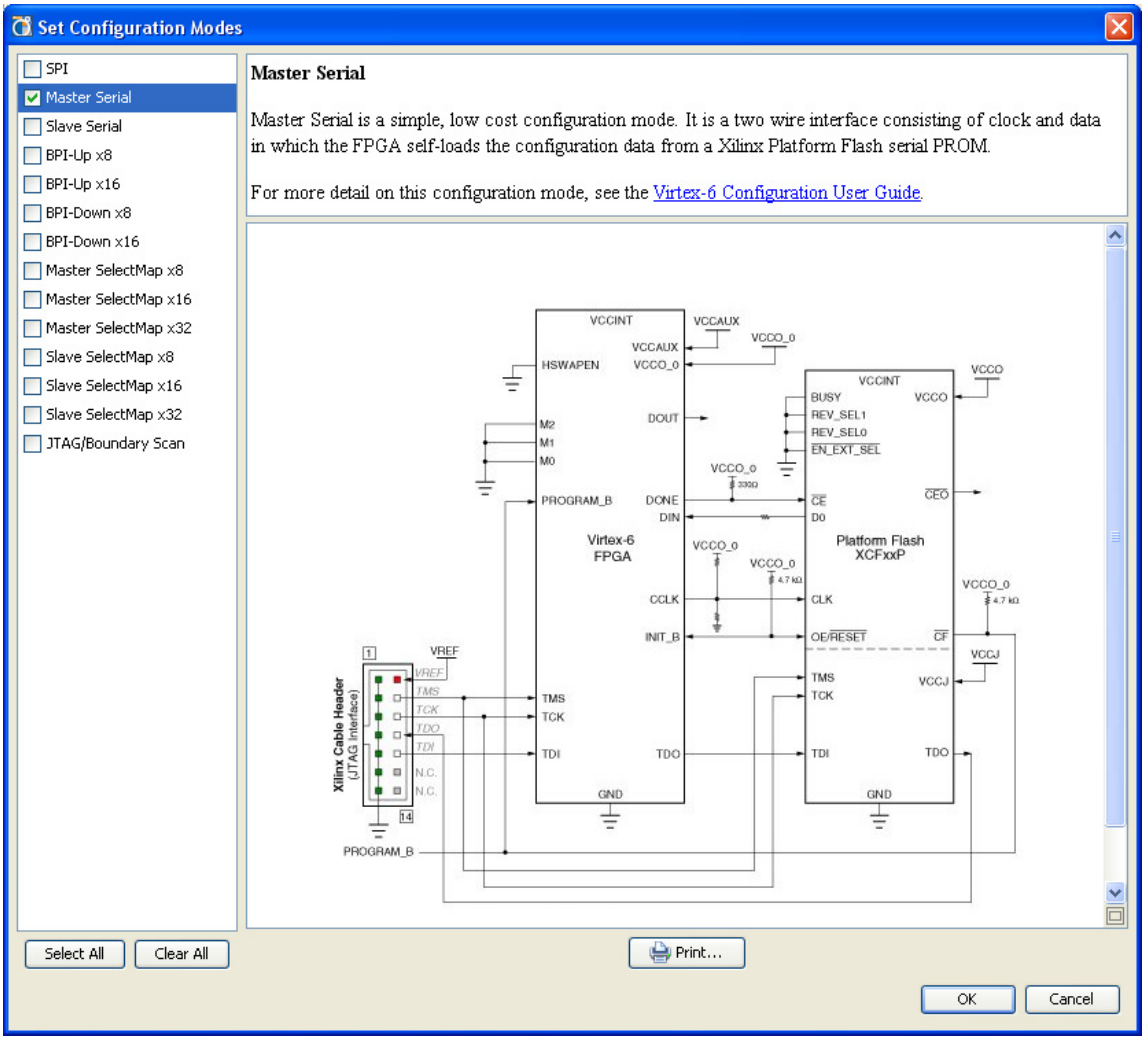

Figure 9: **Selecting Device Configuration Modes**

2. In the Set Configuration Modes dialog box, select one or two of the modes to view the descriptions, schematics, and related data sheets.
3. Click **OK**.
4. Click **OK** in the Confirmation dialog box.

   The pins associated with the selected Device Configuration Modes display in the Package Pins view allowing you to examine potential multi-function pin conflicts. There is no PCI, MCB, or other logic that could cause a conflict in this design.
5. Click the **Config** column header twice to reverse sort the list.
6. Scroll to the top to view the configuration pins and observe the pin assignments made.

Step 4: Defining Alternate Compatible Devices

During the FPGA design process, you can change the target device when a design decision calls for a larger or different type. The PlanAhead software lets you define alternate compatible devices up-front so I/O assignments can work across the selected set of devices.

This capability is limited to devices that use a common package.

Defining an Alternate Device

This step ensures that the I/O pinouts work across the selected set of devices.

1. Select **Tools > I/O Planning > Set Part Compatibility**.

   The Set Part Compatibility dialog box opens.

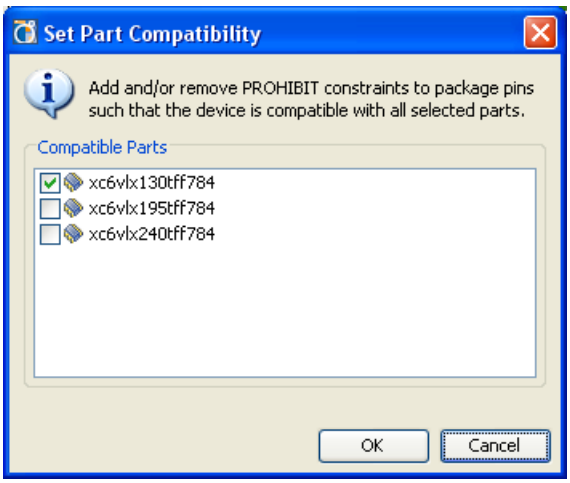

Figure 10: **Defining Compatible Parts**

2. Select the **xc6vlx130tff784** device.
3. Click **OK**.

   The Prohibits are assigned based on the most restrictive parts. In this example you are targeting the smallest device, so no prohibits are placed.

4. In the confirmation dialog box, click **OK** to indicate that no Prohibits were placed.

Step 5: Creating and Configuring I/O Ports

I/O Ports can be created and configured interactively.

Creating and Configuring a New I/O Bus Port Called mybus

1. In the I/O Ports view, right-click and select **Create I/O Ports**.
   The Create I/O Ports dialog box opens.

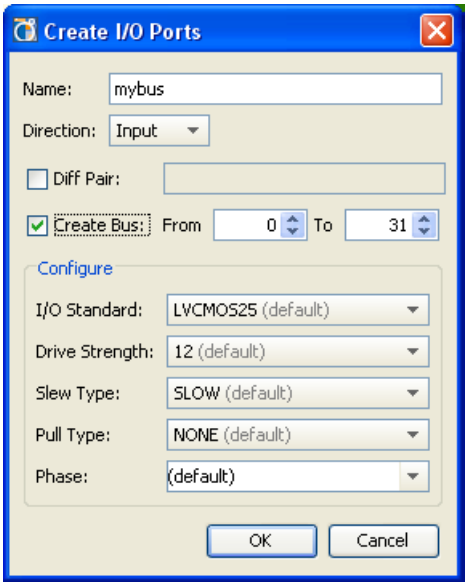

Figure 11: **Create I/O Ports**

Note: The Configure I/O Ports command opens a similar dialog box that enables you to configure existing I/O Ports.

2. Type **`mybus`** in the Name field.
3. Select **Create Bus**.
4. Accept the default dialog box options.
5. Click **OK**.

The new I/O Ports display in the I/O Ports view.

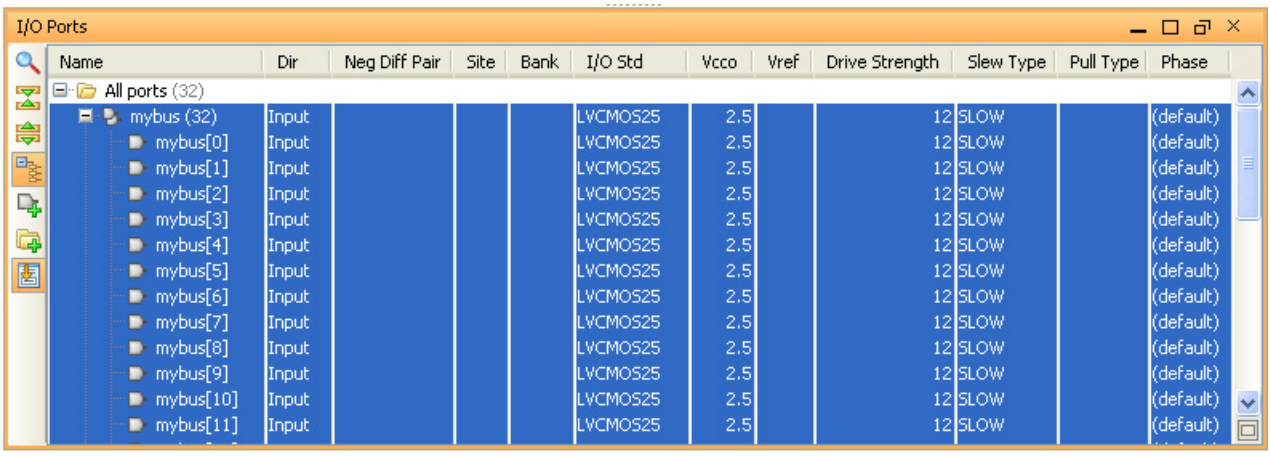

Figure 12: **Displaying Newly Added I/O Ports**

6. Select **Edit > Undo** to remove the recently added `mybus` I/O ports.

Step 6: Importing an I/O Port List

The PlanAhead software can import a variety of file formats to begin the I/O pin planning process. You can import CSV, UCF, or RTL format files and perform I/O pin exploration and assignments. You can also create I/O Ports interactively, which was covered in the last step.

Use care with early input methods for I/O pin planning. Without a synthesized netlist, the I/O Ports placement and DRC routines do not take clocks, clock relationships or GT logic into account in their calculations. When possible, perform I/O pin assignment after importing a synthesized netlist. Legal I/O pinouts are guaranteed only after the design has run through the ISE implementation tools, and after DRCs for I/O and clock placement are run without error.

Importing and Examining the CSV Format I/O Port List

1. In Windows Explorer, open the following I/O Ports CSV file:

   `<Extract_Dir>/PlanAhead_Tutorial/Sources/IO_Ports_import.csv`

2. Examine the I/O ports spreadsheet format and content, and exit without saving.
3. In the PlanAhead software environment, select **Import I/O Ports** from the Flow Navigator, located on the left side.

   Note: You may need to click the arrow on the left side of the PlanAhead environment to display the Flow Navigator.

4. Select the CSV File browser, and browse to select:

   `<Extract_Dir>/PlanAhead_Tutorial/Sources/IO_Ports_import.csv`

The Device and Package views display the assigned Ports, and the I/O Ports view is now populated with the imported I/O Ports. Notice that the mybus ports defined in an earlier step have been overwritten by the ports defined in the CSV file. If you are going to import a CSV file, do this before defining ports with the Create I/O Ports command.

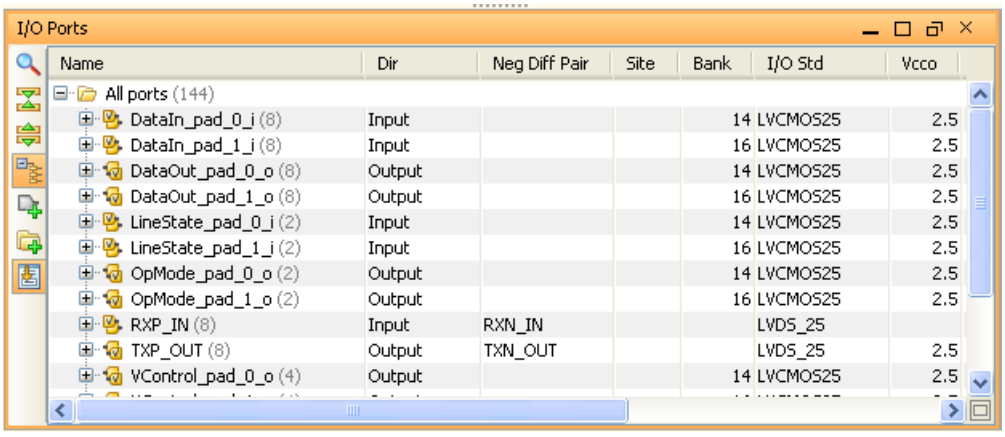

Figure 13: **I/O Bus Ports are Grouped by Bus**

The buses are grouped together and are expandable.

Step 7: Exporting the Device and I/O Pin Assignments

You can export the I/O Port assignments to UCF, CSV, VHDL or Verilog format files. This is useful for creating HDL headers and PCB schematic symbols.

The CSV format output file contains package information for all pins, which can be used to begin I/O Port assignments.

Exporting the I/O Ports List Using the Export I/O Ports Command

1. Select **File > Export > Export I/O Ports**.
2. Select **CSV** and **UCF** in the Specify Types to Generate. (See Figure 14.)

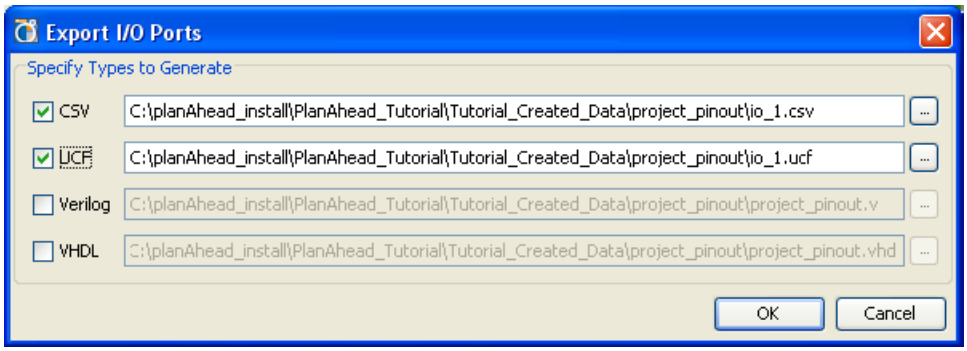

Figure 14: **Exporting I/O Ports to a CSV Spreadsheet and UCF File**

3. Click **OK** to accept the default file name and location.
4. Open a Windows Explorer window and browse to find and open the exported CSV file located in:

   `<Extract_Dir>/PlanAhead_Tutorial/Tutorial_Created_Data/project_pinout/io_1.csv`

5. Examine the exported I/O ports spreadsheet.

#Top: design_netlist_EMPTY Floorplan: io_1 Part: xc6vcx75tff784-1
#Generated by: brianj on: Wed Jan 12 19:12:52 2011
#Build: PlanAhead v13.1 by: hdbuild on: Wed Jan 12 09:12:30 PST 2011

IO Bank	Pin Number	IOB Alias	Site Type	Min Trace	Max Trace	Trace Leng	Prohibit	Interface	Signal Name	Direction	DiffPair Type	DiffPair Signal
14	V25	IOB_X0Y32	IO_L3N_14	49.602	57.869	8267			DataIn_pad_0_i[7]	IN		
14	W25	IOB_X0Y33	IO_L3P_14	56.874	66.353	9479			DataIn_pad_0_i[6]	IN		
14	U28	IOB_X0Y34	IO_L2N_14	57.912	67.564	9652			DataIn_pad_0_i[5]	IN		
14	V28	IOB_X0Y35	IO_L2P_14	66.642	77.749	11107			DataIn_pad_0_i[4]	IN		
14	U27	IOB_X0Y36	IO_L1N_14	52.968	61.796	8828			DataIn_pad_0_i[3]	IN		
14	T27	IOB_X0Y37	IO_L1P_14	51.204	59.738	8534			DataIn_pad_0_i[2]	IN		
14	R28	IOB_X0Y38	IO_L0N_14	50.226	58.597	8371			DataIn_pad_0_i[1]	IN		
14	R27	IOB_X0Y39	IO_L0P_14	48.678	56.791	8113			DataIn_pad_0_i[0]	IN		
14	Y24	IOB_X0Y24	IO_L7N_14	57.264	66.808	9544			DataOut_pad_0_o[7]	OUT		
14	Y25	IOB_X0Y25	IO_L7P_14	61.92	72.24	10320			DataOut_pad_0_o[6]	OUT		
14	Y27	IOB_X0Y26	IO_L6N_14	70.332	82.054	11722			DataOut_pad_0_o[5]	OUT		
14	W27	IOB_X0Y27	IO_L6P_14	65.628	76.566	10938			DataOut_pad_0_o[4]	OUT		
14	W28	IOB_X0Y28	IO_L5N_14	65.526	76.447	10921			DataOut_pad_0_o[3]	OUT		
14	Y28	IOB_X0Y29	IO_L5P_14	73.074	85.253	12179			DataOut_pad_0_o[2]	OUT		
14	V26	IOB_X0Y30	IO_L4N_VREF_14	48.12	56.14	8020			DataOut_pad_0_o[1]	OUT		
14	W26	IOB_X0Y31	IO_L4P_14	56.616	66.052	9436			DataOut_pad_0_o[0]	OUT		
14	P22	IOB_X0Y22	IO_L8N_SRCC_14	12.15	14.175	2025			LineState_pad_0_i[1]	IN		
14	P21	IOB_X0Y23	IO_L8P_SRCC_14	7.236	8.442	1206			LineState_pad_0_i[0]	IN		

Figure 15: **Examine Exported I/O Ports Spreadsheet**

If defined, the Interface group names are included in the spreadsheet. Printed circuit board designers can use this spreadsheet to create Interface-specific schematic symbols. Creating I/O Port Interfaces is covered in an upcoming step.

6. Close the `io_1.csv` file.

Exporting an IBIS Model

1. Select **File > Export > Export IBIS Model**.
2. Examine the options in the dialog box.

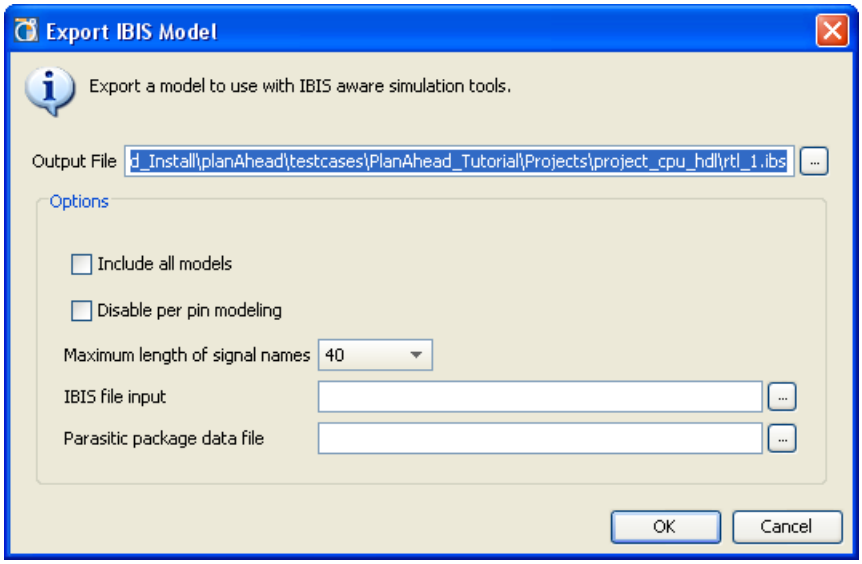

Figure 16: **Exporting an IBIS Model File**

3. Enter a file name.
4. Click **OK**.
5. Examine the output file.

Closing the I/O Pin Planning Project

1. Select **File > Close Project**.
2. If prompted to save, select **I/O Design – constr_1**.
3. Click **Save**.
4. Click **OK** in the Close Project dialog box.

Step 8: Analyzing I/O Port Placement

The I/O Planning features provide several ways to place the I/O ports onto either package pins or I/O die pads. The automatic placement command attempts to place all of the selected groups of I/O ports. It also attempts to adhere to I/O bank rules while grouping buses and Interfaces together.

For more control over I/O port placement, you can drag the selected I/O Ports into the Package or Device views interactively using one of the following semi-automatic placement modes:

- Place I/O Ports in an I/O Bank
- Place I/O Ports in an Area
- Place I/O Ports Sequentially

In addition, the I/O Planning features enables you to toggle DRCs on and off during I/O placement.

Opening the Synthesized Netlist-Based Project

1. Click the **Open Project** link in the Getting Started view, or select **File > Open Project**.
2. Browse to select the following project file:

   `<Extract_Dir>/PlanAhead_Tutorial/Projects/project_cpu_netlist/project_cpu_netlist.ppr`

   Alternately, select **Open Example Design > CPU (Synthesized)** from the Getting Started page.
3. In the Sources view, ensure that the `constr_1` Constraints folder is shown as *(active)*. If not, right-click on the `constr_1` folder, and select **Make Active**.
4. Select **Flow > Netlist Design** to open the synthesized design.

   Alternately, you can select **Netlist Design** in the Flow Navigator in the left side of the main window.
5. From the Design Analysis pulldown located in the main toolbar, select **I/O Planning**.

The I/O Planner view layout displays.

Splitting the Workspace to Display the Package and Device Views Simultaneously

The PlanAhead software graphical viewing area is called the Workspace. It can be split either horizontally or vertically to display multiple views simultaneously. This allows you to select I/O banks and Interfaces in order to see the physical package pin and internal die pad locations.

1. Click and drag the Package view tab to the right edge of the Workspace until the grey rectangle for the view appears as shown in Figure 17.

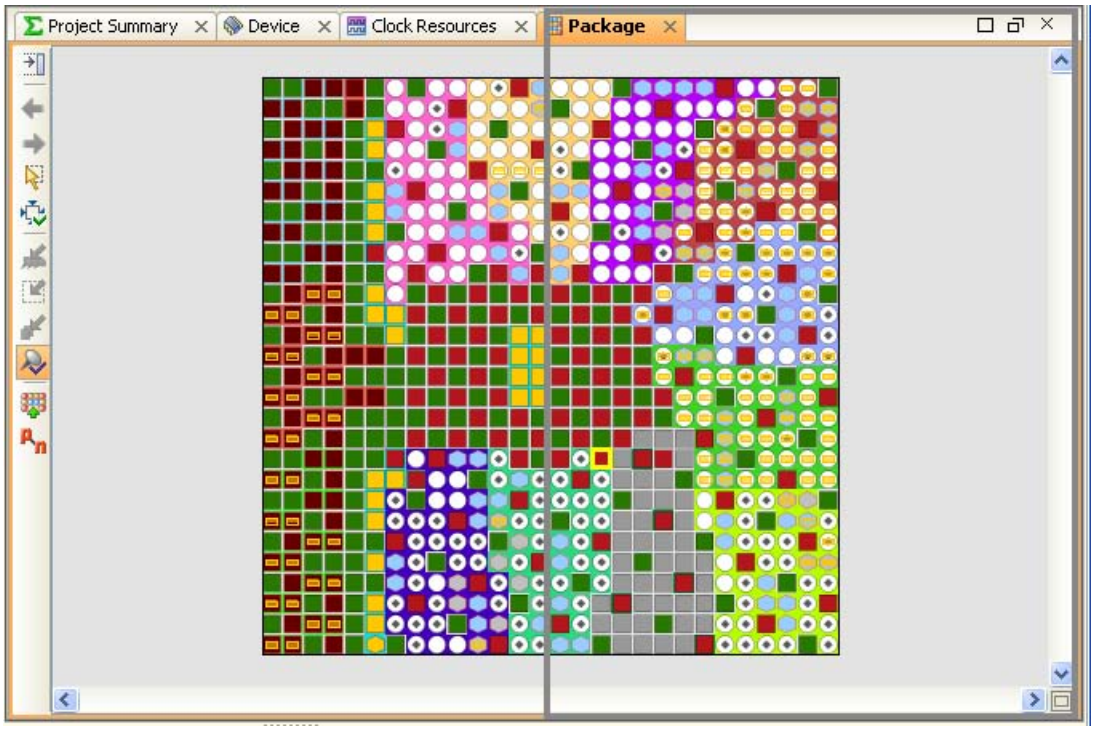

Figure 17: **Splitting the Workspace Viewing Area**

2. Drop the view in place.
3. If necessary, click the **Device** view tab to bring it to the front.
4. Adjust the Workspace size as needed.

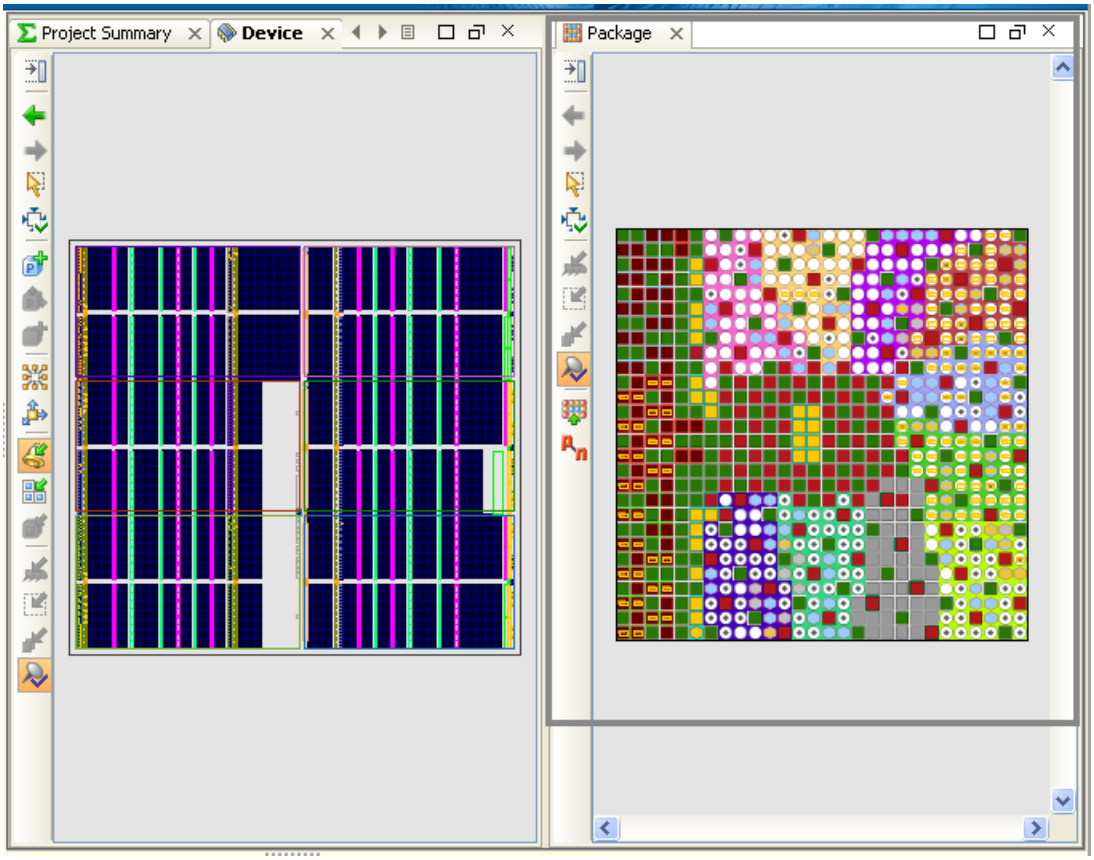

Figure 18: **Displaying the Package and Device Views Simultaneously**

Examining the I/O Ports in the Design

1. In the I/O Ports view banner, click the Maximize View button .
2. Click Expand All in the I/O Ports view.
3. Scroll down the list of buses and signals.

   The Neg Diff Pair fields are populated for some of the buses indicating that they are differential pair buses.
4. In the I/O Ports view, click to unselect Group by Interface and Bus .

   The I/O Ports now display as a flat list rather than grouped by bus.
5. Scroll down the list to display the I/O Standards (I/O Std) values.

I/O Ports

Id	Name	Dir	Interface	Neg Diff Pair	Site	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type
35	LineState_pad_0_i[1]	Input					LVCMOS25	2.500		12	SLOW
36	LineState_pad_1_i[0]	Input					LVCMOS25	2.500		12	SLOW
37	LineState_pad_1_i[1]	Input					LVCMOS25	2.500		12	SLOW
38	OpMode_pad_0_o[0]	Output					LVCMOS25	2.500		12	SLOW
39	OpMode_pad_0_o[1]	Output					LVCMOS25	2.500		12	SLOW
40	OpMode_pad_1_o[0]	Output					LVCMOS25	2.500		12	SLOW
41	OpMode_pad_1_o[1]	Output					LVCMOS25	2.500		12	SLOW
42	RXP_IN[0]	Input		RXN_IN[0]			LVDS_25				
43	RXP_IN[1]	Input		RXN_IN[1]			LVDS_25				
44	RXP_IN[2]	Input		RXN_IN[2]			LVDS_25				
45	RXP_IN[3]	Input		RXN_IN[3]			LVDS_25				
46	RXP_IN[4]	Input		RXN_IN[4]			LVDS_25				
47	RXP_IN[5]	Input		RXN_IN[5]			LVDS_25				
48	RXP_IN[6]	Input		RXN_IN[6]			LVDS_25				
49	RXP_IN[7]	Input		RXN_IN[7]			LVDS_25				
50	RxActive_pad_0_i	Input					LVCMOS25	2.500		12	SLOW
51	RxActive_pad_1_i	Input					LVCMOS25	2.500		12	SLOW
52	RxError_pad_0_i	Input					LVCMOS25	2.500		12	SLOW
53	RxError_pad_1_i	Input					LVCMOS25	2.500		12	SLOW
54	RxValid_pad_0_i	Input					LVCMOS25	2.500		12	SLOW
55	RxValid_pad_1_i	Input					LVCMOS25	2.500		12	SLOW
56	SuspendM_pad_0_o	Output					LVCMOS25	2.500		12	SLOW

Figure 19: **Examining I/O Standard and Diff Pair Requirements**

The RXP_IN, TXP_OUT, and TILE_REFCLK_PAD buses are differential pairs and have unique I/O Standards applied.

Step 9: Creating I/O Port Interfaces

It can be beneficial to group I/O Ports associated with various I/O interfaces. The I/O Planning layout enables you to define groups of pins, buses or other interfaces together as an "Interface." This ability helps with I/O Port management and with generating interface-specific PCB schematic symbols. It also forces the I/O Port automatic placement command to group the entire interface together on the device (where this is possible).

Creating Interfaces for Similar I/O Port Groups

The design used in this tutorial has two USB interfaces, each containing many I/O ports. The I/O port names are differentiated by _0 and _1. You will create Interfaces for all signals in USB0 and USB1.

1. Click the Show Search button  .
2. Type **_0** in the Search field.

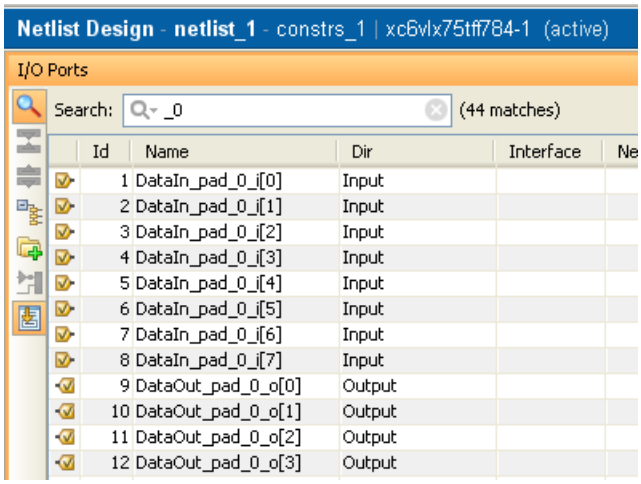

Figure 20: **Selecting USB_0 Related Ports**

3. Select one of the ports in the filtered list.

   Press **Ctrl+A** to select all ports in the filtered list.
4. Right-click and select **Create I/O Port Interface**.

   The Create I/O Port Interface dialog box opens.
5. Type **USB0** in the Name field.

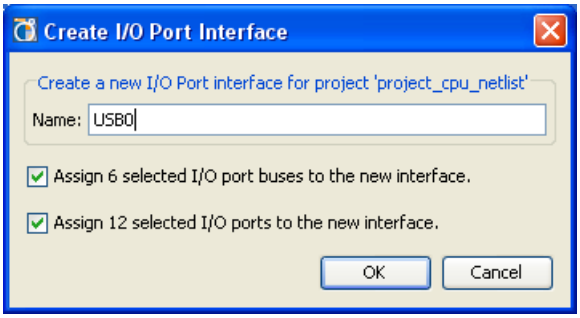

Figure 21: **Create I/O Port Interface**

6. Click **OK**.
7. In the Search field, change _0 to **_1** and follow the same steps to create a USB1 I/O Port Interface.
8. Click the Show Search button to remove the Search filter.
9. Click the Group by Interface and Bus button.
10. Click Collapse All.

    The I/O ports list is condensed with all of the USB related ports in Interface groups.
11. Expand the **Scalar ports** folder to view the clocks resets and other ports.
12. Click the Restore button in the view banner.

The I/O Ports view is restored to the original location.

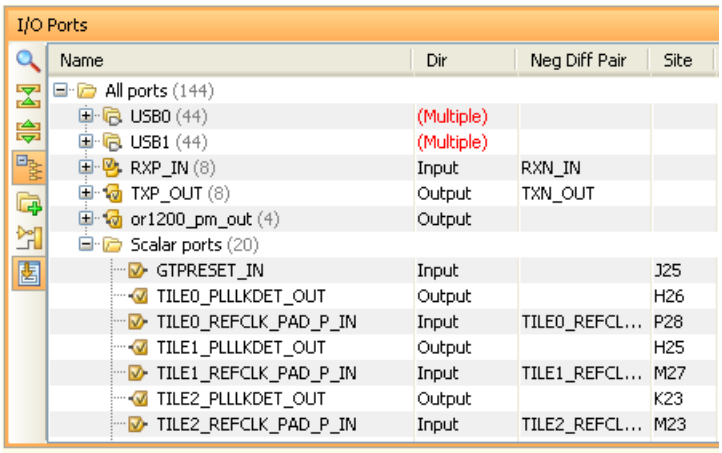

Figure 22: **Viewing I/O Port Interface Groups and Scalar Ports**

Step 10: Clearing Imported I/O Placement Constraints

The PlanAhead software has a robust set of options and filters for keeping or removing placement constraints. As I/Os are manually assigned, the placed I/O and clock logic are assigned fixed LOC placement constraints. The PlanAhead software differentiates between user-placed (fixed) and ISE implementation placed (unfixed) placement constraints. All fixed placements are included as LOC constraints in the UCF file exported for ISE implementation.

In order to walk through the steps involved in creating the pin assignment, you will first need to clear the existing I/O LOC constraints in this project.

Clearing Imported I/O Constraints Using the Clear Placement Constraints Command

1. Click the Unselect All button  .
2. Select **Tools > Floorplanning > Clear Placement**.

   The Clear Placement Constraints wizard opens.
3. Select **I/O port placement**.
4. Click **Next**.

   The Fixed Placement dialog box opens.

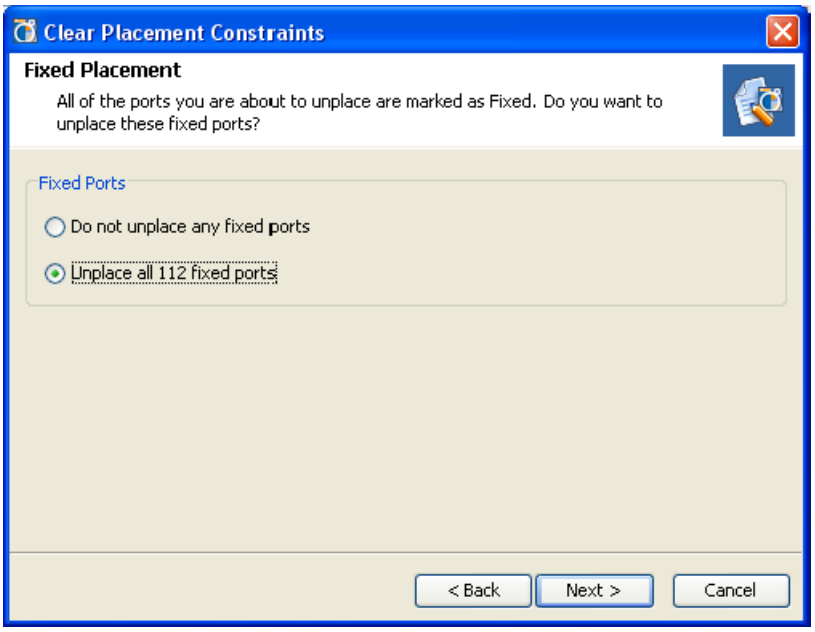

Figure 23: **Selecting Ports to Clear**

5. Select **Unplace all # fixed ports**. (The number may vary.)
6. Click **Next**.
7. Review the Summary dialog box.
8. Click **Finish**.

The placement constraints are now removed in the Package and I/O Ports views.

Step 11: Placing I/O Ports

The PlanAhead software provides several ways to place the I/O Ports onto either package pins or I/O die pads. The automatic placement command tries to place all of the selected group of I/O Ports, adhering to I/O bank rules while grouping buses and Interfaces together.

By default, the PlanAhead software uses interactive Design Rule Checks (DRCs) during I/O placement. To disable this check, in the Device and Package views, toggle the Automatically Enforce Legal I/O Placement button .

For more control over I/O port placement, you can drag the selected I/O Ports into the Package or Device views using one of the following semi-automatic placement modes:

- Place I/O Ports in an I/O Bank
- Place I/O Ports in an Area
- Place I/O Ports Sequentially

Placing the USB0 Port Interface

1. In the I/O Ports view, select the **USB0 Interface**.
2. In the Package view, click the Place I/O Ports in an I/O Bank button .
3. Click and drag the cursor over the Package view.

   As the cursor is dragged over the Package Pins, the assignment pattern displays and the number of pins to be placed is shown in the tooltip.

   The Information bar at the bottom of the PlanAhead software displays information about the objects being dragged over, including I/O Banks and Package Pins.

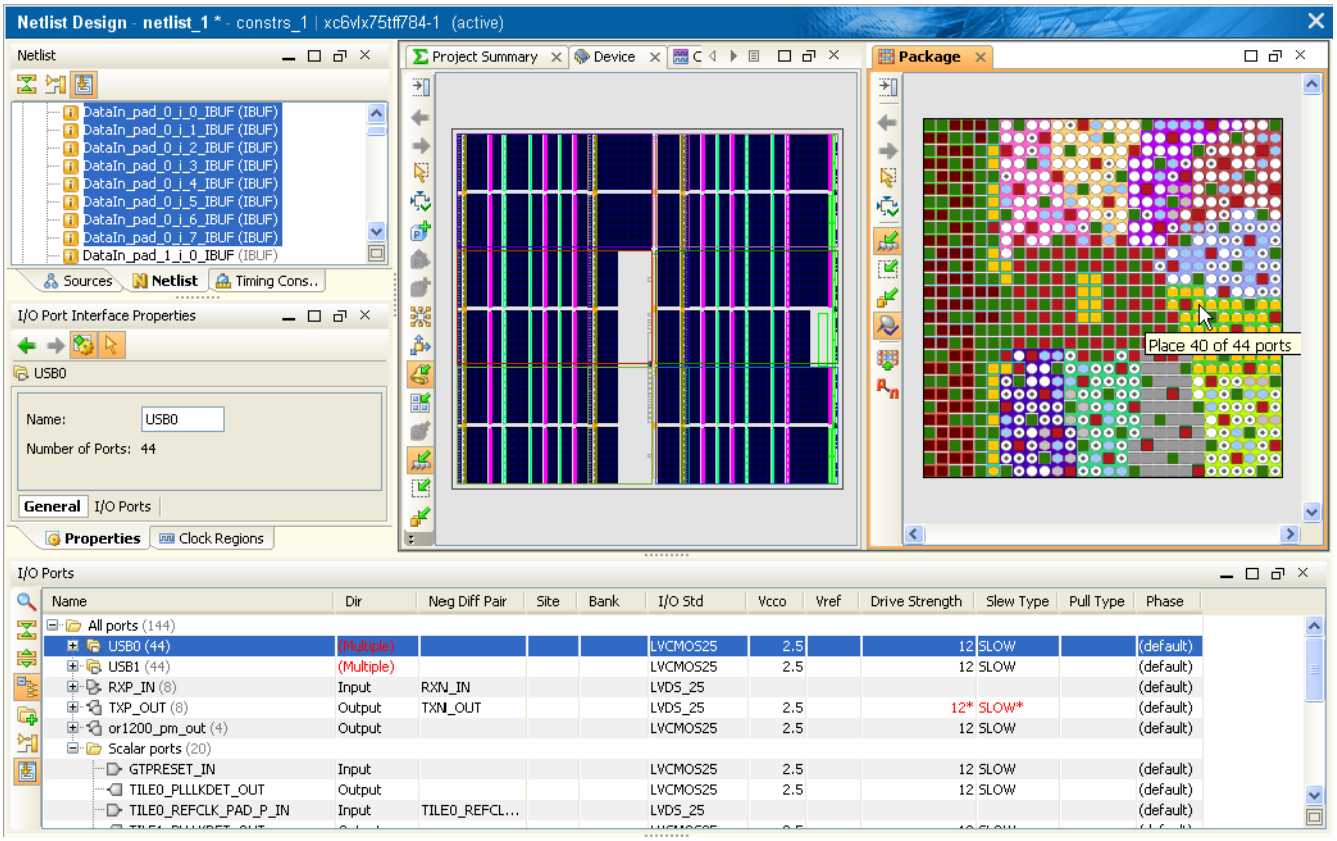

Figure 24: **Place I/O Ports in an I/O Bank**

4. Click **I/O Bank 14** on the right side of the package to drop the I/O Ports, as shown in Figure 24.

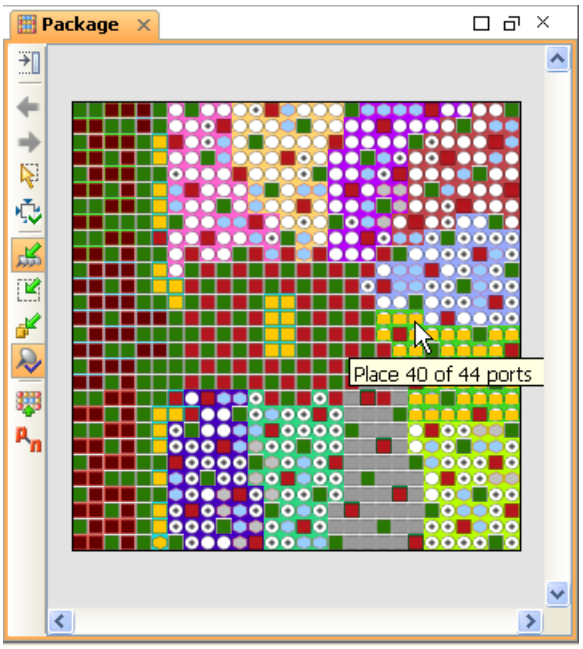

Figure 25: **Continuing to Place I/O Ports in I/O Banks**

The I/O Ports are assigned in the order in which they appear in the I/O Ports view. Assignment locations are vectored out from the initial pin selected.

5. Select **I/O Bank 24**, below and adjacent to I/O Bank 14, to place the remaining ports.
6. In the I/O Ports view, click the Collapse All button .

Placing the USB1 I/O Port Interface

1. In the Device view, zoom in to the upper left quadrant of the device.
2. In the I/O Ports view, select the **USB1 Interface**.
3. In the Device view, click the Place I/O Ports in an Area button .

   The cursor displays a cross indicating that you can draw a rectangle.
4. Draw a rectangle starting above the upper left I/O bank and drag it down and to the right until all I/O Ports are placed in the rectangle within the top clock region.

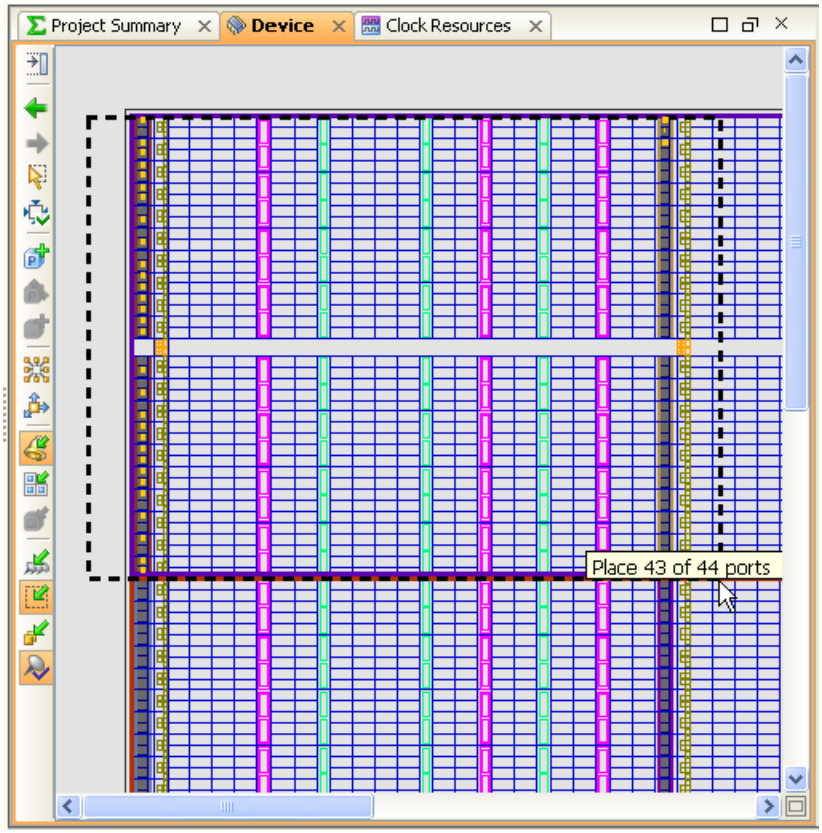

Figure 26: **Placing USB1 I/O Ports in an Area**

There is still one unplaced I/O clock port connected to the cursor. There is no global clock pad in this area of the device. Rather than trying to find a global clock pad, allow the automatic placement command to place it later.

5. Press **Esc** to exit the placement mode command.
6. In the I/O Ports view, click Collapse All .

Placing the RXP_IN Differential Pair Bus

1. In the Package view, toggle the Show Differential I/O pairs button .
2. Zoom in to an area in the bottom left of the Package view where you can see the square GT differential pair pins.
3. Zoom into the GT locations on the right side of the Device view (see Figure 26).
4. Select the **RXP_IN** bus in the I/O Ports view.
5. In the Package view, click Place I/O Ports Sequentially .
6. Drag and click to place the first diff pair I/O Port into one of the GT I/O Banks on a designated pin.

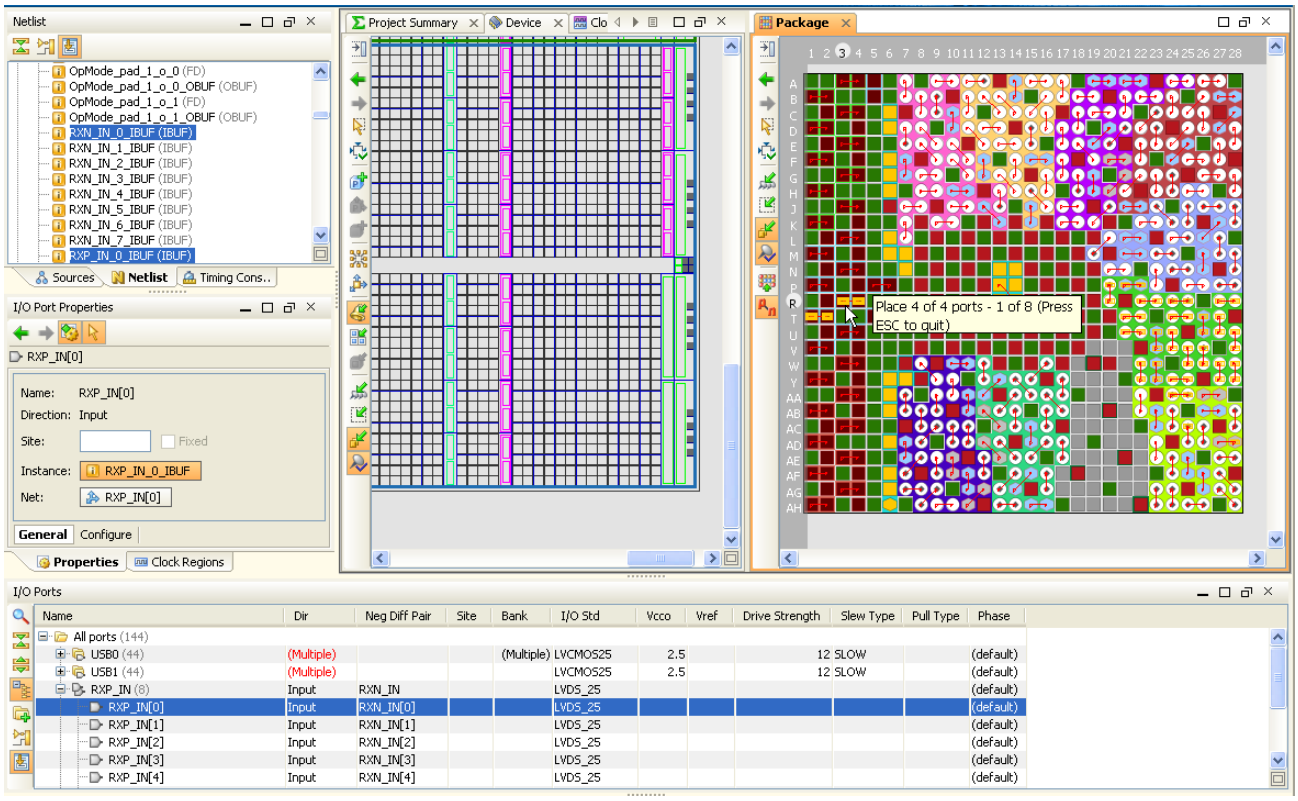

Figure 27: **Placing Diff Pair I/O Bus Ports Sequentially**

Both diff pairs associated with the GTs were placed on legal sites. You might see a tooltip indicating that the selected site is not legal and giving the reason why it is not legal.

You can manually enter a pin location in the Site field in the I/O Port Properties view.

After placing the diff pair pins, PlanAhead will queue up the next group of pins to place.

7. Select another pin in the Package view to place the next diff pair I/O bus port.
8. In the Device view, select one of the pins at the bottom of one of the GT I/O sites.

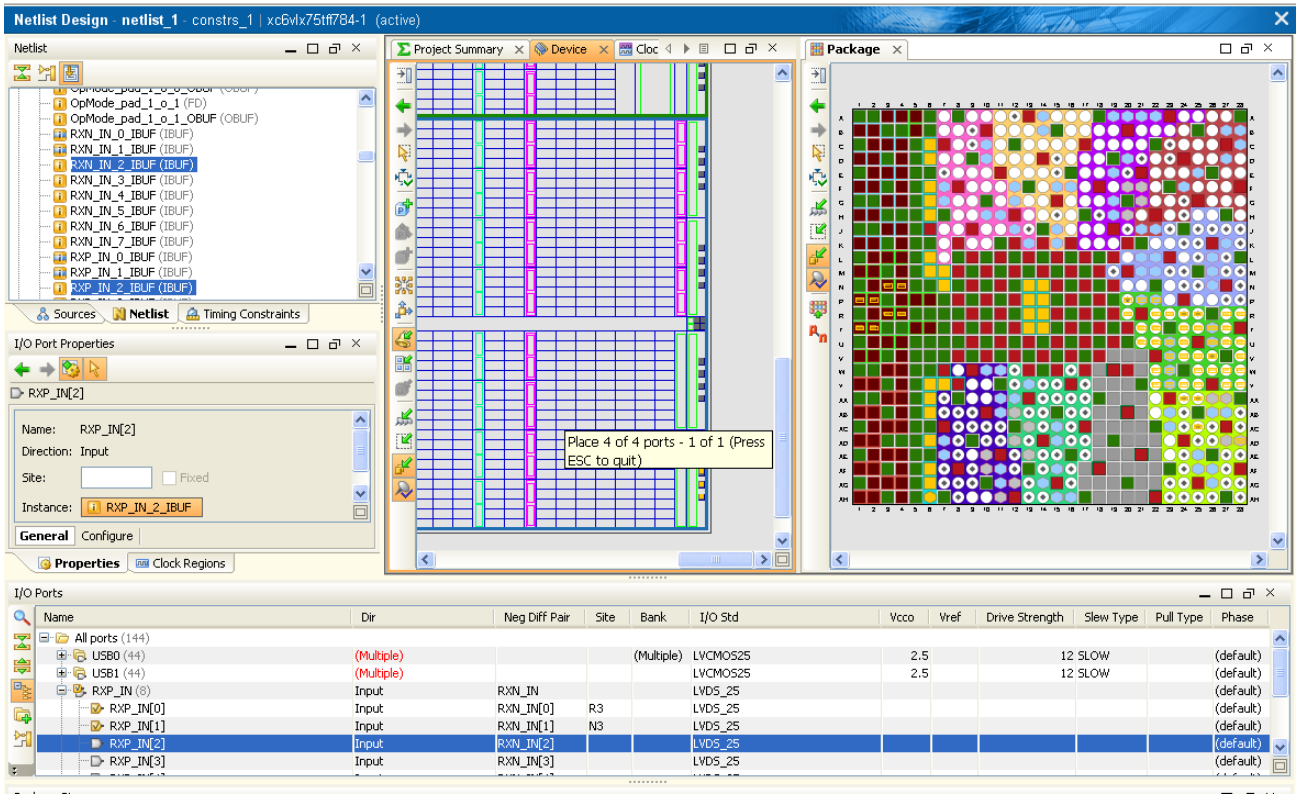

Figure 28: **Placing GT related I/Os Sequentially in the Device View**

9. Press **Esc** to exit the command.

   In the next steps, you will place the rest of the GTs and their related I/Os.

10. In the Package view, toggle Show Differential I/O pairs .
11. Zoom Fit the Package and Device views.

Removing the Split Workspace View for the Device and Package Views

Now that the I/O Ports are all placed, the Package view is no longer needed to share the Workspace view. The split view can be removed easily.

1. Select the **Package** view tab and drag it onto the Device view tab. The grey rectangle should surround the entire Device view.
2. Drop the Package view onto the Device view tab.
3. Select the **Device** view tab to bring it to the front.
4. Adjust the view size, and Zoom fit the view, if needed.

Step 12: Placing Gigabit Transceivers and Clock Logic

The PlanAhead software enables you to place critical clock or I/O related logic. After a synthesized netlist is imported, clocks and clock relationships can be explored and used to lock down these logic objects onto specific device sites. The PlanAhead software automatically groups some logic, such as GTs and their associated I/O pin pairs. This makes selection and placement of GTs and other related logic less prone to errors.

Searching for the Gigabit I/O and Global Clock Logic in the Design

1. Click the Find button or select **Edit > Find**.

   The Find dialog box opens.

2. Click **More** to add another Instance Type to include in the search.
3. Set the Criteria option for the new filter line to **OR**.
4. Adjust the selection filters to match Figure 29.

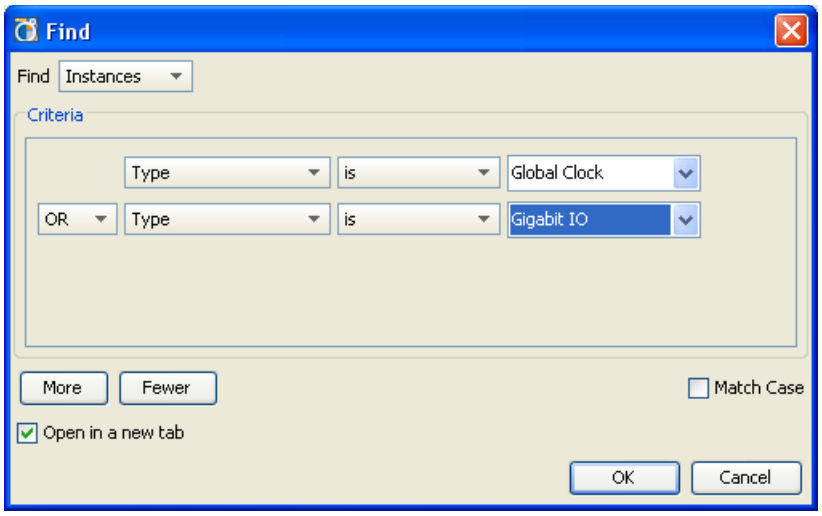

Figure 29: **Searching for Global Clocks and Gigabit I/Os**

5. Click **OK**.

   The Find Results view opens.

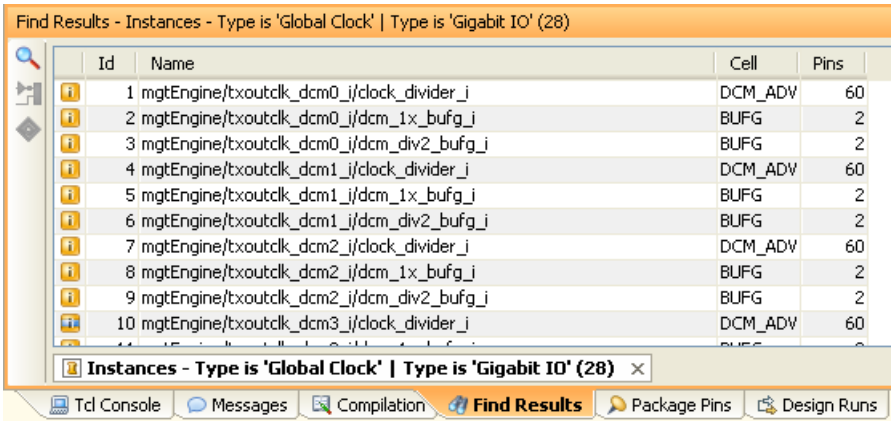

Figure 30: **Viewing the Global Clock and GTXE1 Objects**

6. Scroll down the list of objects, and observe the following:
   - BUFG
   - BUFGP
   - DCM_ADV
   - GTXE1

   The logic names include 0-3 numbers indicating that each DCM_ADV has two BUFGs associated with it.
7. Scroll to the bottom to observe GTXE1.

The objects that you already placed are displayed with a blue striped icon. The GTXE1 logic names are also numbered 0-3 to align with the DCM_ADVs and BUFGs.

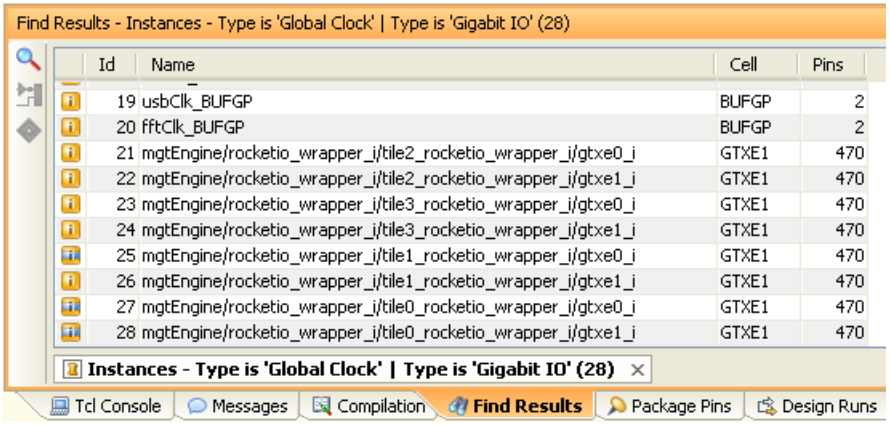

Figure 31: **Placed and Unplaced Icons**

In the next step, you will place these objects in proper relation to each other.

Using the Schematic to Trace Clock Logic

The Schematic view can be used to expand and explore any logic in the design. Placement constraints can be applied from the Schematic view.

1. In the Find Result view, select the first **DCM_ADV** cell that appears at the top of the list.

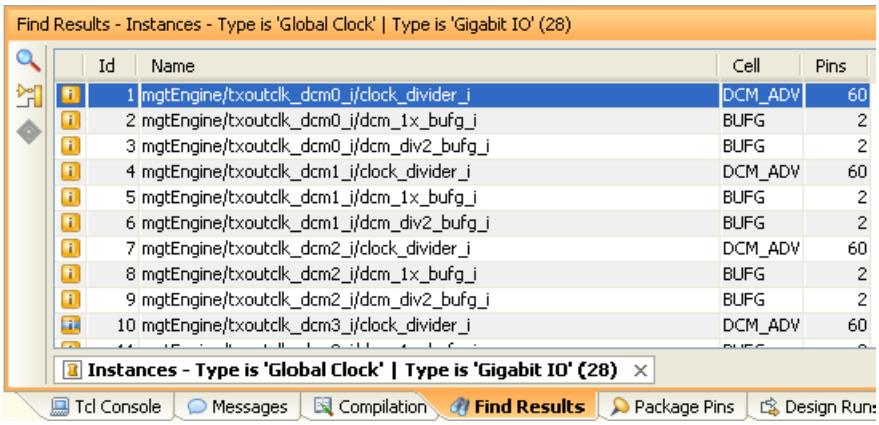

Figure 32: **Selecting Clock Logic to Trace in the Schematic**

2. In the Find Results view, click the Schematic button .
3. In the Schematic view, select Expand all logic outside selected the instance .
   Observe the logic connectivity of the two BUFGs.
4. Double-click the **CLK_IN** port on the `txoutclk_dcm0_1` module.
5. Zoom in to observe the logic connection to the GTX instance.

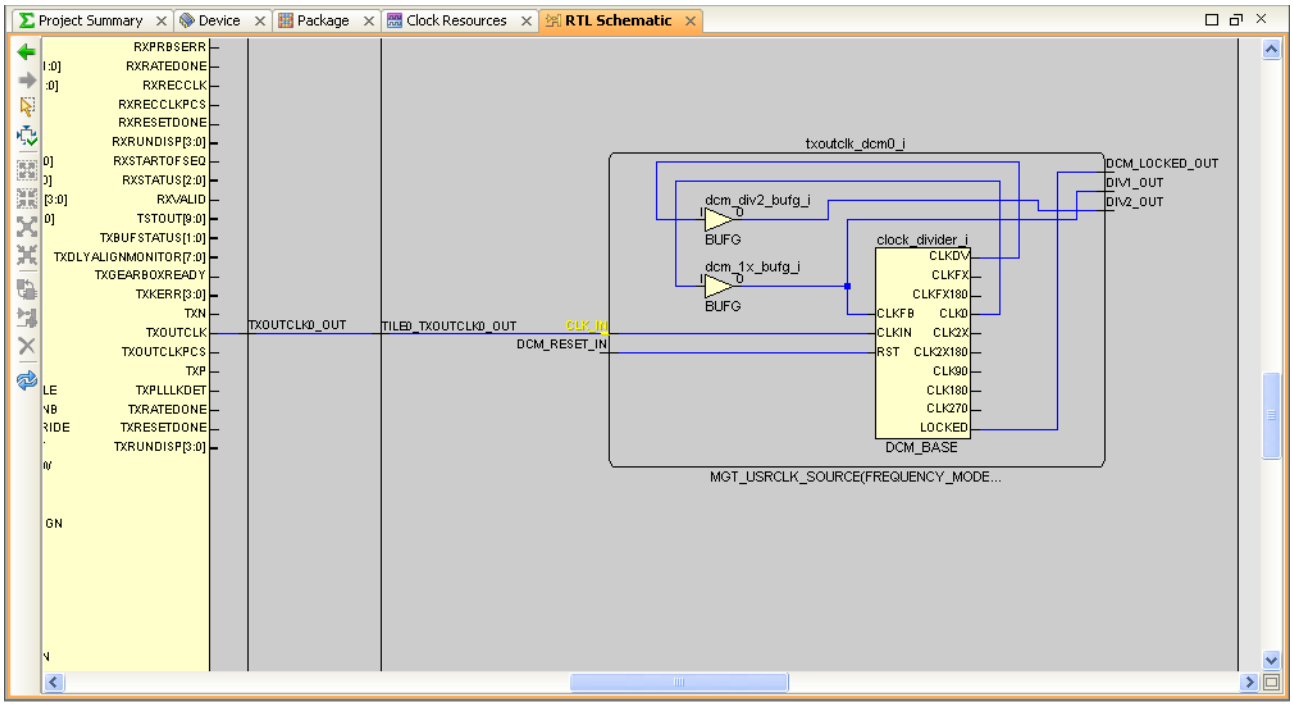

Figure 33: **Exploring Clock Logic Connectivity**

Logic is easily expanded and explored in the Schematic view. Select or highlight logic in the Schematic view to cross-select or highlights it in all other views.

6. Close the Schematic view tab.

Exploring the Clock Resources View

1. In the Workspace, select the **Clock Resources** view tab.
   If no view tab exists, select **Window > Clock Resources** to display the view.
2. Click the Maximize Workspace button in the view banner to display the view full screen.
3. On the left side of the PlanAhead window, select the Hide Navigator icon .
4. Scroll around and examine the Clock Resources view.

The Clock Regions, I/O Banks, and various device resources are displayed in their relative location as found on the device. The Clock Resources view and the Device view show a similar arrangement of device sites.

Sections of the Clock Resources view can be expanded and collapsed to hide or display the resources as needed. Logic that is placed is displayed under the Instance columns.

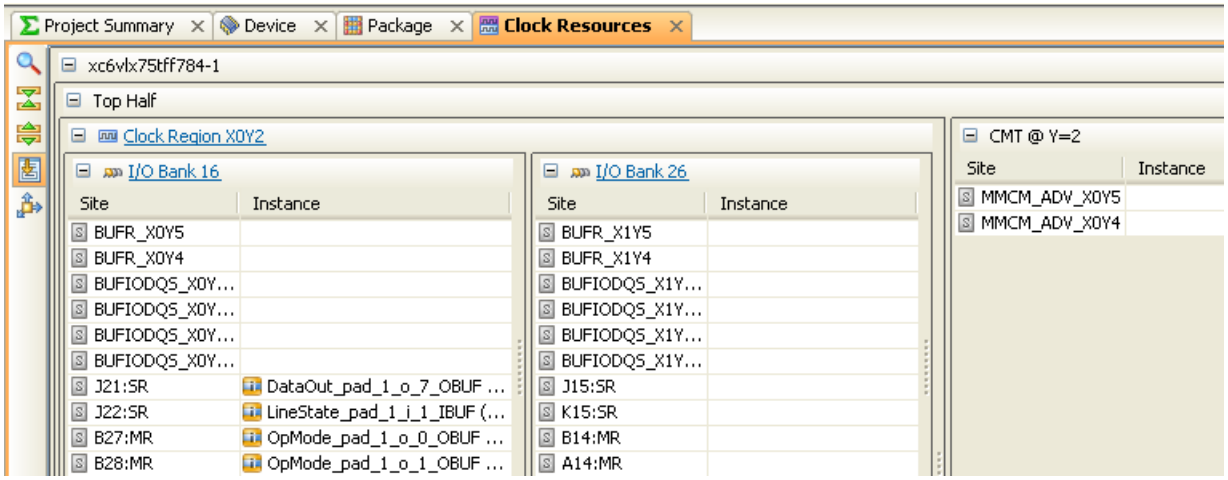

Figure 34: **Viewing Clock Resources in the Clock Resources View**

5. Locate one of the placed GTXE instances in the Clock Resources view.
6. Scroll and resize the view to show the entire section associated with the GTXE.

The corresponding I/O pairs are also placed in the GT Bank.

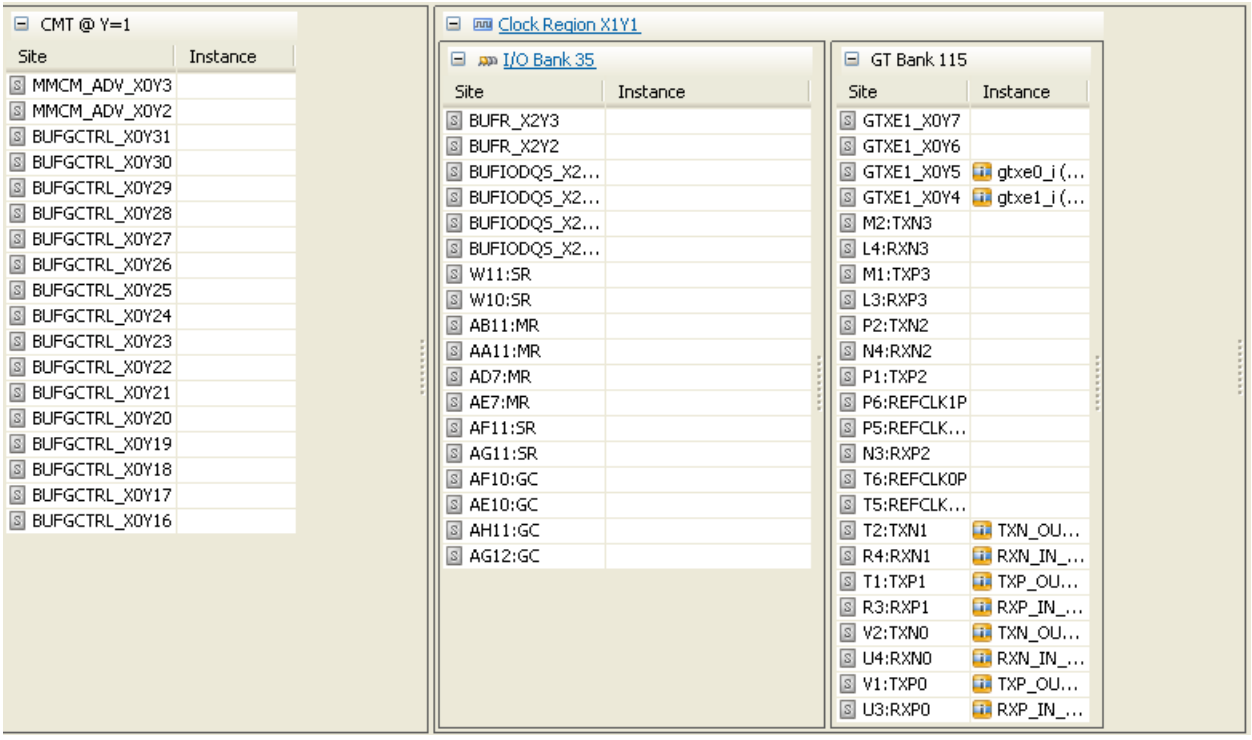

Figure 35: **Displaying GTXE1 Placement**

Placing the DCM_ADV and BUFGs Associated With the GTXE1 Instance

1. Click the **Find Results** view tab on the bottom of the screen to display the view.
2. Scroll to find the DCM_ADV and BUFGs that are associated with the GTXE1 instance that you selected. It has the same 0-3 logic names.
3. Select **DCM_ADV** and drag it into the Clock Resources view on the Instance field next to one of the MMCM_ADV_XXYY Sites in the same quadrant of the device.
4. Select one of the BUFGs and drag it into the Clock Resources view on the Instance field next to one of the BUFGCTRL_XXYY Sites.
5. Repeat the previous step for the remaining BUFG.

   Notice how easy it is to place clock and related I/O logic in the Clock Resources view.

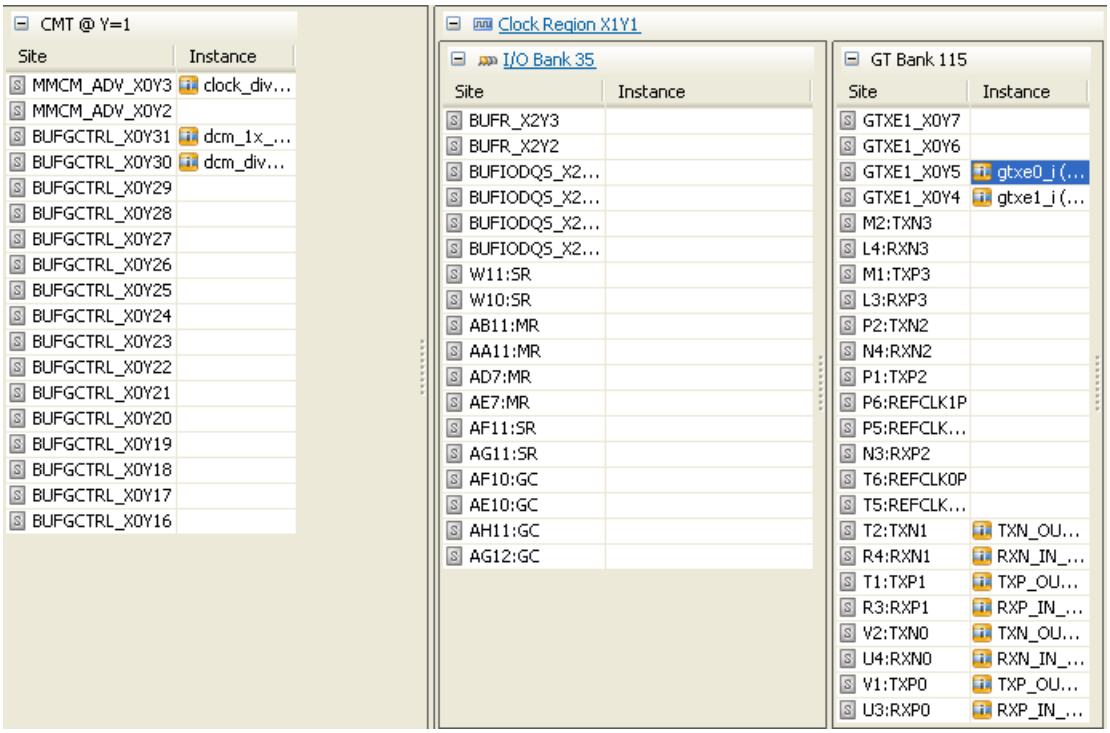

Figure 36: **Displaying Placed Clock Logic Relative to the GTXE**

6. Close the Find Results view.
7. In the Clock Resources view, click the Restore Workspace button in the view banner to return the view layout.
8. Select the Show Navigator button  on the left side of the PlanAhead software window to restore the Flow Navigator.
9. Click the **Device** view tab in the Workspace.

Placing the Remaining I/O Ports Automatically

1. If appropriate or necessary, click Unselect All  .
2. Select **Tools > I/O Planning > Auto-place I/O Ports**.
3. In the Autoplace I/O Ports dialog box, click **Next**.

The Placed I/O Ports dialog box opens.

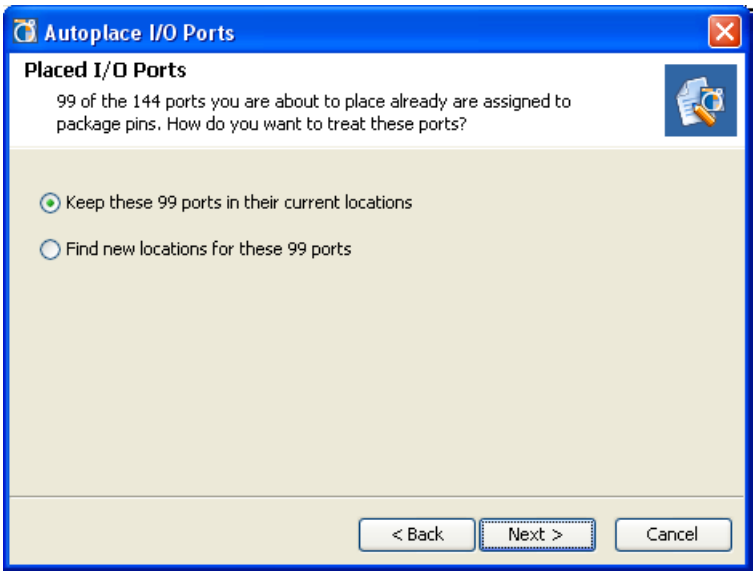

Figure 37: **Autoplacing I/O Ports Dialog Box**

If any I/O ports are selected when the command is run, only those I/O ports are auto placed.

4. Select **Keep these # ports in their current locations**. (The number of placed ports in your example design may vary from what is shown in the figure above.)
5. Click **Next**.
6. In the Summary dialog box, click **Finish**.

   The ports are placed.
7. Click **OK** in the placement confirmation dialog box.

Step 13: Running DRC and SSN Analysis

The PlanAhead software has an extensive set of I/O related DRC checks to be sure that I/O Ports are assigned accordingly. You can explore and resolve any violations interactively.

Running the I/O Related DRC Checks

1. Click **Run DRC** in the Flow Navigator.
2. Deselect the **Netlist**, **Floorplan**, **DSP48**, **RAMB16**, **RAMB** and **FIFO** rule categories.

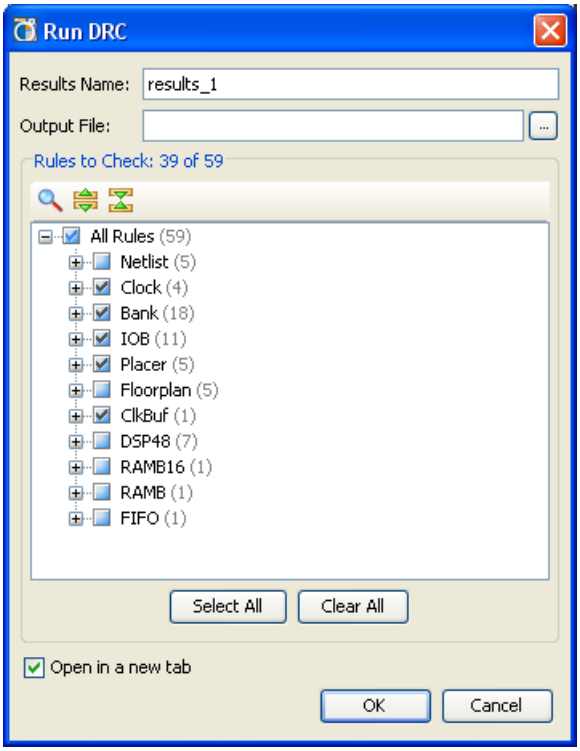

Figure 38: **Run I/O Related DRCs**

3. Expand the selected rules to examine the rule types.
4. Click **OK**.

   In this case, no violations are found. If your design reports violations, proceed regardless for purposes of this tutorial.
5. Click **OK** in the Run DRC confirmation dialog box.

Running the Run Noise Analysis Command to Check for Potential Signal Integrity

Simultaneous Switching Noise (SSN) Analysis can also be performed to help identify potential signal integrity concerns.

1. In the Flow Navigator, click **Run Noise Analysis**.
2. Click **OK** in the Run SSN Analysis dialog box.

   The SSN Results view opens.

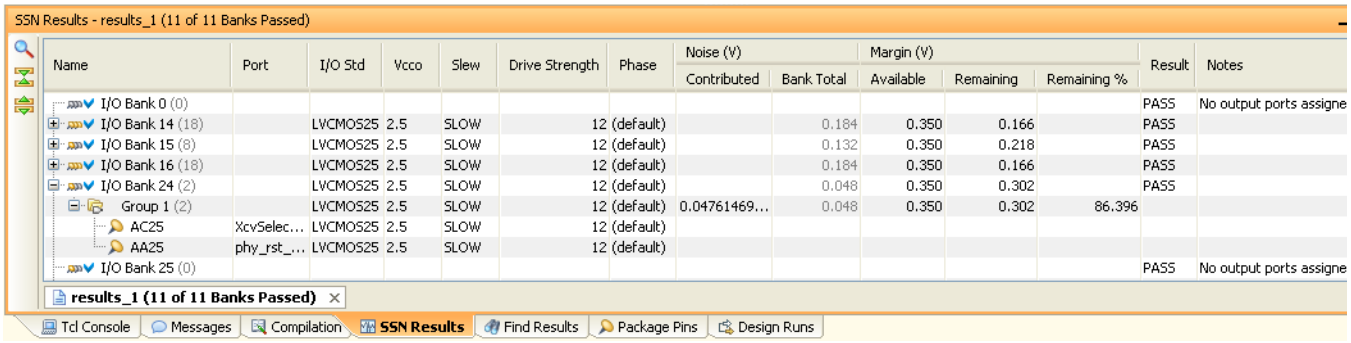

Figure 39: Examining the SSN Results View

3. Maximize the SNN Results View.
4. Scroll down and expand the list of I/O Banks.

View the Noise information in the report, including Contributed Noise for each group, Bank Total, Available and Remaining. The Status is PASS for all of the I/O Banks.

Closing the PlanAhead Software

1. Select **File > Exit**.
2. Click **OK**.

Conclusion

In this tutorial, you:

- Used the I/O pin planning environment to explore device resources and define alternate compatible devices for the design.
- Imported, created, and configured I/O Ports.
- Created Interfaces by grouping the related I/O Ports together.
- Used the semi-automatic placement modes to assign critical I/O Ports to package pins. Placement of the remaining I/O Ports was done using automatic placement.
- Exported and examined the I/O Ports list, which can be used for HDL header or PCB schematic symbol generation.
- Opened a netlist-based project and placed GTXE, DCM_ADV, and BUFG objects using logic connectivity as a guide for correct placement.
- Ran DRCs and Noise Analysis to validate legal I/O placement.

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Appendix A

Additional Resources

Xilinx Resources

- ***ISE Design Suite: Installation and Licensing Guide*** *(UG798)*: http://www.xilinx.com/support/documentation/sw_manuals/xilinx13_1/iil.pdf
- ***ISE Design Suite 13: Release Notes Guide*** *(UG631):* http://www.xilinx.com/support/documentation/sw_manuals/xilinx13_1/irn.pdf
- **Xilinx® Documentation**: http://www.xilinx.com/support/documentation.htm
- **Xilinx Global Glossary**: http://www.xilinx.com/support/documentation/sw_manuals/glossary.pdf
- **Xilinx Support**: http://www.xilinx.com/support.htm
- **Video Demonstrations**: http://www.xilinx.com/products/design_resources/design_tool/resources/index.htm

PlanAhead Documentation

- ***PlanAhead User Guide*** *(UG632)*: http://www.xilinx.com/support/documentation/sw_manuals/xilinx13_1/PlanAhead_UserGuide.pdf
- **PlanAhead Methodology Guides**: http://www.xilinx.com/support/documentation/dt_planahead_planahead13-1_userguides.htm
  - ***Pin Planning Methodology Guide*** *(UG792)*: http://www.xilinx.com/support/documentation/sw_manuals/xilinx13_1/ug792_pinplan.pdf
- **PlanAhead Tutorials:** http://www.xilinx.com/support/documentation/dt_planahead_planahead13-1_tutorials.htm