XPower Estimator User Guide

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/05/07	1.0	Initial Xilinx release.
05/04/09	2.0	Added information to describe the XPE spreadsheets for the 11.1 release of ISE.
06/24/09	3.0	Updated with information to describe the XPE spreadsheets for the 11.2 release of ISE, and added references to Spartan-6 and Virtex-6 FPGAs.
05/03/10	4.0	Updated with information to describe the XPE spreadsheets for the 12.1 release of ISE.
09/21/10	5.0	Updated with information to describe the XPE spreadsheets for the 12.3 release of ISE.
12/14/10	6.0	Updated with information to describe the XPE spreadsheets for the 12.4 release of ISE.
03/01/11	13.1	Updated with information to describe the XPE spreadsheets for the 13.1 release of ISE.
07/06/11	13.2	Revisions to manual for ISE 13.2 release: • Updated screen displays for all 7 Series figures. • In Using Named Cells section, updated all tables to include information on 7 series transceivers. • Added applicability to Defense-Grade FPGAs.

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Using XPower Estimator

Introduction

The XPower Estimator (XPE) spreadsheet is a power estimation tool typically used in the pre-design and pre-implementation phases of a project. XPE assists with architecture evaluation and device selection and helps in selecting the appropriate power supply and thermal management components which may be required for your application.

XPE considers your design's resource usage, toggle rates, I/O loading, and many other factors which it combines with the device models to calculate the estimated power distribution. The device models are extracted from measurements, simulation, and/or extrapolation.

The accuracy of XPE is dependent on two primary components:

- Inputs you enter into the tool
- Device data models integrated into the tool

For accurate estimates of your application, enter realistic information which is as complete as possible. Modeling a certain aspect of the design over conservatively or without sufficient knowledge of the design can result in unrealistic estimates. Some techniques to drive the XPE to provide worst-case estimates or typical estimates are discussed in this document.

XPE is a pre-implementation tool for use in the early stages of a design cycle or when the RTL description is incomplete. After implementation, the XPower Analyzer (XPA) tool (available in the ISE® Design Suite software) can be used for more accurate estimates and power analysis. For more information about XPA, see the XPower Analyzer Help.

XPE is a spreadsheet, so all Microsoft Excel functionality is fully retained in the writable or unprotected sections of the spreadsheet. XPE has additional functionality oriented to ease of use. The drop-down menus and the comment-enabled cells are helpful features to inform and guide you.

Getting Started with XPE

Opening XPE

1. XPE requires a licensed version of Microsoft Excel 2003 or Microsoft Excel 2007 to be installed.

   Microsoft Excel 2010 is not officially supported in this release of XPE. OpenOffice and Google Docs spreadsheet editors are not supported in this release of XPE.

2. Download the latest available spreadsheet for your targeted device. The XPE spreadsheets are available at the Power Solutions webpage here:

   http://www.xilinx.com/power

3. Make sure your Microsoft Excel settings allow macro executions. XPE uses several macros built into the XPE spreadsheet.

   - **Microsoft Excel 2003** - By default, the macro security level is set to High, which disables macros. To change the macro security level, follow these steps (actual menu names will vary with language of Microsoft Excel):

     a. On the Tools menu, point to **Macro** and click **Security**.

     b. In the Security dialog box, click the **Security Level** tab.

     c. Select **Medium**, then click **OK**.

     d. Open or, if already open, reopen the XPE spreadsheet.

     e. When prompted whether to enable or disable macros, click **Enable Macros**.

   - **Microsoft Excel 2007 or Windows Vista** - The following steps are required:

     a. From the Microsoft Office button select **Excel Options**.

     b. In the Options dialog, click on **Trust Center**.

     c. In the Trust Center dialog, click on **Trust Center Settings** and select the **Macro Security** tab.

     d. Select **Enable all macros**, then click **OK**.

     e. Open or, if already open, reopen the XPE spreadsheet.

     Note: You can save an Excel 2007 or later spreadsheet as an .xlsm file (Macro Enabled Workbook), and this will enable macro content. Calculations in XPE will not be affected if you decide to change to this extension. You can also enable the macro content each time you open the workbook. Enabling macro content by changing the Trust Center settings is a potentially dangerous way of enabling macro content.

     Note: If you save an Excel 2007 or later spreadsheet as an .xlsx file (Excel Workbook) you will lose the macro capability and render XPE nonfunctional. You will be warned of this if you try to save as an .xlsx file.

Minimum Required User Input

Power estimation for programmable devices like FPGAs is a complex process, since it is highly dependent on the amount of logic in the design and the configuration of that logic. To produce accurate estimates, the power estimation process requires accurate input values, such as resource utilization, clock rates, and toggle rates. To use this tool to its minimum capability with reasonable accuracy, you need the following:

- A target device-package combination
- A good estimate of resources you expect to use in the design (for example, flip-flops, look-up tables, I/Os, block RAMS, DCMs, etc.)
- The clock frequency or frequencies for the design
- An estimate of the data toggle rates for the design

As a general rule, input as much information about your design as available, then leave the remaining settings to default values. This strategy will allow you to determine the device power supply and heat dissipation requirements.

Tip: Use Excel formulas to link different cells together. For instance type '=CLOCK!E9' in the Logic sheet lines which list the resources driven by this clock domain.

XPE Calculations and Results

XPE uses your design and environmental input, then combines this information with the device data model to compute and present an estimated distribution of the power in the targeted device.

XPE presents multiple views of the power distribution.

- **Power by Voltage Supplies** - For each required voltage source, this information is useful to select and size power supply components such as regulators, etc. Supply power includes both off-chip and on-chip dissipated power.
- **Power by User Logic Resources** - For each type of user logic in the design, XPE reports the expected power. This allows you to experiment with architecture, resources, and implementation trade-off choices in order to remain within the allotted power budget.
- **Thermal Power** - XPE lets you enter device environment settings and reports thermal properties of the device for your application, such as the expected junction temperature. With this information you can evaluate the need for passive or active cooling for your design.

The **Summary** sheet in XPE shows the total power for the device. Other sheets show usage-based power. Leakage within the unused portion of the considered resource (if any) is not shown.

The following sections provide more details on how to enter settings and review results.

Definitions/Terminology

Supported Device Families

Separate spreadsheets are available depending on the targeted architecture. These spreadsheets are updated when new device data become available or when new features are added to XPE.

- 7 Series FPGAs
  - Artix™-7
  - Kintex™-7
  - Virtex®-7
- Virtex-6 and Virtex-5 – This spreadsheet includes all sub-families, including Virtex-6 Low Power, Virtex-6Q Defense-grade, Virtex-5Q Defense-grade, and Virtex-5QV Space-grade
- Virtex-4
- Spartan®-6 and Spartan-3A – This spreadsheet includes all sub-families, including Spartan-6 Lower Power, Spartan-6 Automotive, Spartan-6Q Defense-grade, Spartan-3AN, and Spartan-3A DSP
- Spartan-3E
- Spartan-3

Note: Download the latest available spreadsheet from http://www.xilinx.com/power.

Note: Pre-design power estimation for CPLD and other architectures is described in the Power Solutions webpage on the Xilinx website (http://www.xilinx.com/power).

Device Model Accuracy

The accuracy of the characterization data existing in the tool is reflected by accuracy designations in the **Characterization** field on the **Summary** sheet of XPE. For most FPGAs, the history of the accuracy designation is also displayed in the **Release** sheet. The accuracy designations are Advance, Preliminary, and Production.

Advance

The data integrated into XPE with this designation is based primarily on measurements and characterization data made on early production devices. A set of widely used device resources are included in the characterization. Characterization data is limited to these few blocks. This data is typically available within a year of product launch. Although the data with this designation is considered relatively stable and conservative, some under-reporting or over-reporting may occur. Advance data accuracy is considered lower than the Preliminary and Production data.

Preliminary

The data integrated into XPE with this designation is based on complete early production silicon. Almost all the blocks in the device fabric are characterized. Data for most of the dedicated blocks like TEMAC and PCIe block are also characterized and integrated into XPE. The probability of accurate power reporting is improved compared to Advance data.

Production

The data integrated into XPE with this designation is released after enough production silicon of a particular device family member has been characterized to provide full power correlation over numerous production lots. Characterization data for all blocks in the device fabric is included.

Total Power

The total FPGA power is calculated as follows:

Total FPGA power = Device Static + Design Static + Design Dynamic

The power estimates are modeled to account for temperature and voltage sensitivity. Ambient temperature and regulated voltage on the system can be keyed into the appropriate cells provided for that purpose.

Device Static Power

Also referred to as Leakage. Device static represents the transistor leakage power when the device is powered and not configured.

Design Static Power

Design static represents the additional power consumption when the device is configured and there is no switching activity. It includes static power in I/O DCI terminations, clock managers, etc.

Design Dynamic Power

Design dynamic represents the additional average power consumption from the user logic utilization and switching activity.

Activity Rates

XPE shows values for these types of activity rates:

- Toggle Rates
- Signal Rates

Toggle Rates

Providing accurate toggle rates in the various XPE sheets is essential to get quality power estimates. This information, however, may not be readily available at the stage in the design cycle where you enter data in XPE. Activity may be refined as the design gets more defined. Below are guidelines you can follow to help you enter design toggle activity.

- For synchronous paths, toggle rate reflects how often an output changes relative to a given clock input and can be modeled as a percentage between 0–100%. The max data toggle rate of 100% means that the output toggles every active clock edge. For instance, consider a free running binary counter with a 100MHz clock. For the Least Significant Bit you would enter 100% in the **Toggle Rate** column since this bit toggles every rising edge of the clock. For the second bit you would enter 50% since this bit toggles every other rising edge of the clock.
- For non-periodic or event-driven state machine designs, toggle rates cannot be easily predicted. An effective method of estimating average toggle rates for a given design is

to segregate the different sections of the design based on their functionality and estimate the toggle rates for each of the sub-blocks. An average toggle rate can then be arrived at by calculating the average for the entire design. Most logic-intensive designs work at around 12.5% average toggle rate, which is the default toggle rate setting in XPE. For a worst- case estimate, a toggle rate of 20% can be used. Average toggle rates greater than 20% are not very common. Arithmetic-intensive modules of a design seem to take toggle rates of up to 50%, which is representative of the absolute worst case.

Important: In all the sheets which do not have a dedicated **Clock Enable** column make sure you scale the toggle rate to account for any signal which gates this logic. For example, if the data toggle rate is modeled at 50% but the synchronizing clock is enabled 50 percent of the time, the resulting toggle rate should be 25% (50% x 50%).

Important: To appreciate what 100% toggle rate means, think of a constantly enabled toggle flip-flop (TFF) whose data input is tied High. The T-output of this flip-flop toggles every clock edge. Very few designs could possibly have an average toggle rate that high (100%).

Note: The IO sheet has a column to specify signal **Data Rate**. Make sure you adjust the **Toggle Rate** and **Data Rate** columns accurately. For example, on an input signal which toggles on both edges of the clock you would enter **Toggle Rate** = **100%** and **Data Rate** = **DDR** (Dual Data Rate).

Signal Rates

Signal rate defines the number of millions of transitions per second for the element considered. This is a read-only column that appears on some of the XPE sheets (for example, the Logic, I/O, DSP, and Block RAM sheets). The general equation to calculate signal rate is:

Signal Rate (Mtr/s) = Clock Frequency (Mhz) * Effective Toggle Rate (%)

Fanout

Fanout defined in XPE is similar to the fanout reported by the synthesis tool and can differ from the fanout reported by the implementation tool. This difference is expected because fanout will vary with placement and packing of the logic.

- In XPE fanout represents the number of individual loads or logic elements the considered element is connected to (LUTs, flip-flops, block RAM, I/O flip-flops, distributed RAM, and shift registers).
- In the implementation tool (ISE PAR Report), fanout is the number of SLICEs the considered net is routed to. A SLICE typically contains multiple logic elements and users generally do not control packing of the different elements into SLICEs. XPE algorithms will estimate this packing before calculating the power.

Effective ΘJA (C/W)

This coefficient defines how power is dissipated from the FPGA to the environment (device junction to ambient air). Typically this option is calculated by XPE, taking into account, among other things, the different environment parameters in the **Settings** panel of the **Summary** sheet. Entering a value in this field will override XPE calculations. Use this option if you have calculated this parameter by simulations. You may also want to use this feature to factor out environmental parameters when analyzing power differences with another spreadsheet in which environment settings have been set differently.

ΘSA (C/W)

Heatsink to ambient air thermal resistance. By default XPE obtains this value from a representative selection of heatsink data matched to the device package, combined with the **Heat Sink** value you set (**Low Profile**, **Medium Profile**, or **High Profile**) and the **Airflow** value you set. The value used by XPE is shown in the Θ**SA** field on the **Summary** sheet.

If you have the ΘSA information for your system you can enter your specific value. First set the **Heat Sink** drop-down menu on the **Summary** sheet to **Custom**, then enter your Θ**SA** value.

ΘJB (C/W)

Device junction to board thermal resistance. By default XPE estimates the junction to board thermal resistance based on standard JEDEC four-layer measurements. If you have done thermal simulations of your system you can enter your own specific value. First set the **Board Selection** drop-down menu on the **Summary** sheet to **Custom**, then enter your Θ**JB** value.

Junction Temperature (°C)

This field forces the value of the device junction temperature. XPE then adjusts the ambient temperature to meet the specified junction temperature. This option could be used when you need to work backward from a known or assumed worst case junction temperature and define the environment that would ensure this temperature is not exceeded.

User Interface

XPE has these spreadsheet sheets:

- The **Summary** sheet lets you enter and edit all device and environment settings. This sheet also displays a summary of the power distribution and provides buttons to import data into XPE, export results, and globally adjust settings.
- Other sheets allow you to enter usage and activity details for the different resource types available in the targeted device (for example, IO, Block RAM (BRAM), and Multi-Gigabit Transceivers (MGTs)). These sheets report design power based on the resource usage. Resource leakage power is shown on the **Summary** sheet.

Tip: XPE is intended to be intuitive to the novice spreadsheet-user. For information about a cell in the spreadsheet, move the mouse over the comment indicators (red triangle at the top right corner of the title cells) to read the relevant notes for the intended use (see Figure 1).

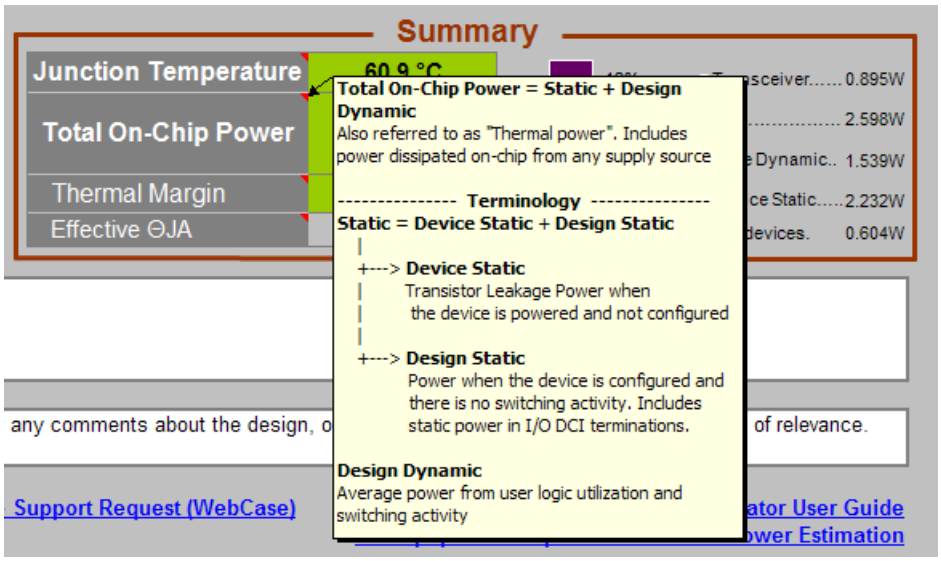

Figure 1: **Comment Indicators and Comment**

The XPE Toolbar

To make data entry into the tool easier, XPE supports importing data from different sources and allows settings to be changed globally. The toolbar is shown in Figure 2.

Note: The toolbar displayed below is the toolbar for the 7 series XPE spreadsheet. Toolbar buttons for earlier architecture spreadsheets may have different names than the names displayed below.

Figure 2: **XPE Toolbar (7 Series)**

Import File

Depending on what stage your design is in the FPGA development cycle, use this dialog box to import design information and activity into the spreadsheet. In the dialog box, select the **Files of type** field to determine whether you will import an .xls, .mrp or .xpe file.

For a description of the import feature, see Importing Data into XPE, page 17.

Export File

The **Export File** button lets you export the following information from the current spreadsheet:

- The current settings for your design within XPE. These settings can be imported into an XPower Analyzer session within ISE.
- A text power report, which allows you to analyze the power information in the XPE spreadsheet in a textual format.

For a description of the export feature, see Exporting XPE Results, page 19.

Reset to Defaults

The **Reset to Defaults** button resets all user settings to their default values, except for values in the **Device** selection table on the **Summary** sheet, and deletes all user entered values on the block details sheets (Clock, Logic, etc.).

Set Default Rates

This button opens up a dialog box which lets you change the default frequency, toggle rates or enable rates for the entire design or for specific sheets (see Figure 3).

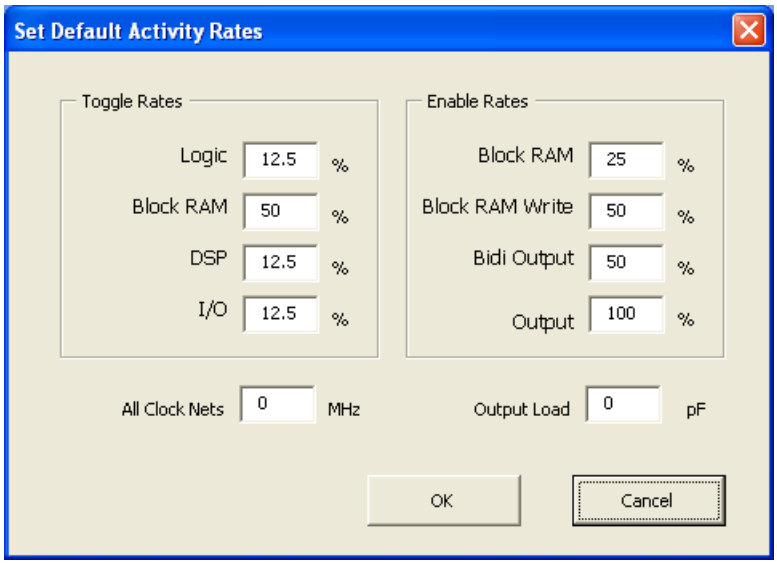

Figure 3: **Set Default Activity Rates Dialog Box**

The fields in the dialog box are:

- **Toggle Rates**

  Each field changes activity of the related sheet only. Acceptable range: 0 to 100%.

  To learn more about toggle rates, refer to the **Toggle Rates** section.

- **Enable Rates**

  Each field changes activity of the related sheet only. Acceptable range: 0 to 100%.

- **All Clock Nets**

  The clock frequency entered here applies to CLOCK, LOGIC, IO, BRAM and DSP sheets. Acceptable range: 0 to 500MHz.

- **Output Load**

  The equivalent capacitance seen by the output driver for the routing and components connected to this board trace. This setting does not affect power calculations for inputs.

XPE Cell Color-Coding Scheme

To simplify data entry and review, the XPE cells are color coded. A color **Legend** appears at the bottom of the **Summary** sheet (see Figure 3).

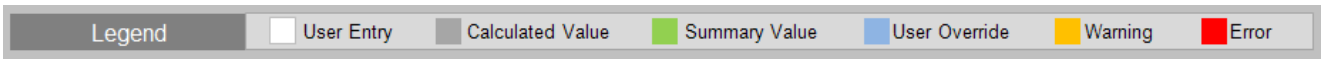

Figure 4: **Color Legend (Summary Sheet)**

A description of the spreadsheet's color-coding scheme is provided in Table 1.

Table 1: **XPE Cell Color-Coding Scheme**

Cell Color	Cell Use	Available User Action
White	Allows user to enter data	Editable
Grey	Displays a calculated value	Read-only
Green	Displays a summary value	Read-only
Blue	User override of cells normally calculated by XPE	Editable
Orange	Flags a warning. Indicates that a resource is not available.	Editable
Red	Flags an error. Examples of errors are: • A resource limit in the device has been exceeded. • The limits of a device specification (for example, junction temperature) have been exceeded.	Read-only. Edit other cells to correct the error.

Exchanging Power Information with XPower Analyzer

To determine device power supply requirements and estimate thermal dissipation throughout the design process, data exchange mechanisms are available between the different power estimation tools, XPower Estimator (XPE) and XPower Analyzer (XPA). Details on the methodology and user flow are presented in the *Power Methodology Guide* (UG786). This data exchange mechanism is available for the Spartan-6, Virtex-6, Kintex-7 and Virtex-7 families.

- Export settings to XPower Analyzer

  In a typical development process you will first perform power estimation in XPE to size the voltage supply sources, evaluate thermal power dissipation paths, and allocate the total power budget to the different blocks in the FPGA system. Later in the development cycle you will want to perform post implementation power analysis in XPower Analyzer to validate against your power and thermal goals. Instead of manually re-entering this environmental data into XPA you can export to a file and have XPA read it for your next analysis. This process exports all environment, thermal, and voltage settings which in turn helps getting realistic power estimations in XPA that can easily be compared between the two tools.

  For step-by-step export instructions, see Exporting XPE Results.

- Import results from XPower Analyzer

  This flow is useful in the following cases

  - The reported power exceeds your requirements and you want to evaluate different scenarios, adjusting resources used, count, and configuration. You can also estimate power gains from techniques such as logic gating or resource time sharing, without modifying your code.
  - Your project uses (or reuses) IP blocks already implemented in a previous design or acquired. You can import these existing blocks into XPE to quickly get resource and power usage for these blocks. You can then focus your efforts in XPE to enter data for the new pieces of logic not yet defined.
  - Team-based design – A project manager can regularly monitor power for the entire design by integrating resource usage and power consumption for modules developed by the different teams.

  For step-by-step import instructions, see Importing Data into XPE.

Data Import and Export

Depending on the stage in the FPGA development cycle your design is in, XPE provides multiple mechanisms to simplify data entry and manage output data.

Importing Data into XPE

In the **Summary** sheet, click the **Import...** button to open the dialog box shown in Figure 5. This dialog box varies slightly depending on device architecture, as newer family spreadsheets offer more import capabilities.

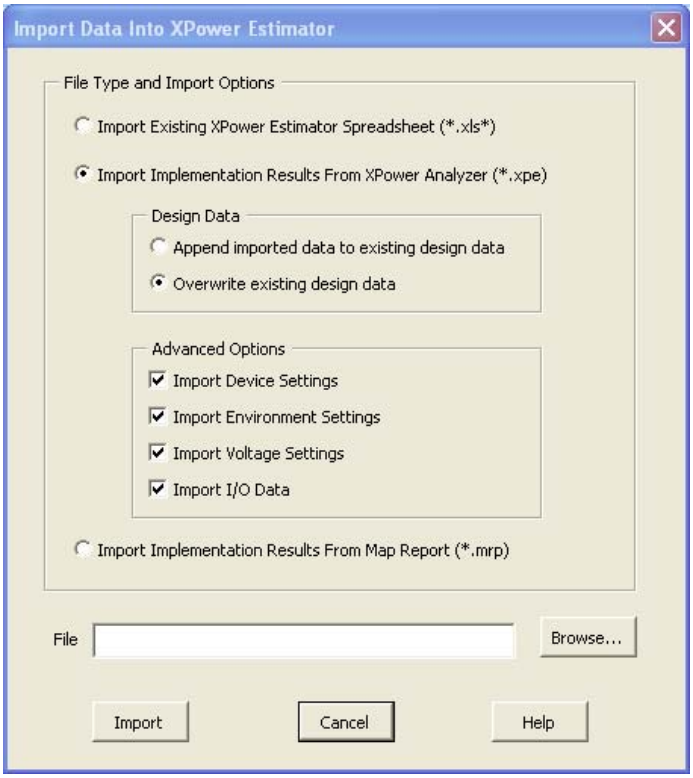

Figure 5: **Import Dialog Box (Virtex-7)**

This dialog box lets you select among the following import options:

- **Import Existing XPower Estimator Spreadsheet (*.xls*)**

  Use this option to import an existing XPE workbook (.xls or .xlsm file). This option is useful when starting a new design which reuses previous IP blocks or when updating the design information into the latest spreadsheet version. This action deletes all data in the current spreadsheet, then imports all data from the selected spreadsheet.

  Note: When the import is complete, make sure to verify and adjust the imported data where appropriate. For example, adjust utilization and resources count columns when porting a design to a new architecture.

- **Import Implementation Results From XPower Analyzer (*.xpe)**

  Use this option to further analyze your design by importing complete designs or IP blocks. Benefits and use model for this flow are presented in the Exchanging Power Information with XPower Analyzer section.

  To import this data into the spreadsheet:

  1. In the Summary sheet of the XPE spreadsheet, click **Import...**.
  2. In the import dialog box, browse and select the `.xpe` file to import.

     Note: Refer to the XPower Analyzer Help or the description of **`-xpe`** option to the **`xpwr`** command line in the *Command Line Tools User Guide (UG628)* for details on how to generate this interoperability file.
  3. (Optional. Newer devices only) In the **Design Data** section of the dialog box, select whether you want the imported data to override any previously entered data in the spreadsheet or rather append to the existing results
  4. (Optional. Newer devices only) In the **Advanced Options** section of the dialog box, Specify data to include during the import (environment settings, I/O details, Voltage level and Device selection)

- **Import Implementation Results From Map Report (*.mrp)**

  Select the import from Map Report (.mrp file) when portions of the design have been implemented in ISE. You can import the exact resource count from a Map Report to get a more accurate power estimation after the design is placed. This flow is also used when portions of the design are implemented while others are still being designed, so you can add details for the expected remaining logic and evaluate the total design power distribution.

  Note: This process overwrites any utilization data, but preserves environment settings.

  Note: After import you will notice resources used are grouped into a minimum set of lines. The map report only contains the counts of the various blocks and you will need to set the bit width, data rate, mode, enable, and other configurations on each XPE sheet to match your design.

  Note: The I/O and BRAM sheets are populated based on unique configuration. I/Os are grouped by bus and all BRAMs with the same configuration appear on a single line. You may therefore need to add additional rows and adjust the counts to group by clock domain, module, or functionality.

Exporting XPE Results

In the **Summary** sheet click the **Export** button to open the dialog box shown in Figure 6.

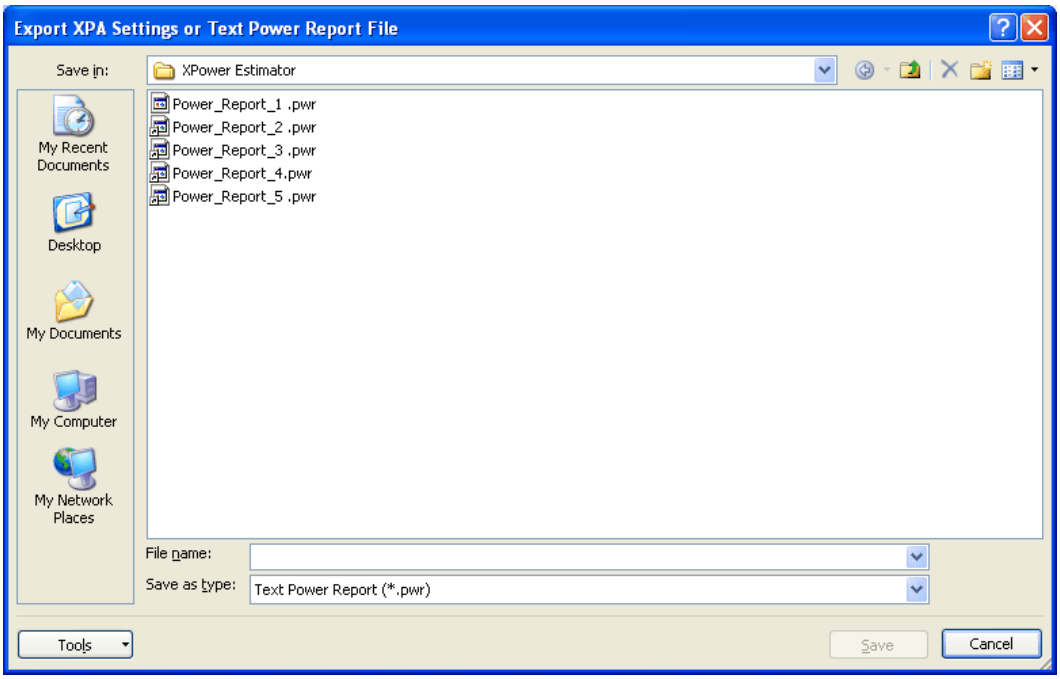

Figure 6: **Export Dialog Box**

In the dialog box the **Save as type** field lets you select among the following data formats:

- Export as **XPA Settings File (*.xpa)**

  Use this format to export XPE settings so they can then be applied to an XPower Analyzer session. This tool is typically used later in the design cycle when you are ready to perform a post place and route power analysis. The tool will create an .xpa file which contains all the environment settings, such as thermal, board and voltage properties. This simplifies the analysis setup in XPower Analyzer and ensures power data can be compared between the two tools.

  Note: To read the data exported from XPE into XPower Analyzer, enter the **Settings file** name (`*.xpa`) in the dialog box that appears when you open a design in XPower Analyzer (**File > Open Design**).

  Note: In the XPower (XPWR) command line tool, which performs a power analysis on your design within ISE, use the **`-x <file_name>`** switch to read in the XPE exported data.

- Export as **Text Power Report (*.pwr)**

  Use this format to export XPE **Summary** sheet results in a text format. XPE will save all the information on the **Summary** sheet in a sequence of tables so the information is easy to read. This feature can be used to archive or compare multiple scenarios. It can also help if your design flow uses scripts to parse and use XPE results.

Summary Sheet

The **Summary** sheet is the default sheet on launch and allows you to enter all device and environment settings. On this sheet the tool also reports estimated power rail-wise and block-wise so you can quickly review thermal and supply power distribution for your design (see Figure 7).

A **Project** field (top) and a **Comment** field (bottom) allow you to add a description or short details about the design or calculations related to the design. If your data does not fit in these boxes, then go to the **User** sheet. There you can add links, data tables, graphics, or any other object you can enter in a regular Excel document.

Note: The Spartan-3, Spartan-3E and Virtex-4 spreadsheets have a slightly different layout for this sheet. The description of the different user settings and data presented in this view is, however, applicable to these spreadsheets.

XILINX
XPower Estimator (XPE) - 13.2
Artix™-7, Kintex™-7, Virtex®-7
Release: 6-Jul-2011

Import File | Export File | Reset to Defaults | Set Default Rates

Project

Settings

Device	
Family	Kintex-7
Device	XC7K325T
Package	FBG900
Speed Grade	-2L
Temp Grade	Extended
Process	Typical
Characterization	Advance, 04-May-2011

Environment	
Junction Temperature	User Override
Ambient Temp	25.0 °C
Effective ΘJA	User Override
Airflow	250 LFM
Heat Sink	Medium Profile
ΘSA	3.3 °C/W
Board Selection	Medium (10"x10")
# of Board Layers	12 to 15
ΘJB	2.1 °C/W
Board Temperature	

Software	
Optimization	Balanced

On-Chip Power

Resource	(Jump to sheet)	Power (W)	(%)
Core Dynamic	CLOCK	0.348	7
	LOGIC	0.571	11
	BRAM	0.295	6
	DSP	0.360	7
	PLL	0.051	1
	MMCM	0.000	0
	PHASER	0.495	10
	PCIE	0.058	1
I/O	IO	1.125	22
Transceiver	GTX	1.398	28
Device Static		0.353	7

Power Supply

Source	Voltage	Total (A)
V_{CCINT}	1.000	2.069
V_{CCBRAM}	1.000	0.033
V_{CCAUX_IO}		
V_{CCAUX}	1.800	0.302
V_{CCO} 3.3V	3.300	
V_{CCO} 2.5V	2.500	
V_{CCO} 1.8V	1.800	0.625
V_{CCO} 1.5V	1.500	
V_{CCO} 1.35V	1.350	
V_{CCO} 1.2V	1.200	
$MGTV_{CCAUX}$	1.800	0.031
$MGTAV_{CC}$	1.000	0.733
$MGTAV_{TT}$	1.200	0.411
-		
-		
-		

Summary

Junction Temperature	33.0 °C	
Total On-Chip Power	5.053 W	
Thermal Margin	67.0°C	40.9W
Effective ΘJA	1.6 °C/W	

28%	Transceiver.....	1.398W
22%	I/O.....	1.125W
43%	Core Dynamic..	2.177W
7%	Device Static.....	0.353W
	Power supplied to off-chip devices.	0.000W

Messages

Comments

XILINX Power Solutions (check for updates) | File Support Request (WebCase) | XPower Estimator User Guide
Whitepaper - 7 Steps for Worst Case Power Estimation

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Legend: User Entry | Calculated Value | Summary Value | User Override | Warning | Error

Summary | CLOCK | LOGIC | IO | BRAM | DSP | PLL | MMCM | PHASER | PCIE | GTX | User | Graphs | Release

Figure 7: **Summary Sheet (Kintex-7) - Adjust Settings and Display Power Results**

Settings Panel

Use the **Settings** panel to specify details of the device, board, cooling and ISE settings. This panel varies slightly depending on the targeted device. A Virtex-6 example is presented in Figure 8.

Some settings are dependent on other settings. When this occurs the dependent cell becomes un-editable and turns to a grey background.

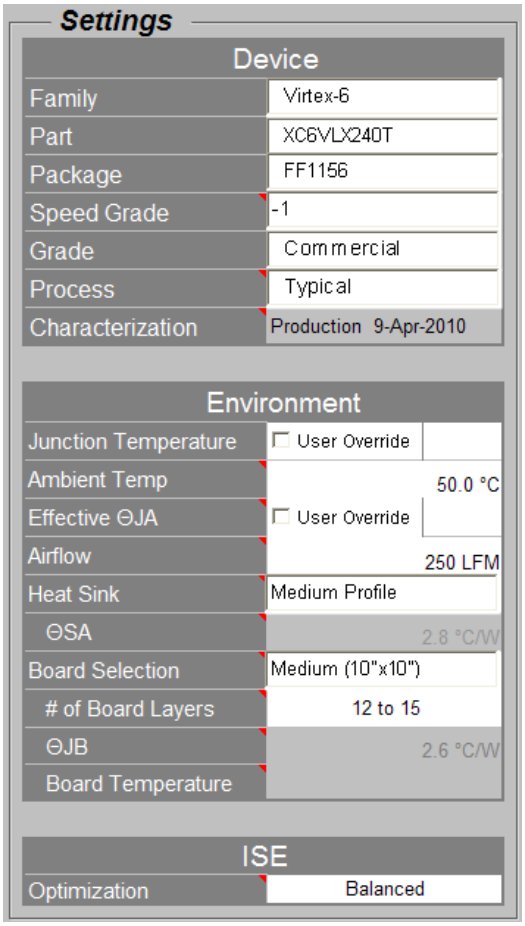

Figure 8: **Settings Panel (Virtex-6)**

The sections in the **Settings** panel are:

- **Device**

  Select the smallest device which meets your requirements.

  Note: Larger devices exhibit higher device static power consumption.

- **Environment**

  For XPE to report the estimated junction temperature it needs to understand how the device logic is configured and activated. It also needs a description of the device environment. The information of how heat can be transferred into the surrounding air (**ΘSA**) or PCB (**ΘJB**) affects the device junction temperature. If these parameters are known enter them; otherwise, select from the different drop-down menus the environment settings closest to your specific project. This will help to indirectly determine **Effective ΘJA**.

For more details about the thermal parameters of the XPower Estimator, please refer to Chapter 3: Thermal Management & Thermal Characterization Methods & Conditions in the *Device Package User Guide* (UG112).

- **ISE**

  ISE settings are available to focus the synthesis and implementation tools on minimizing towards different objectives. Adjust this area to best match the ISE settings you plan on using. This option affects the core dynamic power by an amount seen in a suite of customer designs.

  Optimization settings are:

  - Balanced – Default ISE options
  - Power – Minimize core dynamic power
  - Performance – Best timing performance
  - Area – Minimize slice usage
  - CPU – Minimize runtime

  These options are described in the ISE documentation for Design Goals and Strategies.

  Note: In the 7 series spreadsheet, this section is labeled **Software**, and only Balanced and Power Optimization settings are available.

- **Power mode**

  This setting allows you to review the estimated power for the different active and power down modes of the device. **Power Mode** is available for some device families.

Power Distribution Panels

There are two separate aspects to evaluate when integrating Xilinx FPGAs in a system. Typically designers first evaluate the FPGA current drawn on each voltage supply to ensure all voltage sources can provide enough power for the device to function properly. Second, designers need to know how much of that supplied power is consumed by the device itself as opposed to power supplied to off-chip components such as board termination networks. The power consumed on-chip, also referred to as thermal power, generates heat which must be transferred to the environment in order to maintain the device junction temperature within the normal operating range. Figure 9 shows the on-chip power contributing to junction temperature (**On-Chip Power** panel) and the total supply power (**Power Supply** panel).

On-Chip Power

Resource	(Jump to sheet)	Power (W)	Power (%)
Core Dynamic	CLOCK	0.348	7
	LOGIC	0.571	11
	BRAM	0.295	6
	DSP	0.360	7
	PLL	0.051	1
	MMCM	0.000	0
	PHASER	0.495	10
	PCIE	0.058	1
I/O	IO	1.125	22
Transceiver	GTX	1.507	29
Device Static		0.354	7

Power Supply

Source	Voltage	Total (A)
V_{CCINT}	1.000	2.070
V_{CCBRAM}	1.000	0.033
V_{CCAUX_IO}		
V_{CCAUX}	1.800	0.303
V_{CCO} 3.3V	3.300	
V_{CCO} 2.5V	2.500	
V_{CCO} 1.8V	1.800	0.625
V_{CCO} 1.5V	1.500	
V_{CCO} 1.35V	1.350	
V_{CCO} 1.2V	1.200	
$MGTV_{CCAUX}$	1.800	0.031
$MGTAV_{CC}$	1.000	0.786
$MGTAV_{TT}$	1.200	0.457
-		
-		
-		

Figure 9: **Power Distribution Panels (Kintex-7)**

On-Chip Power Panel

The **On-Chip Power** panel presents the total power consumed within the device. It includes device static and user design dependant static and dynamic power. The total is broken out by resource type. This view can help determine the amount of power being consumed and dissipated by the device. It also helps identify potential areas in the user logic where trade-offs or power optimization techniques could be used to meet the targeted power budget.

In this view you can click on the resource name to directly jump to the detailed sheet for this resource.

Power Supply Panel

The **Power Supply** panel displays the device estimated power across the different supply sources. This information can be used for instance to size or review voltage supply components, such as regulators. The table includes all power required by the internal logic along with power eventually sourced and consumed outside the FPGA, such as in external board terminations. This view includes both static and dynamic power.

You can adjust individual voltages within the supported range and XPE will calculate and display the total current required. When Maximum **Process** is selected in the **Environment** table and any power-on supply current values exceed the estimated operating current requirements, the **Power Supply** panel will display the minimum power-on supply requirements.

Multiple power supplies are required to power an FPGA. For logic resources typically available in Xilinx FPGAs, Table 2 presents the voltage source that typically powers them.

This table is provided only as a guideline because these details may vary across Xilinx device families.

Table 2: **FPGA Resources and the Power Supply that Typically Powers Them**

Power Supply	Resources Powered
V_{CCINT} & V_{CCBRAM}(3)	• All CLB resources • All routing resources • Entire clock tree, including all clock buffers • Block RAM/FIFO(1) • DSP slices(1) • All input buffers • Logic elements in the IOB (ILOGIC/OLOGIC)(1) • ISERDES/OSERDES(1) • PowerPC™ processor(1) • Tri-Mode Ethernet MAC(1) • Clock Managers (DCM, PLL, etc.) (minor) • PCIE and PCS portion of MGTs
V_{CCAUX} & V_{CCAUX_IO}(3)	• Clock Managers (MMCM, PLL, DCM, etc.)(1) • IODELAY/IDELAYCTRL(1) • All output buffers • Differential Input buffers • V_{REF}-based, single-ended I/O standards, e.g., HSTL18_I • Phaser
V_{CCO}	• All output buffers • Some input buffers • Digitally Controlled Impedance (DCI) circuits, also referred to as On-Chip Termination (OCT)(2)
MGT*	• PMA circuits of transceivers

Notes:

1. These resources are available only in certain device families. Refer to the appropriate data sheets and user guides for more information.
2. V_{CCO} in bank 0 (V_{CCO_0} or V_{CCO_CONFIG}) powers all I/Os in bank 0 as well as the configuration circuitry. See the applicable *Configuration User Guide*.
3. Xilinx 7 series FPGAs only

Summary Panel

The Summary panel presents in a concise format all the main data of interest (see Figure 7).

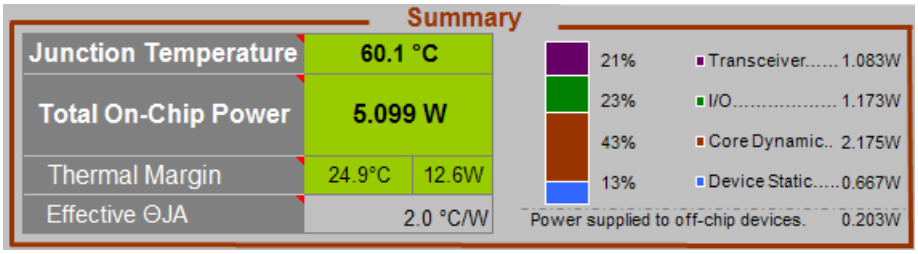

Figure 10: **Summary Panel (Virtex-7)**

- **Junction Temperature**

  Estimated junction temperature as the design operates. Each device operates within a temperature grade specified in the datasheet. The background for this cell turns orange when the value is outside the operating range (timing may be affected) and turns red when outside the absolute maximum temperature (device damage possible). The background color turns light blue when the value is set by user.

- **Total On-Chip Power**

  Includes power consumed and dissipated by the device across all supply sources. Also referred to as thermal power. This cell follows the color scheme of the **Junction Temperature** cell described above.

- **Thermal Margin**

  Temperature and power margin up to or in excess of the maximum accepted range for this device Grade. Thermal margin is negative when estimated junction temperature exceeds the maximum specified value. In this case, use this information to decide how best to address the excess power consumed on-chip.

- **Effective ΘJA**.

  The calculated Effective Thermal Resistance (Effective ΘJA) summarizes how heat is transferred from the die to the environment. The value is calculated from the settings entered in the **Environment** panel. If you have run thermal simulations of your environment then you may also override this value (in the **Environment** panel).

Resource Sheets

The following sections provide details for entering data into or interpreting results in the different available resource sheets. XPE only shows sheets available on the particular FPGA family and device selected. These resource sheets are organized with a center table where you enter utilization, configuration, and activity of the device resources you use. Above this main table are tables representing the total utilization and a summary of the resource's contribution to the total power per voltage supply.

These sheets represent usage based power; therefore, they include all power related to the utilization and configuration of the specified resource. The sheets do not include the leakage power contribution, since this is accounted for on the Summary sheet.

Clock Sheet

Important factors in dynamic power calculation are the activity and the load capacitance that needs to be switched by each net in the design. Some of the factors in determining the loading capacitance are fanout, wire length, etc. With clocks typically having higher activity and fanouts, the power associated with clock nets can be significant and thus is reported in a separate worksheet sheet (see Figure 11).

Summary

Clock Tree Power

Power		
V_{CCINT}	1.000V	0.348W
7% of total on-chip power 5.099W		

Utilization		
Global	32	100%
Regional	30	100%
Other	0	-

Name	Frequency (MHz)	Type	Fanout	Clock Buffer Enable	Slice Clock Enable	Power (W)
Global clock always active	250.0	Global	10000	100%	100%	0.164
	0.0	Global	0	100%	50%	0.000
Global clock with enable signal on driver	250.0	Global	10000	50%	100%	0.082
	0.0	Global	0	100%	50%	0.000
Global clock with enable signal on loads	250.0	Global	10000	100%	50%	0.102
	0.0	Global	0	100%	50%	0.000

Figure 11: **Clock Tree Power Example (Virtex-7)**

- Buffer **Type** Column

  Xilinx devices have different types of buffers capable of driving the clock routing structures and these types are modeled within XPE. Refer to the applicable *Device User Guide* to select the appropriate buffer type.

- Clock **Fanout** Column

  The number of synchronous elements driven by this clock.

- **Clock Buffer Enable** Column

  Gates the clock net at its source. The value is the percentage of the time in which the clock buffer is active. Reduce this percentage if you plan on disabling the clock net at the source when this portion of the design is not used. This reduces power.

- **Slice Clock Enable** Column

  Gates the clock net at its loads. Reduce this percentage if you plan on disabling some of the clock loads with slice level Clock Enable signals. This reduces power.

  Note: Some algorithms in software such as "Intelligent Clock Gating" will remap or change the packing in order to minimize this number.

Logic Sheet

The Logic sheet (see Figure 12) is used to estimate the power consumed in the CLB resources. The estimated power accounts for both the logic components and the routing. Two types of information should be entered:

- **Utilization** – Enter the number of LUTs, Shift Registers and LUT-based RAMs and ROMs. If your design or a previous generation has been implemented within ISE use the **Import** button in the **Summary** sheet to automatically import this information. Otherwise, use your experience to estimate utilization required to implement the desired functionality.
- **Activity** – Enter the **Clock** domain this logic belongs to. Then enter the **Toggle Rate** the logic is expected to switch and the **Average Fanout**.

  Note: The default setting for **Toggle Rate** (12.5%) and **Average Fanout** (3) are based on an average extracted from a suite of customer designs. In the absence of a better estimate for your specific design, Xilinx recommends using the default setting.

  Note: The **Signal Rate** column defines the number of millions of transitions per second for the considered element. This is a read-only column.

  Signal Rate is computed in this way:

  Signal Rate (Mtr/s) = Clock Frequency (Mhz) * Toggle rate (%)

Summary

Logic Power

Power		
V_{CCINT}	1.000V	0.573W
11% of total on-chip power 5.099W		

Utilization		
FFs	20,000	6%
LUTs	48,000	27%
Combinatorial	40,000	22%
Shift Registers	1,000	7%
Distributed RAMs	7,000	

Name	Clock (MHz)	LUTs as Logic	LUTs as Shift Registers	LUTs as Distributed RAMs	FFs	Toggle Rate	Average Fanout	Signal Rate (Mtr/s)	Power (W)
LUTs	250.0	20000	0	0	0	12.5%	3.00	31.3	**0.131**
	0.0	0	0	0	0	12.5%	3.00	0.0	0.000
LUTs with high fanout	250.0	20000	0	0	0	12.5%	6.00	31.3	**0.171**
	0.0	0	0	0	0	12.5%	3.00	0.0	0.000
Registers	250.0	0	0	0	10000	12.5%	3.00	31.3	**0.052**
	0.0	0	0	0	0	12.5%	3.00	0.0	0.000
Registers with high activity	250.0	0	0	0	10000	25.0%	3.00	62.5	**0.104**
	0.0	0	0	0	0	12.5%	3.00	0.0	0.000
Shift registers	250.0	0	1000	0	0	12.5%	3.00	31.3	**0.019**
	0.0	0	0		0	12.5%	3.00	0.0	0.000
Distributed memory	250.0	0	0	7000	0	12.5%	3.00	31.3	**0.096**
	0.0	0	0	0	0	12.5%	3.00	0.0	0.000

Figure 12: **Effect of LUT Configuration, Toggle Rates and Average Fanout on Power Estimation (Virtex-7)**

I/O Sheet

With higher switching speeds and capacitive loads, switching I/O power can be a substantial part of the total power consumption of an FPGA. Because of this, it is important to accurately define all I/O related parameters.

Figure 13 shows the top section of the I/O sheet (for the 7 series spreadsheet). Note that this sheet, as well as other sheets in the 7 series spreadsheet, contains buttons to display applicable documentation from the Xilinx website (in this case, the *7 Series SelectIO Resources User Guide* and the *7 Series FPGAs XADC User Guide)*.

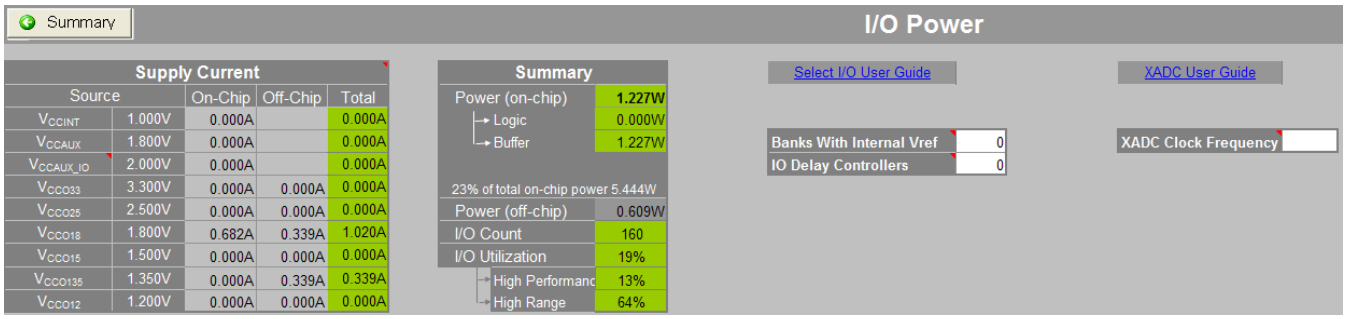

Figure 13: **I/O Sheet - Top Section (7 Series)**

In the I/O sheet XPE helps you calculate the on-chip and, eventually, off-chip power for your I/O interfaces. Figure 14 illustrates the three main types of information to enter: **IO Settings**, **Activity**, and, if needed, **External Termination**.

Name	Bank	I/O Settings								Activity						On Chip Power (W)				External Termination Output			Off Chip
	I/O Type	I/O Standard	Input Pins	Output Pins	Bidir Pins	I/O LOGIC SERDES	I/O DELAY	IBUF LP	Input Term	Clock (MHz)	Toggle Rate	Data Rate	Output Enable	Term Disable	IBUF Disable	Output Load (pF)	Signal Rate (Mtr/s)	V_{CCINT} 1.000V	V_{CCAUX} 1.800V	V_{CCAUX_IO} 2.000V	V_{CCO} all rails	Type	R/RDIFF	RS	V_{CCO} all rails
Bi-directional bus	HR	LVCMOS 1.8V 16mA (Slow)	0	0	32	No	Off	Yes	None	100.0	12.5%	SDR	100.0%	0.0%		5	12.5	0.000	0.001	0.000	0.012	None			0.000
Bi-directional w/ 50% OE rate	HR	LVCMOS 1.8V 16mA (Slow)	0	0	32	No	Off	Yes	None	100.0	12.5%	SDR	50.0%	0.0%		5	12.5	0.000	0.001	0.000	0.009	None			0.000
Output w/ external termination	HP	SSTL Class II 1.8V	0	32	0	No	Off	Yes		100.0	12.5%	SDR	100.0%	0.0%		5	12.5	0.000	0.002	0.000	0.237	Parallel	50		0.609
Output w/ DCI termination	HP	SSTL Class II DCI 1.8V	0	32	0	No	Off	Yes		100.0	12.5%	SDR	100.0%	0.0%		5	12.5	0.000	0.002	0.000	0.848	None			0.000
Output w/ T_DCI termination	HP	SSTL Class II T DCI 1.8V	0	32	0	No	Off	Yes		100.0	12.5%	SDR	100.0%	0.0%		5	12.5	0.000	0.002	0.000	0.159	None			0.000

Figure 14: **I/O Sheet - Effect of Output Enable Rate on Power Estimates for Inputs, Outputs, and Bidirectional I/Os (7 Series)**

The following paragraphs provide more information on how to fill in each of these columns.

- **I/O Settings**
  - **I/O Standard**

    Specify here the expected I/O standard you will use for this interface. Configurations which use the on-chip terminations are shown with a **DCI** suffix in this drop-down menu. Differential I/O standards have a **(pair)** suffix. For calculations, XPE assumes the standard V_{CCO} level (for example, 3.3V) that is closest to the nominal listed in the datasheet for that I/O standard.

    Tip: To minimize power on output signals always use the weakest driver settings which meet your performance goals (lower the drive strength and slew rate).

    Tip: Using on-chip terminated standards is a good way to improve the signal integrity of the waveforms seen by the receiver. Since the terminations are

embedded inside the FPGA, the termination power will contribute to raising the device junction temperature. In order to minimize this power try to use the tri-statable on-chip terminated standards (denoted **T_DCI**) whenever possible.

- I/O Direction Columns

  Enter the number of **Input**, **Output** and **Bidir** (bidirectional) signals for each I/O interface.

  Tip: Since toggling activity of inputs and outputs is often very different, Xilinx recommends you place each direction on a separate row.

  Tip: Enter one pin for each differential I/O pair. For instance, if your memory has four differential DQS pairs, enter **4** on the **Input Pins** column.

- I/O Performance Settings

  These performance settings, such as **IO LOGIC SERDES** or **IO DELAY**, are family dependent. Enter the configuration in which you expect to program these I/Os.

  Tip: typically performance settings increase power consumption. Try to enable these setting only if your I/O interface absolutely requires them.

- **Activity**

  Enter in these four columns the expected activity for each I/O interface.

  - **Clock (MHz)**

    Synchronous signals: Enter the frequency of the clock capturing or generating these signals.

    Asynchronous signals: Calculate the equivalent frequency of the signal. For instance, if you can determine the signal will toggle (change state) 2 million times per second then enter 1 in this column (when converting signal rate to frequency you need 2 transitions to make a period: the transition from 0 to 1 and the transition from 1 to 0).

  - **Toggle Rate**

    Synchronous elements: Enter how often compared to the clock this signal is expected to change state. For instance if the data changes every 8 clock cycles on average, enter 12.5% (1/8, converted to a percentage).

    Asynchronous elements: As explained in the **Clock (MHz)** description above, enter the equivalent frequency in the **Clock (MHz)** column then enter 100% in this column.

  - **Data Rate**

    Synchronous elements: Enter **DDR** if the signal is sampled on both the positive and negative edges of the clock.

    Asynchronous elements: This column is not applicable (leave value at **SDR**).

  - **Output Enable**

    Input only signals: This column has no effect.

    Output and bi-directional signals: Specify for a long period of time how much of this time the output buffer is driving a value (compared to the time the driving buffer is disabled or tri-stated.

    Tip: As shown in Figure 14 (red frame) for line 1 and 2, setting **Output Enable** to **100%** is a common mistake which degrades the tool accuracy.

- **Signal Rate**

  Defines the number of millions of transitions per second for the considered element. This is a read-only column.

  Signal Rate is computed in this way:

  For Inputs:

  Signal Rate (Mtr/s) = Clock Frequency (Mhz) * Toggle rate (%) * Data Rate

  For Outputs:

  Signal Rate (Mtr/s) = Clock Frequency (MHz) * Toggle Rate (%) * Data Rate * Output Enable Rate (%)

- **External Termination**

  When not using the available on-chip termination you can use XPE to calculate the power supplied by the FPGA to off-chip components such as external board termination resistor networks. When the **Show External Board Termination Settings** checkbox is checked, additional columns appear in the table. Also, a graphic appears below the table and shows the supported **External Board Termination Topologies**, so you can easily understand which column to fill depending on the topology you want to build.

  Multiple termination types are supported for I/Os configured as outputs. External input terminations are not supported since calculations often require details of the driver side but these details are not available to XPE.

  - **Term. Type**

    Select the appropriate topology from this drop-down menu.

  - **R/RDIFF** and **RS**

    Some termination schemes require two resistor values while others require only a single value. Refer to the termination graphic then enter the resistor value on the appropriate column. Figure 15 shows the supported I/O termination topologies in this release.

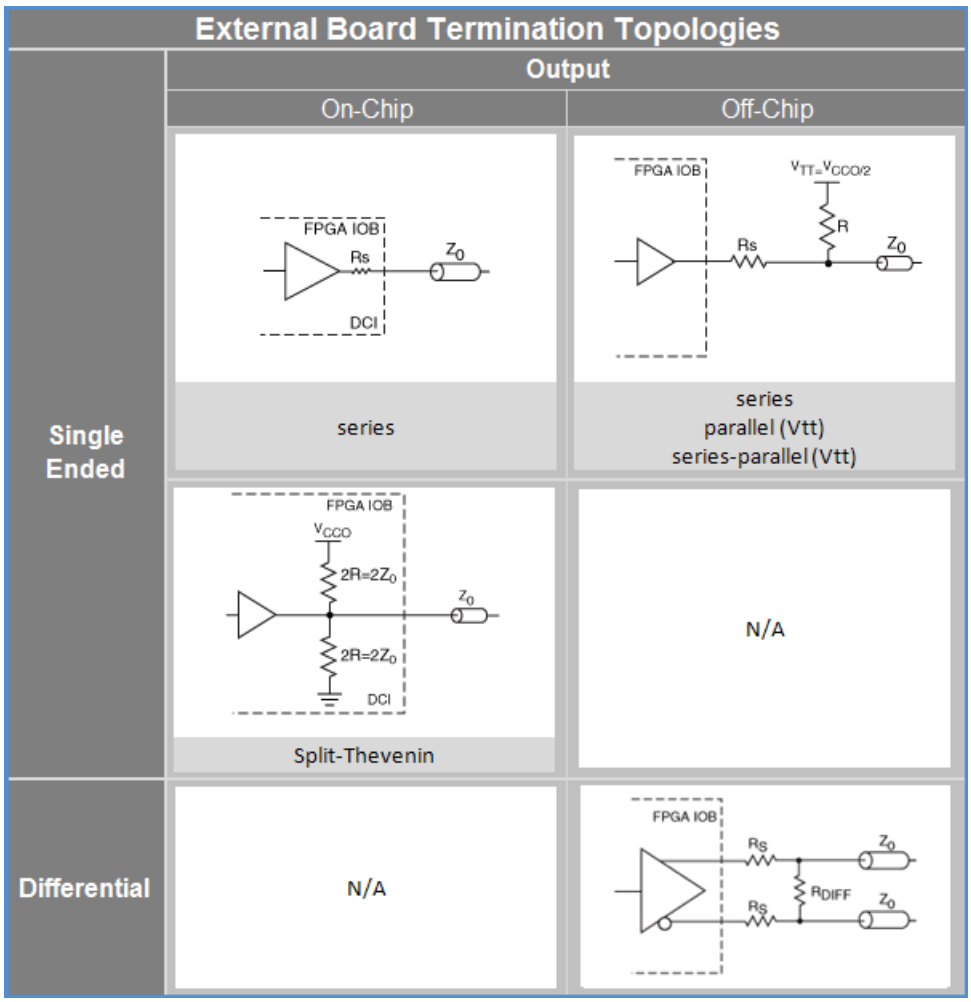

Figure 15: **External I/O Termination Topologies (Virtex-6)**

Block RAM (BRAM) Sheet

FPGA devices have dedicated Block RAM resources. To accurately set Block RAM parameters in XPE, a good understanding of device resources and configuration possibilities is recommended. This information is available in the BRAM section of the device family *Device User Guide*. If implementation details for the block RAM are known, follow the guidelines described in the For Better Accuracy section. Otherwise, refer to Preliminary BRAM Estimates.

Note: Distributed RAM/ROM and SRL usage should be specified in the Logic Sheet.

- **Enable Rate** column

  Use the **Enable Rate** to specify the percentage of time each block RAM's ports are enabled for reading and/or writing. To save power, the RAM enable can be driven Low on clock cycles when the block RAM is not used in the design. BRAM **Enable Rate**, together with **Clock** rate, are important parameters that must be considered for power optimization.

- **Write Rate** column

  The **Write Rate** represents the percentage of time that each block RAM port performs write operations. The read rate is understood to be 100% – write rate.

- **Signal Rate** column

  Defines the number of millions of transitions per second for the considered BRAM output port. This is a read-only column which takes into account port enable rates and a weighted average of the port widths.

Figure 16 illustrates the effect of block RAM configuration modes and bit widths on power estimates.

Summary

Block RAM Power

Power		
V_{CCINT}	1.000V	0.265W
V_{CCBRAM}	1.000V	0.029W
6% of total on-chip power 5.163W		

Utilization		
RAMB18	150	17%
RAMB36	50	11%

Memory Resources User Guide

Name	BRAMs	Mode	Toggle Rate	Port A Clock (MHz)	Port A Enable Rate	Port A Bit Width	Port A Write Mode	Port A Write Rate	Port B Clock (MHz)	Port B Enable Rate	Port B Bit Width	Port B Write Mode	Port B Write Rate	Signal Rate (Mtr/s)	Power (W) V_{CCINT} 1.000V	Power (W) V_{CCBRAM} 1.000V
Single port	50	RAMB18SDP	50.0%	250.0	25.0%	36	WRITE_FIRST	50.0%	0.0	25.0%	36	WRITE_FIRST	50.0%	31.250	0.054	0.006
		RAMB18	50.0%	0.0	25.0%	1	READ_FIRST	50.0%	0.0	25.0%	1	WRITE_FIRST	50.0%	0.000	0.000	0.000
Simple dual port	50	RAMB18SDP	50.0%	250.0	25.0%	36	WRITE_FIRST	50.0%	250.0	25.0%	36	WRITE_FIRST	50.0%	31.250	0.064	0.006
(PortA: write PortB: read)		RAMB18	50.0%	0.0	25.0%	1	WRITE_FIRST	50.0%	0.0	25.0%	1	WRITE_FIRST	50.0%	0.000	0.000	0.000
		RAMB18	50.0%	0.0	25.0%	1	WRITE_FIRST	50.0%	0.0	25.0%	1	WRITE_FIRST	50.0%	0.000	0.000	0.000
True dual port	50	RAMB18	50.0%	250.0	25.0%	18	WRITE_FIRST	50.0%	250.0	25.0%	18	WRITE_FIRST	50.0%	31.250	0.053	0.006
		RAMB18	50.0%	0.0	25.0%	1	WRITE_FIRST	50.0%	0.0	25.0%	1	WRITE_FIRST	50.0%	0.000	0.000	0.000
FIFO	50	FIFO36	50.0%	250.0	25.0%	36	WRITE_FIRST	50.0%	250.0	25.0%	36	WRITE_FIRST	50.0%	31.250	0.093	0.012

Figure 16: **Block RAM Sheet - Effect of Block RAM Configuration Modes and Bit Widths on Power Estimates (Kintex-7)**

Preliminary BRAM Estimates

If the exact block RAM types and modes to be used in the design are unknown, the best approach is to determine how many kilobytes of memory are needed in the design and use the appropriate number of basic 18k True dual-port RAMs. If the data width of memory access is known, select this from the drop-down menu for each port. Depth and width are the two most important characteristics of a memory.

For Better Accuracy

If the breakdown of the memory usage of your design is known, the XPE spreadsheet allows you to specify which block RAM modes are being used. The **Mode** column has selectable values from a drop-down menu that lists the different ISE primitive names and modes of the block RAM. Depending on the target family, this includes:

- **BRAM** - Simple dual-port or True dual-port Block RAM,
- **FIFO** - Dedicated built-in FIFO,
- **CASC (pair)** - Cascaded block RAM blocks (built from two RAM blocks),
- **ECC** - When the block RAM is configured in ECC mode.

In True dual-port mode the following data write mode options are available:

- **WRITE_FIRST** – The port will first write to the location and then read out the newly written data.
- **READ_FIRST** – The old data is first read out and then the new data is written in. This mode effectively allows 4 operations per clock cycle (saving power or resource utilization) – as the old data can be read out and replaced with new data on the same clock cycle of each port.
- **NO_CHANGE** – When a Write happens the block RAM outputs remain unchanged.

Clock Management Resource Sheets (DCM, PMCD, PLL, MMCM)

Xilinx FPGA families have different clock generation and management capabilities. To enter information in these sheets, first review the *Device User Guide* to understand how to parameterize these resources in XPE. Depending on the step in the project development cycle you may or may not already know all the clocking details for your design. Enter what is known or can be estimated first, then later you can always reopen and complete the spreadsheet as design details become available.

Figure 17 shows a sample clock management resource sheet (the **PLL Power** sheet).

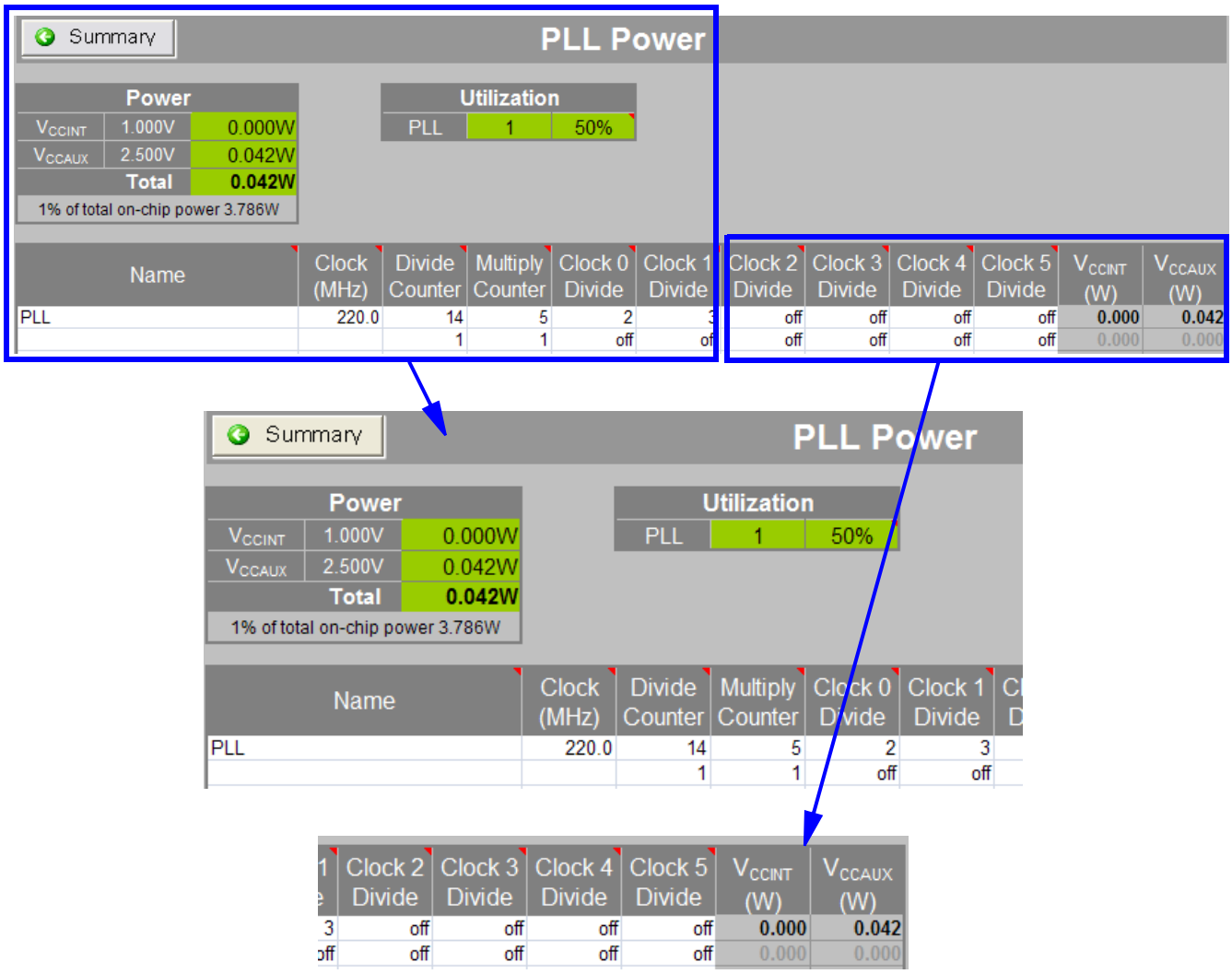

Figure 17: **PLL Power Sheet (Virtex-5)**

DSP Sheet (MULT, DSP48)

Xilinx FPGA families have different Digital Signal Processing (DSP) blocks with different capabilities. To enter information in these sheets first review the *Device User Guide* to understand the parameters in the DSP sheet.

Tips:

- For random input data, a good **Toggle Rate** approximation for DSP operations is 50%.
- DSP slices have clock enable (CE) ports. When entering data in the **Toggle Rate** column remember to multiply your data input toggle rate with the DSP slice clock enable rate. For example, if random data (typically ~38% data toggle rate) is input into the DSP slice and the slice is clock enabled only 50% of the time, then the output data toggle rate should be scaled by the CE rate such that the data toggle rate becomes 19% (38% x 50%). see Figure 18 for a Virtex-7 example.
- For families which have a register within the multiplier (MREG), using this pipeline register helps lower dynamic power.

Summary

DSP48E1 Power

Power		
V_{CCINT}	1.000V	0.109W
5% of total on-chip power 2.190W		

Utilization		
DSP48	60	8%

Name	DSP Slices	Clock (MHz)	Toggle Rate	MULT Used?	MREG Used?	Pre-add Used?	Signal Rate (Mtr/s)	Power (W)
Multiplier with pipeline register	20	250.0	12.5%	Yes	Yes	No	31.3	0.018
		0.0	12.5%	Yes	Yes	No	0.0	0.000
Multiply accumulate	20	250.0	12.5%	Yes	Yes	Yes	31.3	0.020
		0.0	12.5%	Yes	Yes	No	0.0	0.000
DSP with high activity on inputs	20	250.0	50.0%	Yes	Yes	No	125.0	0.072
		0.0	12.5%	Yes	Yes	No	0.0	0.000
		0.0	12.5%	Yes	Yes	No	0.0	0.000
		0.0	12.5%	Yes	Yes	No	0.0	0.000

Figure 18: **DSP48E1 Power Sheet (Virtex-7) - Effect of Clock, Toggle Rate, and MREG on Power Estimates**

Multi-Gigabit Transceiver Sheets (MGT, GT, GTP, GTX, GTH)

Different Xilinx FPGA families have Multi-Gigabit Transceivers (MGT), which are very high performance serial I/Os. Transceivers typically use separate voltage supplies for the PCS, PMA and termination. To understand each family MGT capabilities and how to enter settings within XPE refer to the applicable *Transceiver User Guide*.

To simplify data entry, drop-down menus are provided with parameter preferred or required values. Figure 19 shows an example Kintex-7 XC7K325T design. The tables in the sheet header report design power and currents. Device leakage for each supply is reported on the Summary sheet.

Note: XPE calculates power for each channel including the power of all associated circuits, shared resources between channels, IO buffers, reference clock circuitry, etc. You therefore do not have to enter resource usage on any other sheet (for example, Clock or I/O) to describe the transceiver resources used.

XPE presents the MGT information in an architecture-specific way. Entering 2 or any multiple of 2 channels for a GTP/GTX_DUAL entry assumes that those channels use the minimum number of DUALs. Similarly, for GTHE1 and GTXE2 4 channels share common circuitry, so XPE assumes each line uses the minimum number of quads. To use 2 channels from one quad and 2 from another, simply specify them on two rows in XPE.

XPE does not support all of the possible MGT configurations. See the specific *Transceiver User Guide* for more information.

Summary

GTX Transceiver Power

Supply Current		
Source		Total
V_{CCINT}	1.000V	0.149A
$MGTV_{CCAUX}$	1.800V	0.031A
$MGTAV_{CC}$	1.000V	0.708A
$MGTAV_{TT}$	1.200V	0.404A

Power		1.398W
Source	Power	
V_{CCINT}	0.149W	
$MGTV_{CCAUX}$	0.056W	
$MGTAV_{CC}$	0.708W	
$MGTAV_{TT}$	0.485W	28% of total on-chip power 5.053W
PMA	1.248W	
PCS	0.149W	

Utilization		
GTX Channels	6	38%
Power Planes	1	

Transceivers User Guide

					RX				TX								
Name	GTX Channels	Operational Mode	Power Mode	Channels Sharing LC PLL	Clock Source	Data Rate (Gb/s)	Data Path	8b/10b	Clock Source	Data Rate (Gb/s)	Data Path	8b/10b	O/P (mV)	V_{CCINT} Power (W)	$MGTV_{CCAUX}$ Power (W)	$MGTAV_{CC}$ Power (W)	$MGTAV_{TT}$ Power (W)
Bi-Directional channel	2	Transceiver	Low Power	4	LC	5.0000	20		LC	5.0000	20		600	0.050	0.019	0.265	0.175
		Transceiver	Low Power	4	LC	5.0000	20		LC	5.0000	20		600	0.000	0.000	0.000	0.000
Transmitter only	2	Transceiver	Low Power	4	LC	5.0000	20		LC	5.0000	20		600	0.050	0.019	0.265	0.175
		Transceiver	Low Power	4	LC	5.0000	20		LC	5.0000	20		600	0.000	0.000	0.000	0.000
Receiver only	2	Receiver	Low Power	4	LC	5.0000	20							0.050	0.019	0.178	0.135

Figure 19: **GT Power Sheet (Kintex-7) Illustrating Data Rate and Power Estimates**

EMAC and TEMAC Sheets

Different Xilinx device families contain Tri-Mode Embedded Ethernet Media Access Controller (MAC) blocks, which are used in Ethernet applications. The Ethernet MACs are paired within a TEMAC block, share a common host and DCR interface, but are independently configurable to meet all common Ethernet system connectivity needs. Refer to the applicable EMAC *User Guide* for a detailed description of the block capabilities and configuration.

In XPE, you need only enter the EMAC operating clock frequency (See Figure 20). You typically need to know the mode and operating speed to obtain the correct clock frequency.

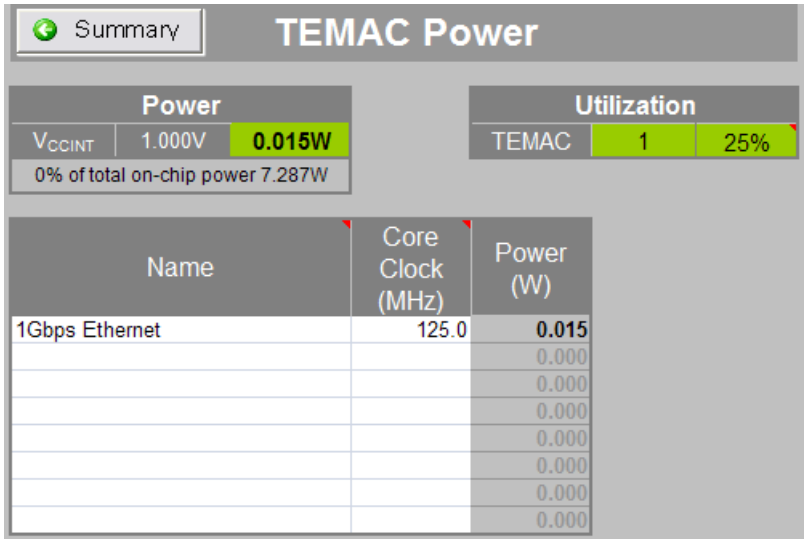

Figure 20: **TEMAC Power Sheet (Virtex-6)**

PCIE Sheet

Different Xilinx device families have Integrated Endpoint Block for PCI Express® designs (integrated Endpoint block). For detailed PCIE information, refer to the applicable PCIE *User Guide* and enter in XPE the settings which correspond to your application.

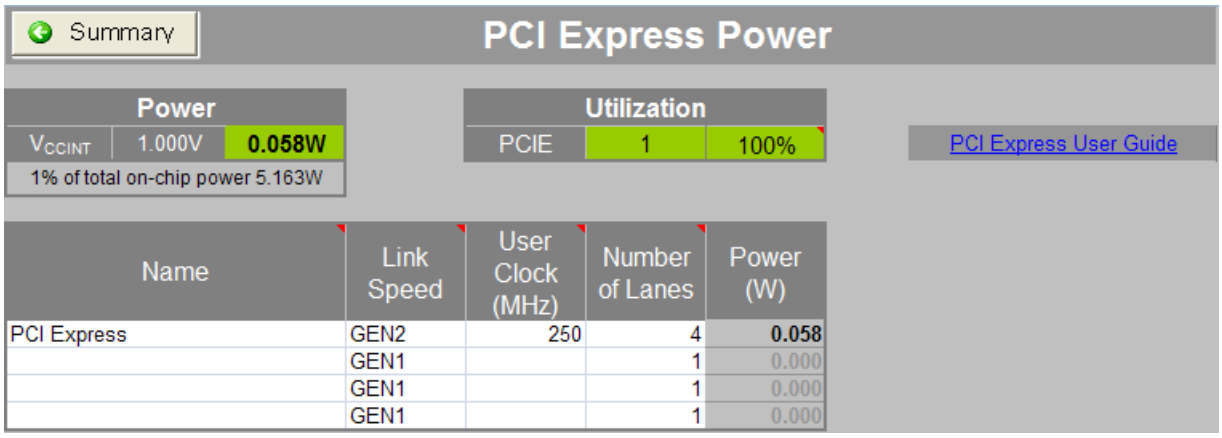

Figure 21: **PCIE Power Sheet (Kintex-7)**

PPC405 and PPC440 (PowerPC) Sheets

Some Xilinx FPGA families contain high-performance PowerPC® microprocessor embedded blocks.

For power estimation, these blocks are represented in a separate sheet within XPE. Details for each PowerPC's settings are available in the applicable *Device User Guide*. Typically you can provide the processor main clock frequency along with details of the processor local bus, memory and eventual DMA controllers. Figure 22 presents a Virtex-5 example.

Summary

PPC440 Power

Power		
V_{CCINT}	1.000V	**0.414W**
11% of total on-chip power 3.786W		

Utilization		
PPC440	1	100%

Name	PPC440 Clock (MHz)	Interconnect Clock (MHz)	DMA 0 Clock (MHz)	DMA 1 Clock (MHz)	DMA 2 Clock (MHz)	DMA 3 Clock (MHz)	Power (W)
PPC440	250.0	125.0	125.0				**0.414**
							0.000

Figure 22: **PPC440 Power Sheet (Virtex-5)**

Phaser Sheet

Phaser blocks are available in 7 Series devices to simplify the interface with high-speed memory devices. For power estimation, these blocks are represented in a separate sheet within XPE. Details for each Phaser setting are available in the *7 Series FPGAs Memory Interface Solutions User Guide (UG586)*. Figure 23 presents a Virtex-7 example.

Summary

Phaser Power

Power		
V_{CCINT}	1.000V	0.246W
V_{CCAUX}	1.800V	0.087W
	Total	**0.333W**
7% of total on-chip power 5.099W		

Utilization		
Phaser	2	14%

Name	Input FIFOs	Output FIFOs	Phaser Ins	Phaser OUTs	FIFO Clock (MHz)	Memory Clock (MHz)	V_{CCINT} (W)	V_{CCAUX} (W)
2133Mbps interface (DDR3)	2	2	4	4	266.0	1066.0	**0.147**	**0.052**
							0.000	0.000
1333 Mbps interface (DDR3)	2	2	4	4	333.0	666.0	**0.099**	**0.035**

Figure 23: **Phaser Power Sheet (Virtex-7)**

User Sheet

This sheet is intentionally left blank and user editable. On this sheet you can provide any documentation (text, image or hyperlinks), details about the project, assumed conditions, or collect the results important to your application.

Automating XPE

To simplify data entry and export or to assist with data manipulation Microsoft Excel offers a variety of mechanisms which you can use to increase your productivity or the breadth of your power estimation and analysis. The following section provides reference material and examples to help you get started quickly with Excel internal automation features and interface with some of the most common external scripting languages.

Using Named Cells

Excel provides a mechanism to name a cell or a range of cells so these can be used within formulae or scripts without referring to them as cell XY coordinates. Since the XPE spreadsheet is protected you cannot see 'named' cells defined on the protected areas. You can however name cells in the unprotected area (User sheet). The following tables and examples show the named cells within XPE that are available to facilitate user formulas and scripting.

Get available resource counts.

The following named cells represent the maximum available resources available for the considered device and package. None of these cells are visible in the spreadsheet, however you can use these read only values in your calculations.

Resource	Named Cells	Description
LUTs	NUM_LUTS	Includes all LUTS
	NUM_LUTRAM	Shift Registers and Distributed Memories LUTs
Registers	NUM_FFS	
DSP blocks	NUM_DSPS	
BlockRAMs	NUM_BRAMS	
PLLs	NUM_PLLS	
MMCMs	NUM_MMCMS	
DCMs	NUM_DCMS	
Transceivers	NUM_GTPS	Lowest speed blocks
	NUM_GTS	Lower speed blocks
	NUM_GTHS	High Speed blocks
	NUM_GTZS	Highest Speed blocks

Examples:

Formulas to quickly set device utilization and evaluate thermal effects when varying device, package or cooling parameters:

`= INT(NUM_LUTS * 0.75)` Sets total LUT utilization to 75% of device capacity (if entered on the Logic sheet)

`= INT(NUM_DSPS * 0.90)` Sets DSP block utilization to 90% of device capacity (if entered in DSP sheet)

Get device operating limits.

The following named cells represent operating limits for the considered device, package, speed grade and temperature grade. None of these cells are visible in the spreadsheet however you can use these read only values in your calculations.

Table 3: **Operating Limits - Named Cells**

Resource	Named Cells	Description
Temperature	TJ_MAX	Maximum operating junction temperature (°C)
	TJ_MIN	Minimum operating junction temperature (°C)
Voltages	VCC_MAX	Maximum operating V_{CCINT} voltage (V)
	VCC_MIN	Minimum operating V_{CCINT} voltage (V)
Transceivers	GTP_MAXRATE	Maximum data rate of lowest speed blocks (Gbps)
	GTX_MAXRATE	Maximum data rate of lower speed blocks (Gbps)
	GTH_MAXRATE	Maximum data rate of high speed blocks (Gbps)
	GTZ_MAXRATE	Maximum data rate of highest speed blocks (Gbps)

Example:

Formula to enter into the user **Junction Temperature** cell on the Summary sheet to force the device junction temperature to the maximum allowed while evaluating different temperature or device and package combination

```
= TJ_MAX
```

Get and edit summary information.

Many cells in the Summary sheet or tables at the top of the other sheets are named. To find these names in Excel you can select the cell then if it is named the 'name box' area of the formula bar will show that name. The following paragraph highlights some of the most commonly used cells on the Summary sheet.

Table 4: **Summary Panel - Named Cells (See Figure 10)**

Named Cell	Description
JUNCTION_TEMP	Estimated or forced **Junction Temperature** (°C)
THERMAL_MARGIN_C	Temperature margin for the device temperature grade (°C)
TJA	Estimated or specified **Effective ΘJA** (°C/W)
TOTAL_POWER	**Total On-Chip Power** (W)
THERMAL_MARGIN_W	Power margin for the device temperature grade (W)
OFFCHIP_POWER	Total power supplied to off-chip devices (W)

Table 5: **On-Chip Power Panel - Named Cells (See Figure 9)**

Named Cell	Description
CLOCK_POWER	Clock tree power (W)
LOGIC_POWER	CLB Logic power (W)
BRAM_POWER	BlockRAM power
DSP_POWER	DSP blocks power (W)
PLL_POWER	PLL blocks power (W)
MMCM_POWER	MMCM blocks power (W)
PHASER_POWER	PHASER blocks power (W)
PCIE_POWER	PCIE blocks power (W)
IO_POWER	SelectIO blocks power (W)
GTP_POWER	Lowest speed transceiver blocks power (W)
GTX_POWER	Lower speed transceiver blocks power (W)
GTH_POWER	High speed transceiver blocks power (W)
GTZ_POWER	Highest speed transceiver blocks power (W)
STATIC_POWER	Device static power (W)

Table 6: **Power Supply Panel - Named Cells (See Figure 9)**

Named Cell	Description
VCCINT	V_{CCINT} core voltage level (V)
VCCBRAM	V_{CCBRAM} voltage level (V)
VCCAUX	V_{CCAUX} voltage level (V)
VCCAUX_IO	V_{CCAUX_IO} voltage level (V)
VCCO33	V_{CCO} 3.3V voltage level (V)
VCCO25	V_{CCO} 2.5V voltage level (V)
VCCO18	V_{CCO} 1.8V voltage level (V)
VCCO15	V_{CCO} 1.5V voltage level (V)
VCCO135	V_{CCO} 1.35V voltage level (V)
VCCO12	V_{CCO} 1.2V voltage level (V)

Table 7: **Environment Table - Named Cells (See Figure 8)**

Named Cell	Description
AMBIENT_TEMP	Ambient temperature (°C)
BOARD_TEMP	Board temperature (°C)
CUSTOMTSA	User specified Theta SA thermal resistance (°C/W)
CUSTOMTJB	User specified Theta JB thermal resistance (°C/W)

Table 8: **Miscellaneous Named Cells**

Named Cell	Description
PROJECT	User description of the spreadsheet
COMMENTS	User comment
VERSION	Spreadsheet revision
RELEASE_DATE	Spreadsheet release date

Using Formulas

With Excel formulas you can simplify data entry, spreadsheet parameterization or create customer reports as explained in the following examples

Example1: Set clock frequency of all attached synchronous loads in a single place.

Typically a clock net may reach multiple types of resources. Instead of entering the clock frequency on each sheet the following formula can be used on the resource sheets while the clock frequency is only defined once in the Clock sheet. Any change of the clock frequency would immediately be reflected on all the linked resource sheets

```
=CLOCK!E19
```

Example 2: Calculate the fanout sum of all the different loads driven by a clock.

On the clock sheet you may find it useful to enter formulas similar to:

```
=SUM(LOGIC!G10:I10,BRAM!E10,DSP!E8)
=SUM(IO!I10:K12)
```

Example 3: Select the GTX data rates to the PCIe interface speed and number of lanes. Entering the following formulae for GTX line rate and number of channels will track the PCIe interface.

- Set channel data rate based on the PCIE bock configuration (if entered on the GTX sheet)

  ```
  =IF(PCIE!E8="GEN3",8,IF(PCIE!E8="GEN2",5,2.5))
  ```

- Set the number of GTX channels to reflect the number of PCIE lanes (if entered on the GTX sheet)

  ```
  =PCIE!G8
  ```

Example 4. Parameterize the spreadsheet entry using formulas and the **User** sheet. Figure 24 illustrates how to evaluate power when a module is replicated more or fewer times in the design. By varying the number of instances, the quantity of resources for the base blocks, or clock frequency, an Excel formula can automatically recalculate the values which need to be entered in other sheets. In Figure 24, the value for **Number instance** (named **num_inst**) in the **User** sheet automatically calculates utilization and activity for cells that appear in the **Logic** sheet.

B8 =30*num_inst

	A	B	C	D	E	F	G
1	This sheet is intentionally blank and provided for the user to perform any calculations or a						
2							
3	Number instance	10					
4	clk1	250	MHz				
5	clk2	25	MHz				
6							
7	Module	LUT	FF	Toggle	Fanout	BRAM	IO
8	Top	=30*num_inst	=20*num_inst	0.75	3	0	=16*num_inst
9	s2p	=140*num_inst	=140*num_inst	0.5	20	0	
10	proc	=1600*num_inst	=140*num_inst	0.75	10	0	
11	p2s	=40*num_inst	=40*num_inst	0.5	5	=4*num_inst	
12							

Summary | CLOCK | LOGIC | IO | BRAM | DSP | MMCM | GTX | TEMAC | PCIE | User

Summary — Logic Power

Name	Clock (MHz)	LUTs as Logic	LUTs as Shift Registers	LUTs as Distribu RAMs
top	=UserIB4	=UserIB8	0	
sunit[1..10]				
s2p	=UserIB4	=UserIB9	0	
proc	=UserIB5	=UserIB10	0	
p2s	=UserIB4	=UserIB11	0	
	0.0	0	0	

Figure 24: **Parameterizing Data Entry Using Formulas on the User Sheet**

Using Visual Basic Macros

The following examples define the public Visual Basic functions defined in the Xilinx 7 series XPE spreadsheet to help you with your automation needs. They provide convenient ways to load files, create power reports, change parts, packages and environment settings from Excel or another program.

- Create a text power report and save with name specified as argument.

```
Public Sub GeneratePowerReportFile(FileName As String)
```

- Create a settings file and save with name specified as argument. This file can later be used in XPower Analyzer.

```
Public Sub GenerateXPAFile(FileName As String)
```

- Import an existing XPE spreadsheet (.xls* path/file specified as argument).

```
Public Sub ImportXPEFile(path As String)
```

- Import a place and route map report (.mrp path/file specified as argument).

```
Public Sub ImportMapReportFile(FileName As String)
```

- Import a implementation results in the .xpe format. Review the Import dialog options for details and format of the different arguments.

```
Public Sub ImportXmlFile(FileName As String, Append As
Boolean,DevSettings As Boolean, EnvSettings As Boolean,
VoltSettings As Boolean, IOSettings As Boolean)
```

- Set the default voltages for all supply voltages. Set argument to False for Nominal voltages and to true for Maximum voltage levels.

```
Public Sub SetDefaultVoltages(Maximum As Boolean)
```

- Set the **Device** field on the summary sheet (will automatically adjust the **Family** field if required).

```
Public Function SetDevice(Device As String) As Boolean
```

- Set the **Package** field on the Summary sheet.

```
Public Function SetPackage(Package As String) As Boolean
```

- Set the **Process** field on the summary sheet. Set argument to False for Typical process and True for Maximum process.

```
Public Sub SetProcess (Maximum As Boolean)
```

- Set the **Temp Grade** field on the Summary sheet. Options are "Commercial", "Industrial", "Q-Grade", "Extended”, etc.

```
Public Function SetTemperatureGrade (Grade as String) as Boolean
```

- Set the **Speed Grade** field on the Summary sheet. Options are "-1", "-1L", etc.

```
Public Function SetSpeedGrade (Grade as String) as Boolean
```

- Set the **Heat Sink** field on the Summary sheet. "Custom", "None", "Low Profile"

```
Public Function SetHeatSink (Sink as String) as Boolean
```

- Set the **Board Selection** field on the Summary sheet. Options are "Custom", "JEDEC", "Small", "Medium", "Large".

```
Public Function SetBoard (BoardSize as String, BoardLayers as
Integer) as Boolean
```

- Set the **User Override** for the **Junction Temperature**, and value.

```
Public Function SetJunctionTemperature(Temperature As Double,
OverRide As Boolean) As Boolean
```

- Set the **User Override** for the **Effective ThetaJA**, and value.

```
Public Function SetEffectiveThetaJA(ThetaJA As Double, OverRide As
Boolean) As Boolean
```

Scripting XPE

Microsoft Excel capabilities described in the previous paragraphs can be accessed from any framework with access to the COM interface. This Component Object Model (COM) is a binary interface standard for software that enable interprocess communications in a large range of programming languages (Visual Basic, Perl, Java…). The following examples illustrate how you can set XPE environment parameters, run calculations and read or export results from different languages.

Visual Basic Scripting Example

This simple example opens XPE, then export results into a text power report using the Visual Basic scripting language.

```
Dim XPE As Workbook
XPEfilename = "C:\\Power\\7_Series_XPE_13_1.xls"

On Error Resume Next
Set XPE = Workbooks(XPEfilename)
   ' Opening XPE
   On Error GoTo 0
   If (XPE Is Nothing) Then
      Set XPE = Application.Workbooks.Open(XPEfilename,
UpdateLinks:=vbFalse, ReadOnly:=vbTrue)
      If XPE Is Nothing Then ' Open failed
         MsgBox ("XPE Open Failed: " & XPEfilename & "Err=" & Err)
         Exit Function
      End If
   End If
' Set Vccint voltage
XPE.Sheets("Summary").Range("VCCINT").Value = myVccint
TotalPower = XPE.Sheets("Summary").Range("TOTAL_POWER").Value
' Export XPE results into a text power report
XPESub = "'" & XPE.Name & "'!" & "ThisWorkBook.GeneratePowerReportFile"
Application.Run(XPESub, FileName)
```

Perl Scripting Example

This simple example opens XPE then export results into a text power report using Perl scripting language.

```
use Win32::OLE;
use Win32::OLE::Const 'Microsoft Excel';

my $myXPEfilename = "C:\\Power\\7_Series_XPE_13_1.xls";

# Opening XPE
my $Excel = Win32::OLE->GetActiveObject('Excel.Application')
    || Win32::OLE->new('Excel.Application', 'Quit');
my $Book = $Excel->Workbooks->Open($myXPEfilename);
# Export XPE results into a text power report
$Excel->Run("ThisWorkBook.GeneratePowerReportFile",
"$path/${design}.pwr");
```

Conclusion

The ability to estimate power consumption in a design is imperative for efficient part selection, board design, and system reliability.

The XPower Estimator tool with its up to date power models and ease of use features is meant to guide and simplify design utilization entry. Although gathering FPGA utilization data may seem difficult in the early design development phases, with a little thought and using XPE, accurate power estimations can be derived. XPE simplifies device selection and helps parallel development of the FPGA logic and the Printed Circuit Board. Finally, XPE helps exploration of alternative implementation and resource configuration when supply power or thermal budgets are exceeded.

Appendix A

Additional Resources

- To download the XPE spreadsheets, see the Power Solutions webpage on the Xilinx website at:

  http://www.xilinx.com/power

- To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

  http://www.xilinx.com/support

- The following are especially pertinent to the subject of this User Guide.
  - *Power Methodology Guide (UG786)*
  - *Seven Steps to an Accurate Worst-Case Power Analysis Using Xilinx Power Estimator (XPE) (WP353)*
  - *Test Boards for Area Array Surface Mount Package Thermal Measurements*
  - Descriptions of the resources available in an FPGA can be found under **FPGA Device Families** at http://www.xilinx.com/documentation.

- ***ISE Design Suite: Installation and Licensing Guide*** *(UG798)*: http://www.xilinx.com/support/documentation/sw_manuals/xilinx13_1/iil.pdf
- ***ISE Design Suite 13: Release Notes Guide*** *(UG631):* http://www.xilinx.com/support/documentation/sw_manuals/xilinx13_1/irn.pdf
- **Xilinx® Documentation**: http://www.xilinx.com/support/documentation
- **Xilinx Global Glossary**: http://www.xilinx.com/support/documentation/sw_manuals/glossary.pdf
- **Xilinx Support**: http://www.xilinx.com/support.htm