Quick Front-to-Back Overview Tutorial

PlanAhead Software

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XILINX®

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Quick Front-to-Back Overview Tutorial

This tutorial provides a quick introduction to some of the capabilities and benefits of using the Xilinx® PlanAhead™ software. PlanAhead software can be used during various stages of the design process for a variety of purposes.

Many of the PlanAhead software analysis features are covered in more detail in other tutorials. Not every command or command option is represented here. This tutorial uses the features contained in the PlanAhead software product, which is bundled as a part of the ISE® Design Suite.

Software Requirements

The PlanAhead software is installed with ISE Design Suite software. Before starting the tutorial, be sure that the PlanAhead software is operational, and that the tutorial design data is installed.

For installation instructions and information, see the *ISE Design Suite: Installation and Licensing Guide (UG798)* at http:/ / www.xilinx.com/ support/ documentation/ sw_manuals/ xilinx13_3/ iil.pdf.

Hardware Requirements

Xilinx recommends a minimum of 2 GB of RAM when using the PlanAhead software on larger devices. For this tutorial, a smaller xc6vlx75t design is used, and the number of designs open at one time is limited. Although 1 GB is sufficient, it can impact performance.

Tutorial Design Description

The small sample design used throughout this tutorial consists of a small design called `bft`. There are several VHDL and Verilog source files in the bft design.

The design targets an xc6vlx75T device. A small design is used to allow the tutorial to be run with minimal hardware requirements and to enable timely completion of the tutorial, as well as to minimize the data size.

Locating Tutorial Design Files

1. Download the PlanAhead_Tutorial.zip file from the Xilinx website:

   http:/ / www.xilinx.com/ support/ documentation/ dt_planahead_planahead13-3_tutorials.htm

2. Extract the zip file contents into any write-accessible location.

   The unzipped PlanAhead_Tutorial data directory is referred to in this tutorial as the *<Extract_Dir>*.

The tutorial sample design data is modified while performing this tutorial. A new copy of the original PlanAhead_Tutorial data is required each time you run the tutorial.

Step 1: Creating a New Project

PlanAhead software enables several types of projects to be created depending on where in the design flow the tool is being used. Register Transfer Level (RTL) sources can be used to create a project for development and analysis, synthesis, implementation and BIT file creation.

Open the software:

- On Windows, select the **Xilinx PlanAhead 13** desktop icon or **Start > Programs > Xilinx ISE Design Suite 13.3 > PlanAhead > PlanAhead**.
- On Linux, change the directory to `<Extract_Dir>/PlanAhead_Tutorial/Tutorial_Created_Data`, and type **planAhead**.

The PlanAhead Getting Started Help page opens.

Figure 1: Getting Started Page

The PlanAhead Getting Started page contains links to open or create projects, and view the documentation.

Creating a new RTL Project Called Project_1

This step uses some RTL Source Files in the `<Extract_Dir>\PlanAhead_Tutorial\Sources\hdl` directory.

1. Select the **Create New Project** link on the Getting Started page.

   The Create a New PlanAhead Project confirmation dialog box opens.

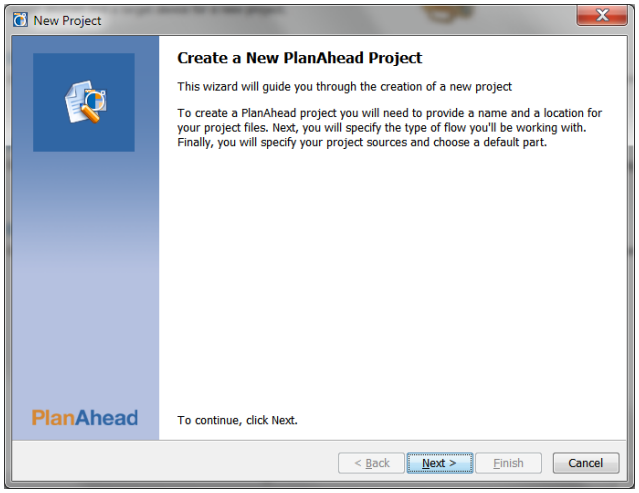

Figure 2: New Project Overview

2. Click **Next**.

   The Project Name page opens.

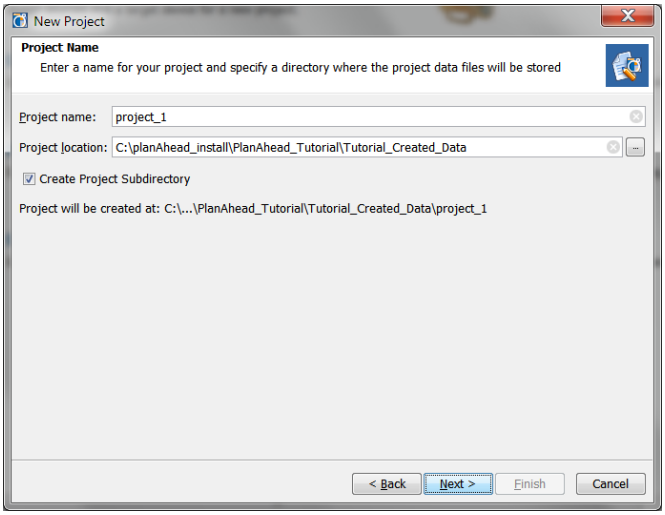

Figure 3: New Project Wizard: Project Name Page

3. Enter `<Extract_Dir>\PlanAhead_Tutorial\Tutorial_Created_Data`.
4. Use the default Project name: **project_1**, then click **Next**.

The Design Source page opens.

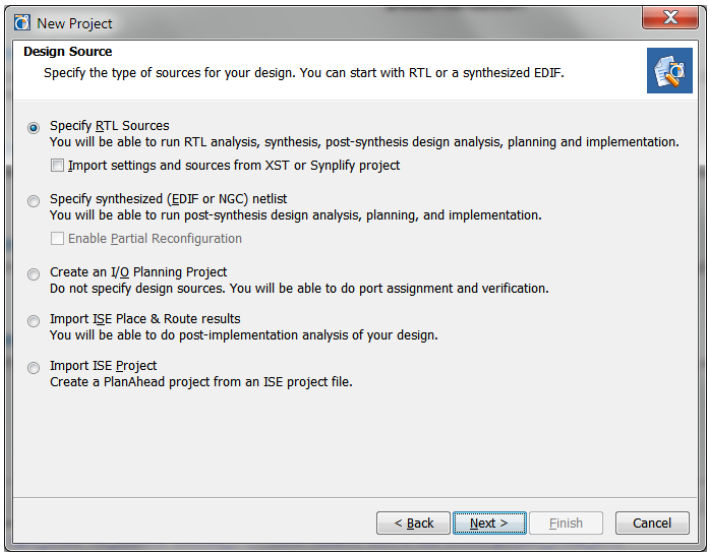

Figure 4: New Project Design Source Dialog Box

5. Click the **Specify RTL Sources** option, and then click **Next**.

   The Add/ Create Sources page opens.

Adding Directories, Files, and the VHDL Library and Source Type

1. Click the **Add Files** button and browse to the following directory:

   `<Extract_Dir>/PlanAhead_Tutorial/Sources/hdl`
2. Press the **Ctrl** key to select **async_fifo.v**, **bft.vhdl**, **bft_tb.v**, and **FifoBuffer.v**, and click **OK**.
3. Click the **Add Directories** button, and browse to select the following directory:

   `<Extract_Dir>/PlanAhead_Tutorial/Sources/hdl/bftLib`.
4. Click on the **work** entry in the Library field for bftLib, and type **bftLib**.
5. For the `bft_tb.v` file, select **Simulation only** under the HDL Source for column.
6. If needed, click these two checkboxes to select **Copy Sources into Project**, and **Add Sources from Subdirectories**.

7. Verify that the page looks like the following figure.

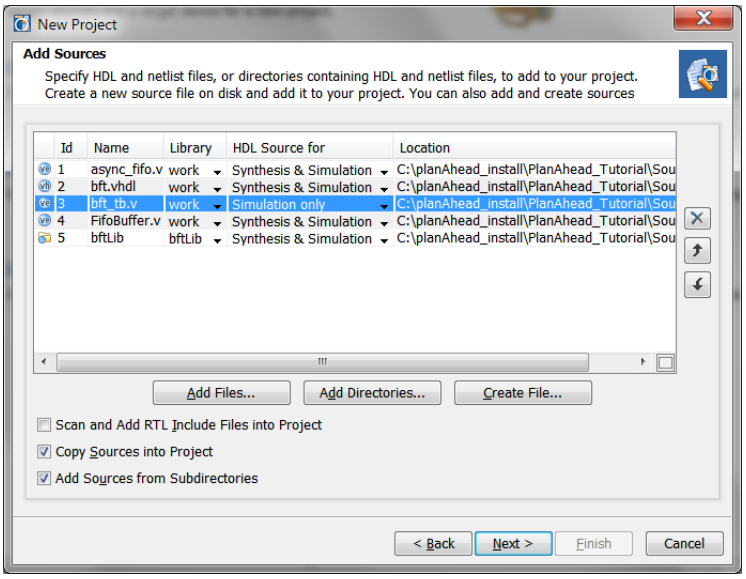

Figure 5: New Project : Selecting Sources to Add to the Project

8. Click **Next**.

   The Add Existing IP page opens. You can select existing IP (Intellectual Property) from CORE Generator™ software .xco project files. However, this tutorial does not include importing IP into the project.

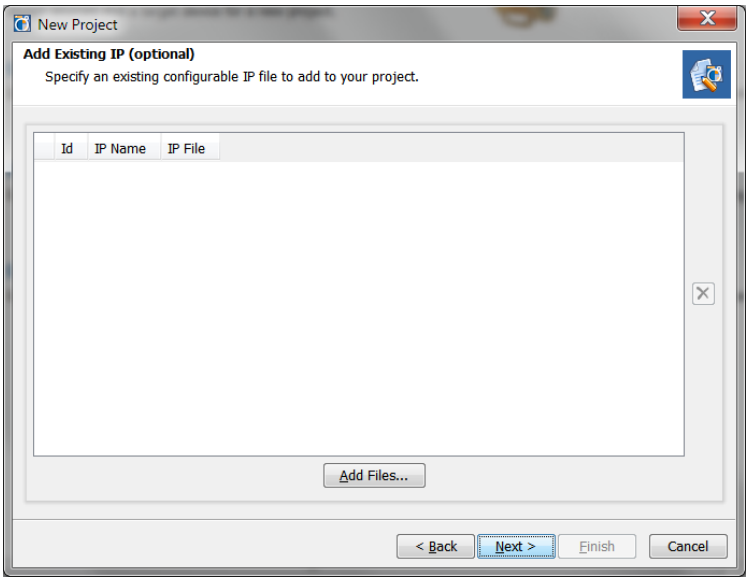

Figure 6:Adding Custom as Sources

9. Click **Next.**

The Constraints Files page opens.

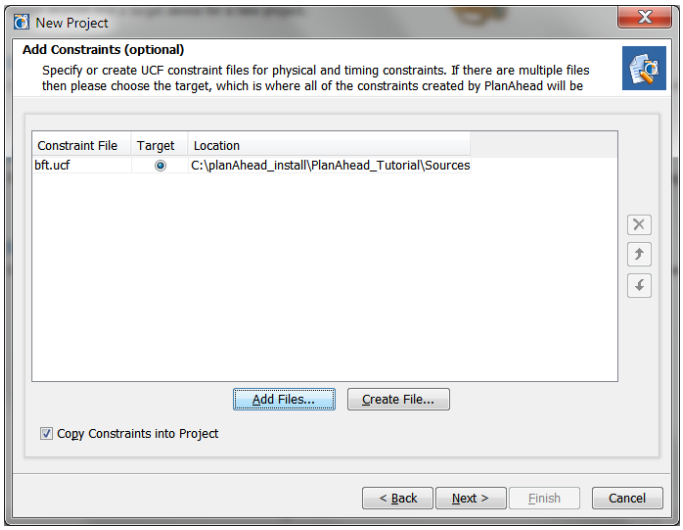

Figure 7: New Project: Adding Constraint Files

Adding a Constraint File

1. Click the **Add Files** button, browse to select the following file:

   `<Extract_Dir>/PlanAhead_Tutorial/Sources/bft.ucf`

2. Click **OK**.

2. Click **Next**.

The Default Part page opens.

Selecting a Default Part

1. In the Filter section, click the Family pull-down menu and select **Virtex6**.

   Notice the list is filtered to only show Virtex®-6 devices.

2. Click the Sub-Family pull-down menu and select **Virtex6 LXT**.

   Notice the list is filtered to only show Virtex-6 LXT devices.

3. In the Search field, type **75t**.

   Notice the 75t devices listed.

4. Select the **xc6vlx75tff484-1** device, and click **Next**.

5. Review the New Project Summary page, and click **Finish**.

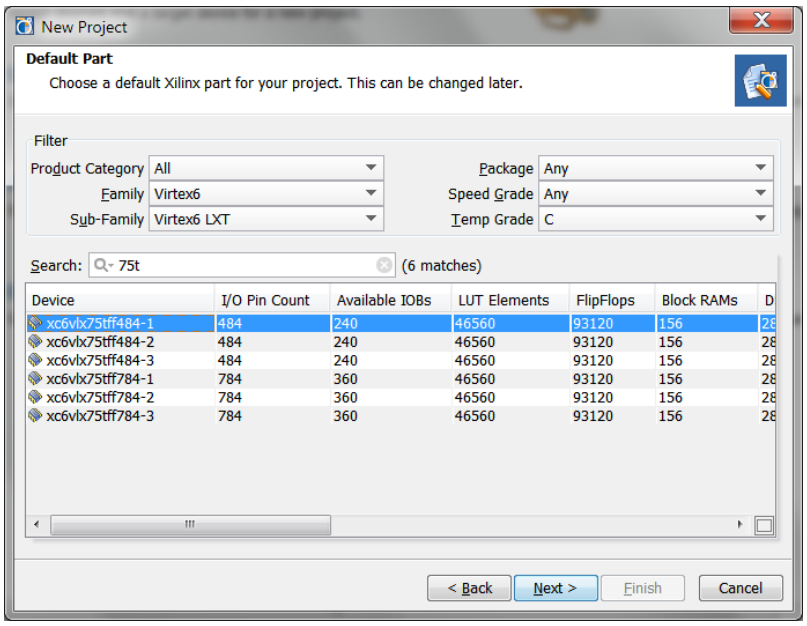

Figure 8: New Project: Selecting a Family and Default Part

The PlanAhead environment opens. Note the Flow Navigator, which is located on the left edge. It will be used throughout the rest of the tutorial to explore and implement the design.

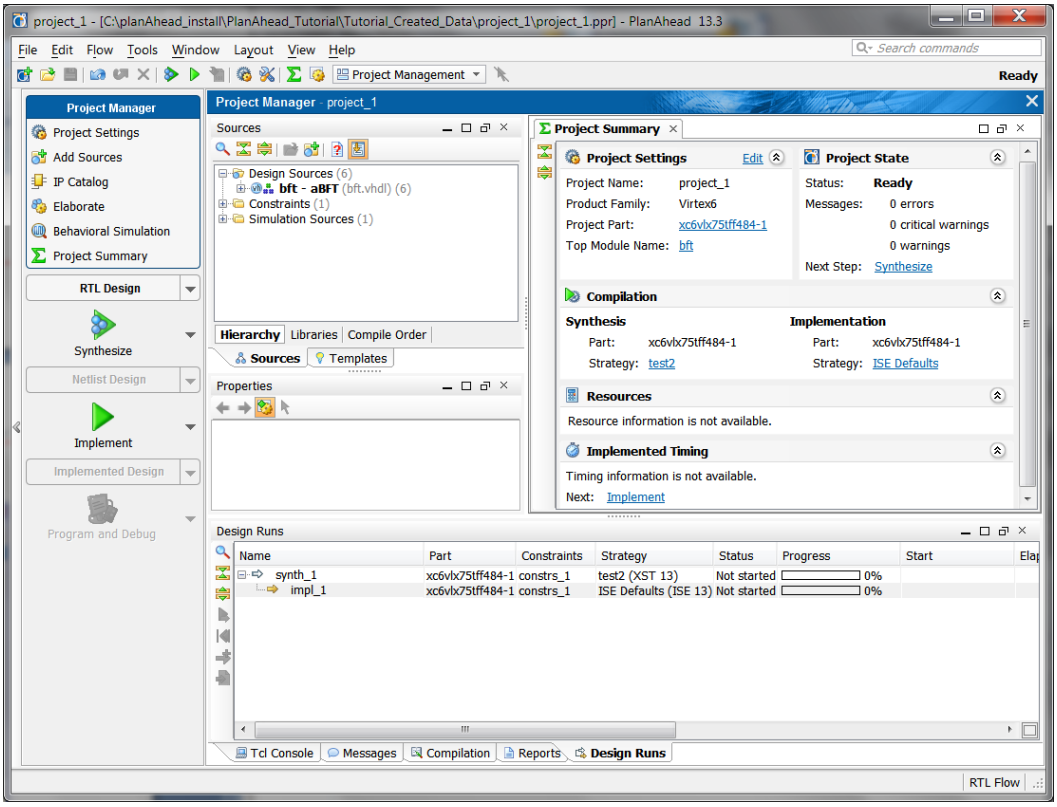

Figure 9: PlanAhead Environment

Step 2: Using the Sources View and the Text Editor

The PlanAhead software allows different file types to be added as design sources including Verilog, VHDL, NGC format cores, UCF/ NCF constraint files, and specific simulation sources. The files display by Hierarchy, Library or Compile Order in the Sources view. A text editor is supplied to create or develop RTL sources. Third party text editors can also be configured.

Exploring the Sources View and Project Summary

1. Examine the information in the Project Summary. More information displays as the design progresses.
2. Examine the Sources view. Scroll or resize the view, if needed.

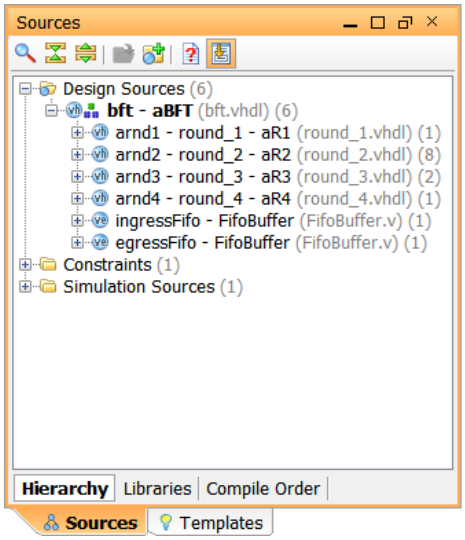

Figure 10: Viewing Sources

The Design Sources folder helps keep track of VHDL and Verilog source files. Notice the design hierarchy is displayed by default. In the Libraries tab, sources are grouped by file type, while the Compile Order tab shows the file order used for synthesis.

Exploring the Sources View Commands and Text Editor

1. Select one of the VHDL sources in the Sources view.
2. Right-click to review the commands available in the Sources view popup menu.
3. Select **Open File**, and use the scroll bar to browse the text in the Text Editor.

   Note: Alternatively, you can double-click on source files in the Sources view to open them in the Text Editor.
4. With the cursor in the Text Editor, right-click and select **Find in Files**.

   The Find in Files dialog box opens with various search options.

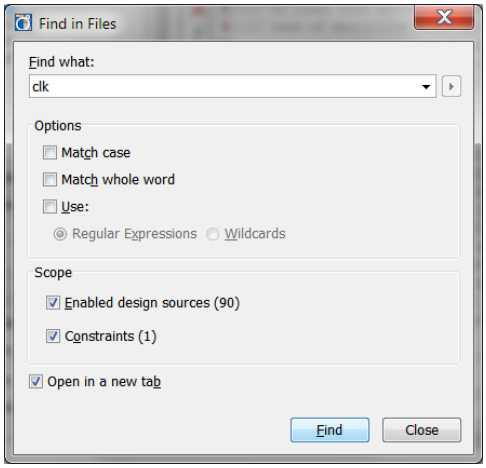

Figure 11: Using the Find in Files Command

5. Type **clk**, and click **Find**.

   The Find in Files view displays in the messaging area at the bottom of the PlanAhead environment.

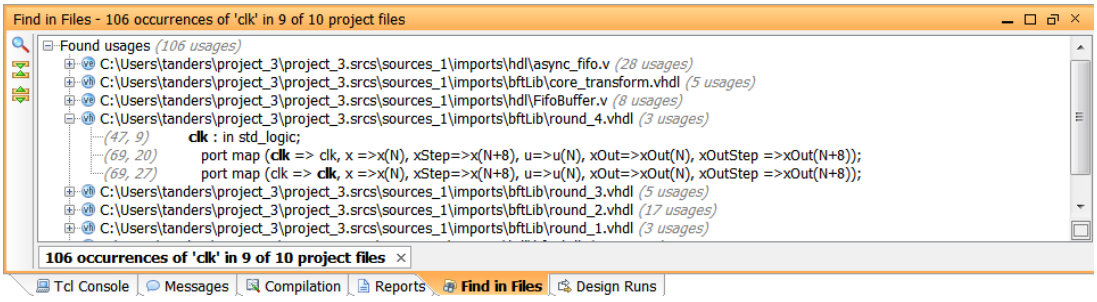

Figure 12: Viewing the Find in Files Results

6. In the Find in Files view, expand and select one of the occurrences of clk and notice that the Text Editor now displays the file and occurrence.
7. Close the **Find in Files – Occurrences** view.
8. Close each of the open RTL file tabs in the Text Editor.

The PlanAhead software also includes an RTL analysis and IP customizing environment. This environment is covered in the *PlanAhead Tutorial: RTL Design and IP Generation (UG675)*.

You can click the RTL Design button in the Flow Navigator to quickly explore the features. The RTL design is elaborated first, which enables various analysis views including an RTL Netlist, Schematic, Graphical Hierarchy, and estimated resource statistics. The views have a "cross-select" feature, which allows you to debug and optimize the RTL.

The Xilinx IP Catalog provides access to the Xilinx CORE Generator™ software tool to generate IP. You can sort and search the Catalog in a variety of ways. IP can be customized, generated, and instantiated. There are also several RTL Design Rule Checks (DRCs) to check for areas to improve performance or power on the RTL.

Step 3: Simulating the Design

The PlanAhead software is integrated with the Xilinx ISim logic simulation environment. The PlanAhead software enables you to add and manage synthesis sources in the project. You can configure simulation options and create and manage various simulation source sets. You can launch behavioral simulation prior to synthesis using RTL sources and launch timing simulation post-implementation.

The Behavioral Simulation command configures and launches a single ISim run, which is the basic flow used in this tutorial. It can be accessed in the Flow Navigator view on the left side of the PlanAhead environment, shown in the following figure.

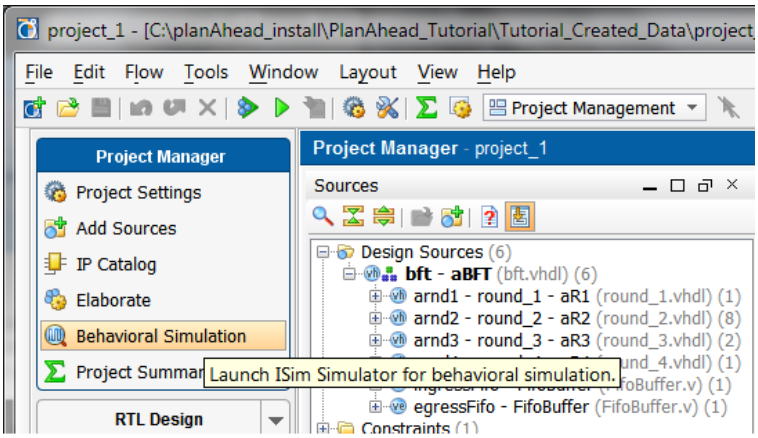

Figure 13: Launching Behavioral Simulation

The Behavioral Simulation command is also available in the RTL Design.

Exploring Simulation Options and Launching Behavioral Simulation

1. In the Flow Navigator, select **Behavioral Simulation**.

   The Launch Behavioral Simulation dialog box opens.

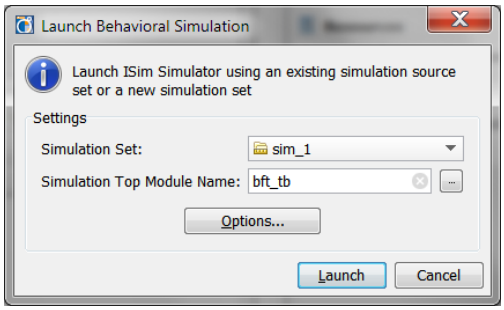

Figure 14: Launch Behavioral Simulation Dialog Box

2. If bft_tb is not specified as the **Simulation Top Module Name**, click the browse button ... .
3. Select **bft_tb**, and click **OK**.
4. Click the **Options** button.

   The **Simulation Options** dialog box opens.

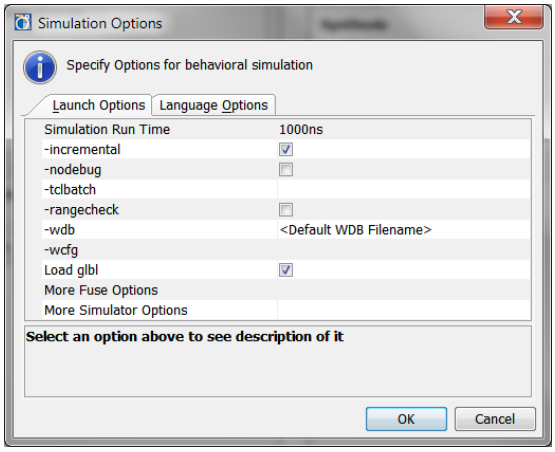

Figure 15: Simulation Options Dialog Box

   Notice the simulation launch options.

5. Click the **Language Options** tab, and examine the language options, and click **OK**.
6. Click **Launch** to invoke the ISE Simulator (ISim) simulation environment.

   The ISim simulation environment opens.

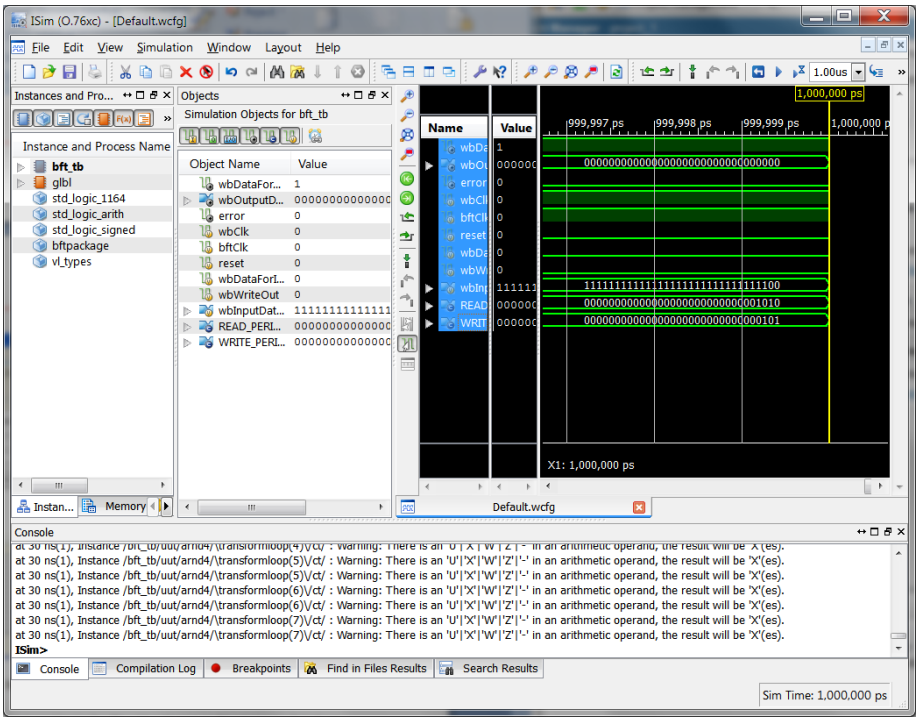

Figure 16: ISim Simulation Environment

Editing source files in the ISim environment results in the PlanAhead source files being updated as well. The two tools are referencing the same sources. Refer to the *ISE Simulator (ISim) In-Depth Tutorial (UG682)*, for information about simulation using ISim.

7. In ISim, select **File > Exit** and click the **Yes** button when prompted to close ISim.

Step 4: Synthesizing the Design

The PlanAhead software enables one or more synthesis runs to be configured, launched, and monitored, either sequentially or simultaneously.

The Synthesize command configures and launches a single run which is the basic flow used in this tutorial. It can be accessed in the Flow Navigator view on the left side of the PlanAhead Environment.

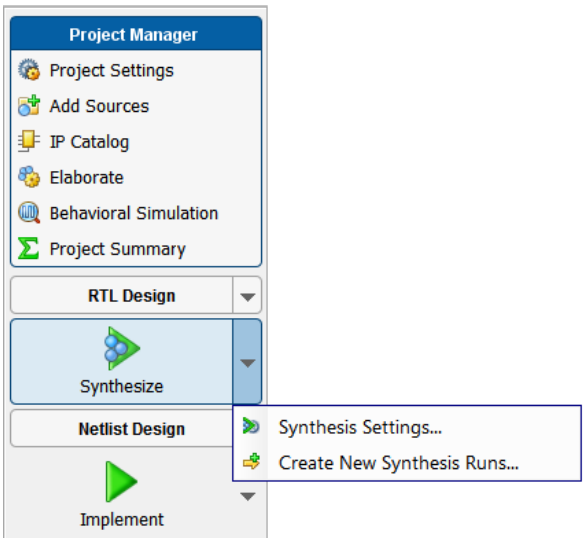

Figure 17: Flow Navigator Synthesize Drop Down Menu

The Flow Navigator launches all major design compilation processes including synthesis, implementation, and generate bitstream. It also lets you open the compiled RTL Design, the synthesized Netlist Design, and the Implemented Design results. These are optional steps to enable design analysis and constraints assignment at each phase of the design process.

Exploring Synthesis Options, Launching Synthesis, and Monitoring a Run

1. In the Flow Navigator, expand the drop-down menu next to the Synthesize button, and select **Synthesis Settings**.

   The Synthesis Settings dialog box opens.

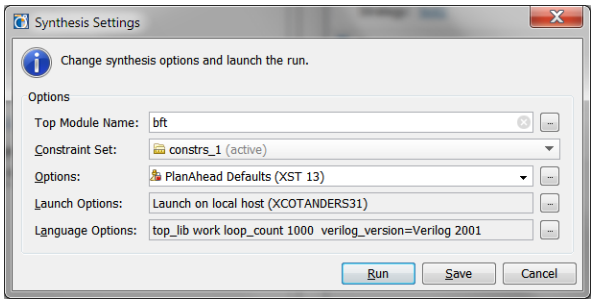

Figure 18: Synthesis Settings Dialog Box

2. If needed, click the Top Module Name field and type **bft**.
3. Use the default Part and Constraint Set.
4. Select the Options: browse button [...] to display the Synthesis Options dialog box.

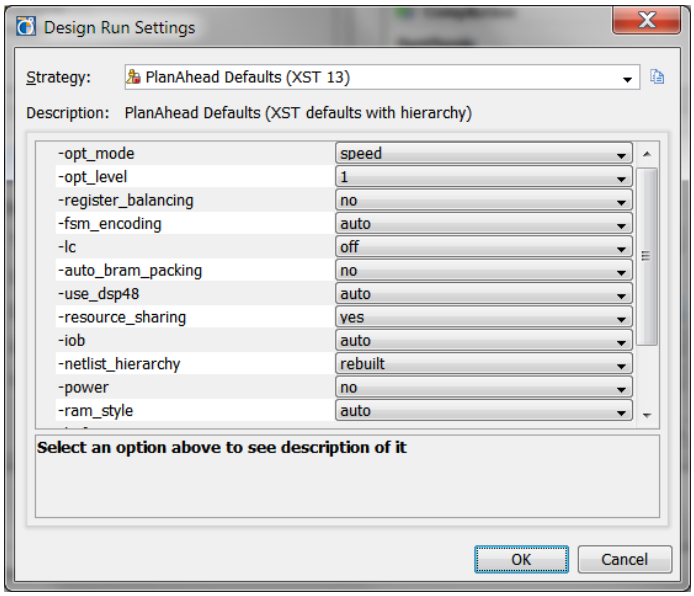

Figure 19: Synthesis Options Dialog Box

5. Review the available options.
6. Click the Strategy drop-down menu, located at the top of the Design Run Settings dialog, review the available Synthesis Strategies, and click **Cancel** to close the dialog.
7. Select the Launch Options browse button [...] to open the **Specify Launch Options** dialog box.

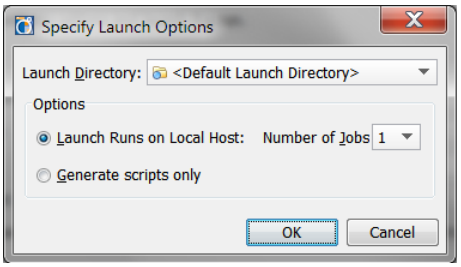

Figure 20: Selecting Synthesis Launch Options

8. Review the options, select **the Launch Runs on Local Host**, and click **OK**.
9. In the **Synthesis Settings** dialog box, click **Run** to launch the run.

   Notice the Status bar in the upper right corner displays Synthesizing (XST), which indicates that synthesis is now running. Clicking the Cancel button halts the synthesis run and removes run data.

   The Compilation view displays the output messages from the ISE commands, and the Messages view displays a filtered list of Warnings and Errors. Clicking on the Synthesis messages in the Messages view opens the RTL file and displays the corresponding line of RTL code that it is referencing.

Opening the Netlist Design

1. Allow the synthesis run to complete, and then click **Open Netlist Design** in the **Synthesis Completed** dialog box.
2. If prompted, click **Yes** to close the RTL Design.

   The PlanAhead Design Planner view layout environment displays with the synthesized netlist, target part, and active constraint set applied.

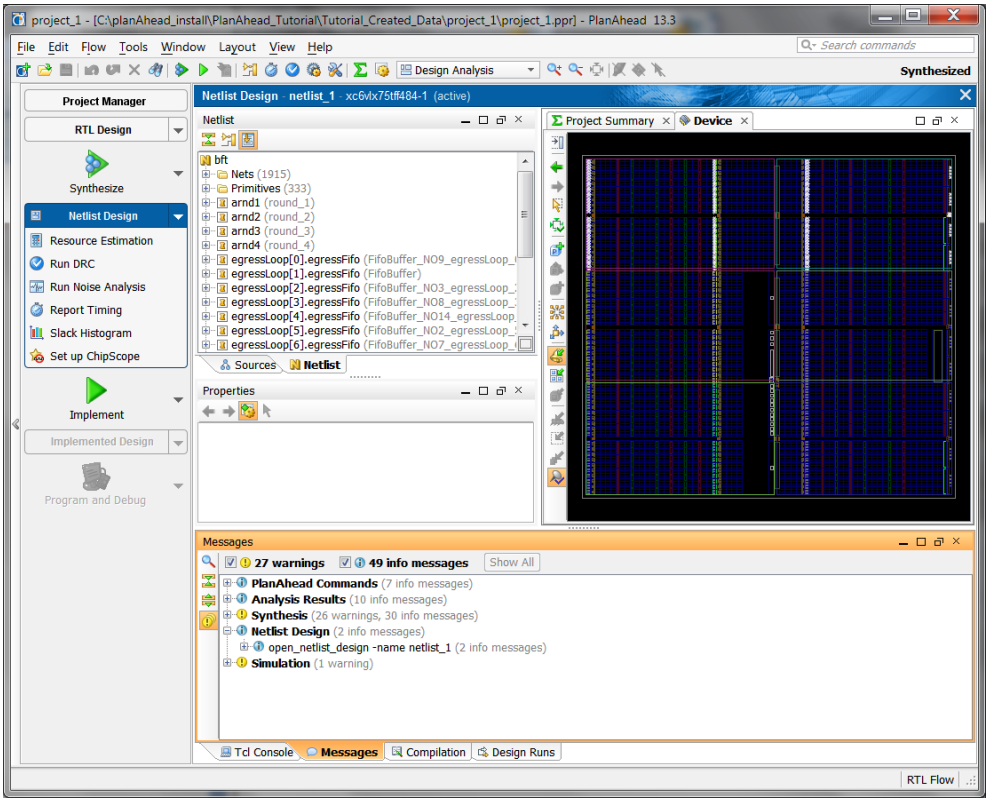

Figure 21: Opening the Netlist Design

Note: Clicking the Netlist Design button in the Flow Navigator also opens the Netlist Design environment. There are options in the pull-down menu for opening designs with different run results, constraints, or target devices.

The PlanAhead software provides a powerful design analysis and floorplanning environment to explore and experiment with the design. Using the PlanAhead analysis and floorplanning environment, you can experiment with various devices, timing constraints, or placement constraints. These capabilities are covered in other PlanAhead tutorials.

3. Select **I/O Planning** from the pull-down menu in the toolbar at the top of the PlanAhead environment.

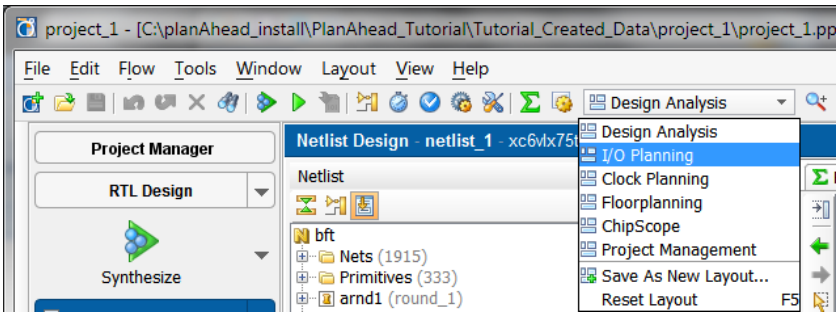

Figure 22: Opening the I/O Planning View Layout

There are several view layouts available to help you perform different design tasks. For example, the I/ O Planning layout provides views to enable I/ O pin exploration and constraint assignment. The Design Analysis layout provides views to analyze the logic in the design and apply constraints. You can also create and display custom layouts. The last layout selected will be used by default the next time that design is opened.

4. Examine the various views and information presented, for example the Package view in the workspace and the I/ O Ports view.

Note: The PlanAhead software includes an I/O planning environment. This environment is covered in the PlanAhead Tutorial: I/O Pin Planning (UG674). You can perform I/O pin planning prior to synthesis in the RTL Design or after synthesis in the Netlist Design. After synthesis, the features expand to enable proper I/O and clock planning with related DRCs.

5. Select **Design Analysis** from the same pull-down menu in the toolbar.

Viewing the XST Report Log File

1. Click the **Reports** view tab at the bottom of the PlanAhead environment.

   Note: If there is no view tab available, select **Window > Reports**.

2. Double-click the **XST Report** to view the XST report in the Workspace.
3. To examine the XST report scroll, through the report.
4. Close the XST Report by clicking on the **X** in the view tab.

   The PlanAhead software also includes a ChipScope™ debug core insertion environment. This environment is covered in the *PlanAhead Tutorial: Debugging with ChipScope (UG677)*. You can use the PlanAhead features to explore and select logic signals to debug. The debug cores can be configured, implemented, and automatically added into the top level design netlist. The cores are also maintained through design netlist iterations.

   You can close the Netlist Design environment after your analysis and constraint definition completes. This helps preserve system memory and avoids having multiple editing environments open simultaneously. You can use the Close button in the view banner or the pull-down menu on the Netlist Design button in the Flow Navigator to close the Netlist Design. For the purposes of this tutorial, it is left open.

Step 5: Implementing the Design

The PlanAhead software provides the flexibility for experimenting with implementation options. You can apply multiple implementation Strategies to multiple runs to find the best performing results.

Exploring Implementation Options, Launching Implementation, and Monitoring a Run

1. In the Flow Navigator, expand the drop-down menu next to the Implement button and select **Implementation Settings**.

   The Implementation Settings dialog box opens.

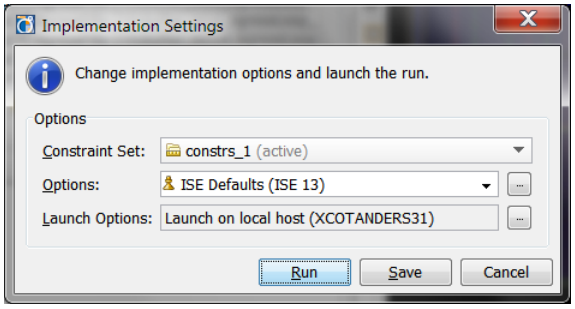

Figure 23: Implementation Settings Dialog Box

2. Use the default Constraint Set.
3. Select the Options: browser button ... to display the **Implementation Options** dialog box.

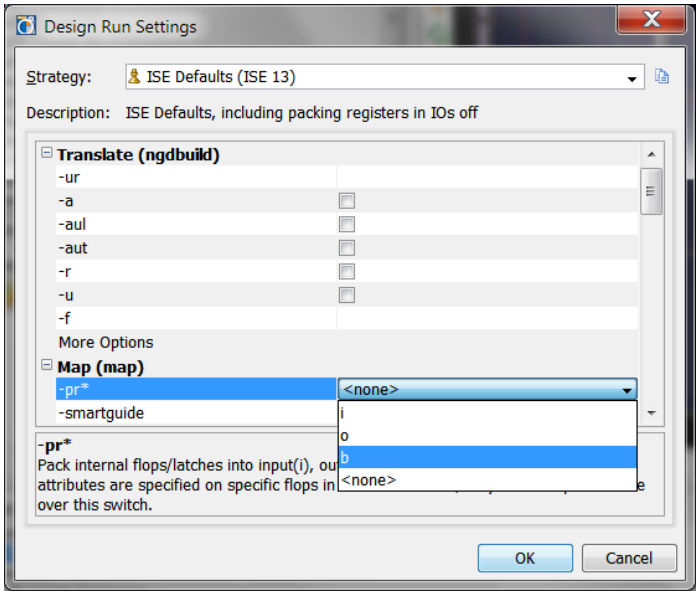

Figure 24: Implementation Options Dialog Box

4. Review the available options. Select the **Strategy** drop-down menu, review the available Implementation Strategies, and click **Cancel**.

5. In the Implementation Settings dialog box, click **Run** to launch the run.

   Notice the Status in the upper right corner displays Implementing (NGDBuild), indicating that ISE implementation is now running.

   The Compilation view displays the output of the ISE commands, and the Messages view displays a filtered list of Warnings and Errors.

6. After the Run completes, select the **Open Implemented Design** option in the Implemented Design dialog box, and click **OK.**

7. Click **Yes** to close the Netlist Design before opening the Implemented Design.

Step 6: Analyzing the Results

The PlanAhead software enables placement and timing results to be imported quickly for analysis from any of the completed runs. The PlanAhead software imports placement and displays it in the form of "unfixed" LOC placement constraints. The TRACE timing results display in the Timing Results view.

Note: For more information about Design Analysis and Floorplanning, see PlanAhead Tutorial: Design Analysis and Floorplanning for Performance (UG676).

Opening the Implemented Design and Briefly Examining the Results

The PlanAhead environment displays with the Implemented Design loaded.

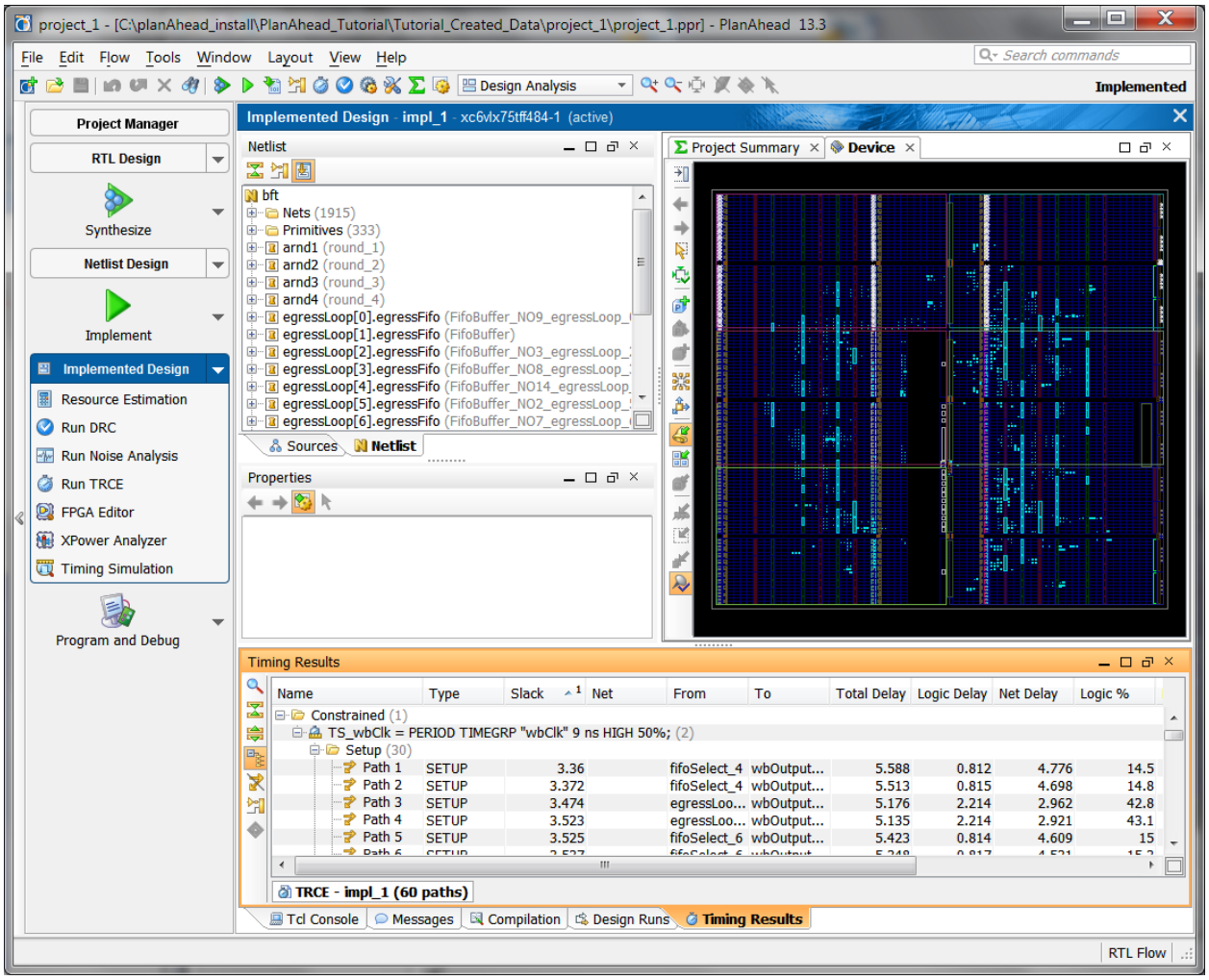

Figure 25: Opening the Implementation Results

Clicking the Implemented Design button in the Flow Navigator also opens the Implemented Design environment. There are options in the pull-down menu for opening Implemented Designs with different run results.

Notice the placement is imported into the Device view and the TRACE timing results are displayed in the Timing Results view. Your results might differ from the figure above.

Note: If there is no view tab available, select **Window > Reports**.

1. Examine the Map report by scrolling through the report.
2. Close the Map report by clicking the **X** button in the Workspace view tab.
3. In the Device view, click the **Hide/Show I/O Nets** button to turn on the I/ O connectivity.
4. In the Device view, click the **Hide/Show I/O Nets** button to turn off the I/ O connectivity.
5. In the Timing Results view, select the top timing path.

   The path is highlighted in the Device view and the logic objects on the path are selected in other views.

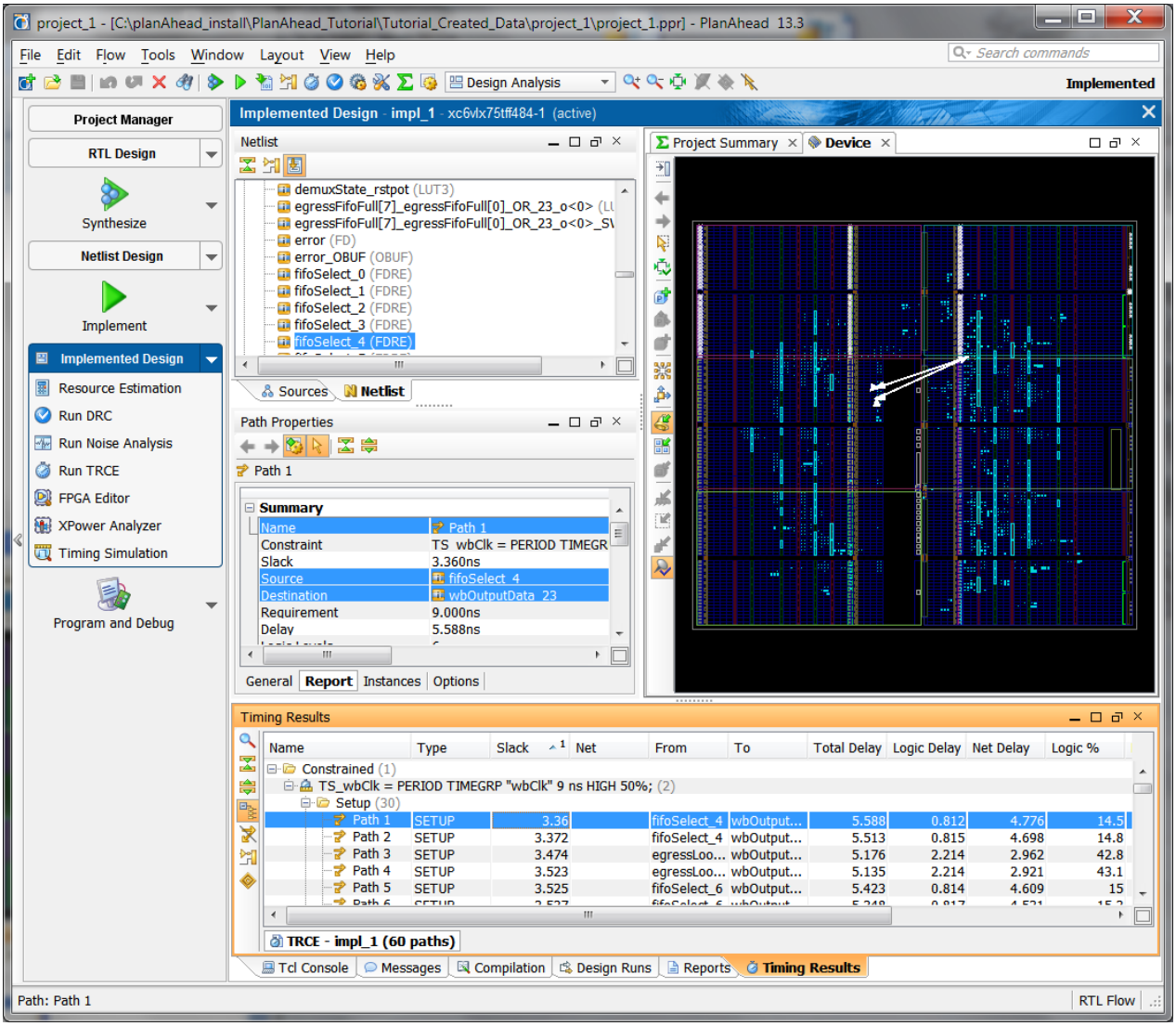

Figure 26: Highlighting Timing Paths from the Implementation Results

6. In the Path Properties view banner, click the **Maximize** button .

The Path Properties view displays in full screen.

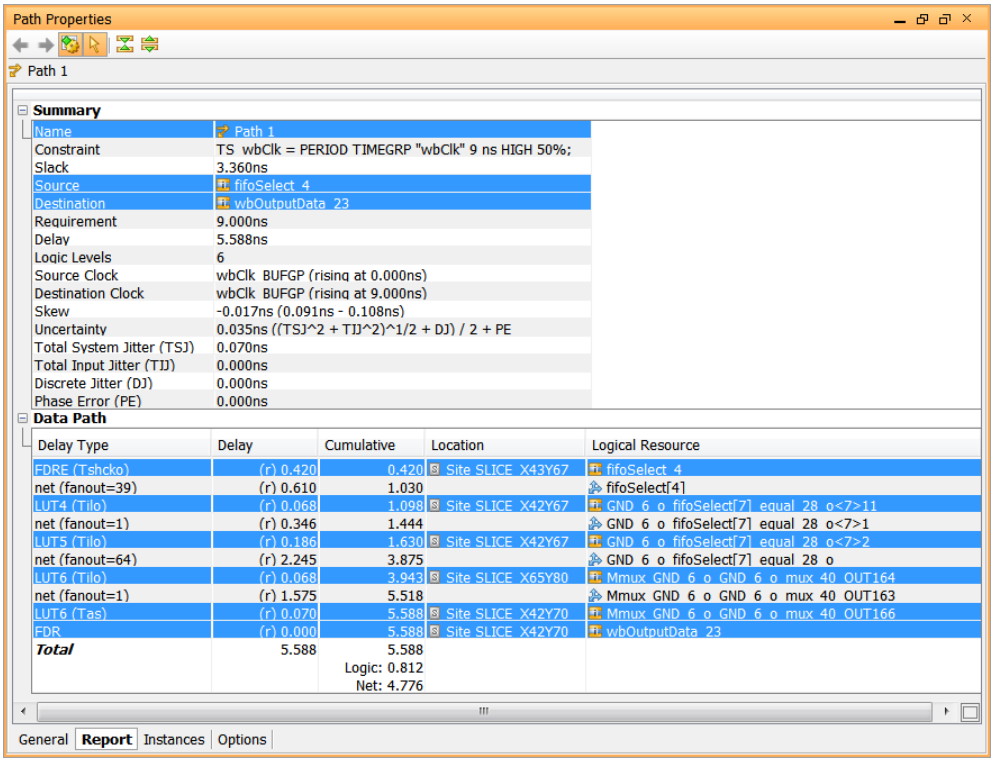

Figure 27: Viewing Path Properties

Notice the Path Properties report looks very similar to the TRACE report. Selecting any of the sites or locations (e.g. SLICE_X43Y67) selects the logic object or site for viewing in Device or other view window.

7. Click the **Restore** button in the Path Properties view banner to bring the view back to the original location.

8. In the Timing Results view, click the **Schematic** button from the view toolbar or select the command from the popup menu.

The Schematic view opens.

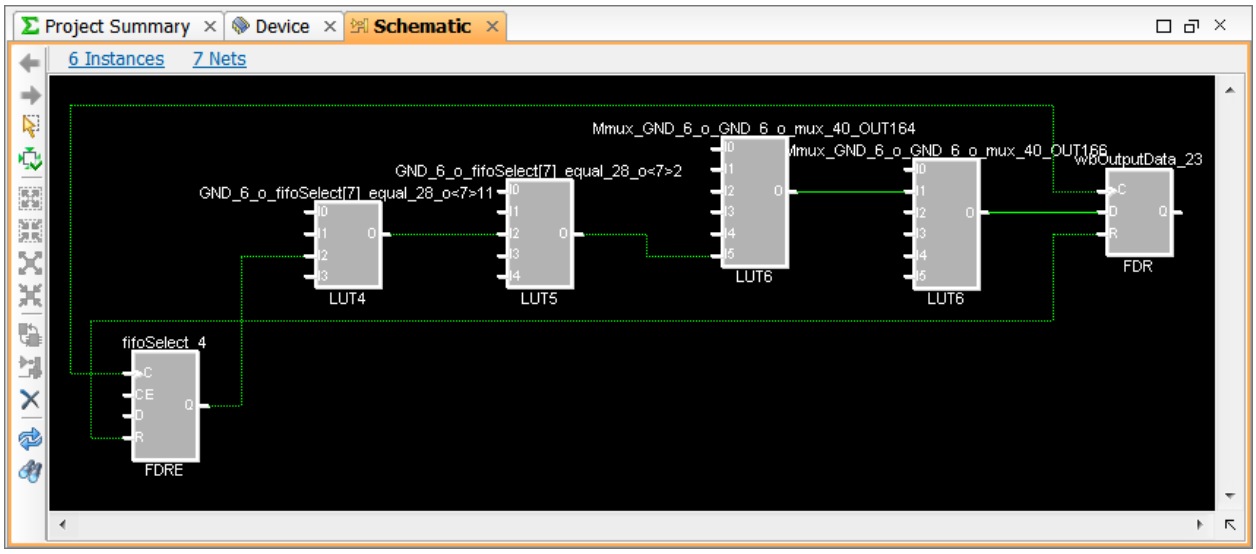

Figure 28: Viewing Timing Paths in the Schematic

Notice that the schematic displays the logic objects on the selected paths as well as the logical hierarchy. This helps identify logic modules for floorplanning. It also displays links to find the Nets and Instances displayed in the current view.

Note: The PlanAhead software also includes a design analysis and floorplanning environment. This environment is covered in the *PlanAhead Tutorial: Design Analysis and Floorplanning for Performance (UG676)*. You can use the analysis features to explore the design or the implementation results. You can apply constraints aimed at better and more consistent results.

9. Close the Schematic view.

Step 7: Creating the Bitstream File

Running Generate Bitstream to Create a BIT file for the Design

1. Click the Generate Bitstream button,  or, select Flow > Generate Bitstream.

   The Generate Bitgen dialog box opens.

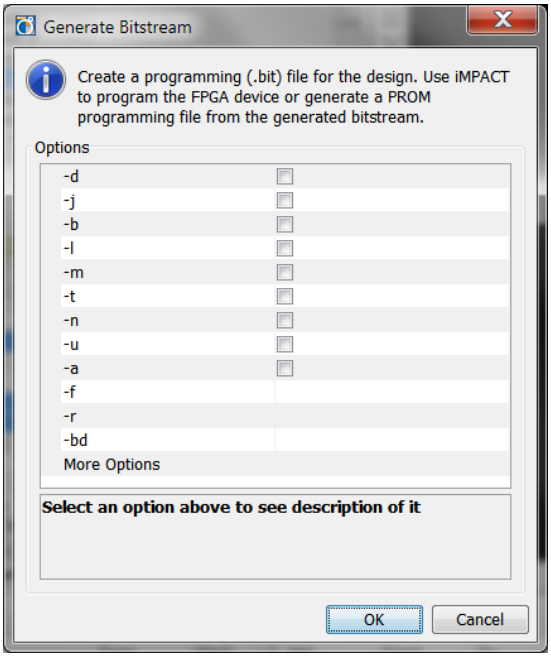

Figure 29: Generating Bitstream File

2. Select **OK**.

   The Generating Bitstream progress bar opens. When the Bitstream is generated, a dialog box opens to inform you that the bitstream was successfully generated. Click the OK button to dismiss it.

3. In the Flow Navigator, click the **Program and Debug** button to expand the menu, and notice that you can launch ChipScope Analyzer and the iMPACT programming tool after a bitstream file is generated.

Reviewing the Project Summary for the Implemented Design

1. Select the **Project Summary** view tab, and review the information presented.
2. Close the PlanAhead software by selecting **File > Exit**, click **Yes** to save, and **OK**.

Conclusion

In this tutorial, you:

- Used a small PlanAhead RTL project to step quickly through the basic PlanAhead design flow, starting by creating an RTL project, and exploring RTL sources in the Text Editor.
- Reviewed the simulation options and launched ISim.
- Reviewed the various synthesis run options, ran synthesis.
- Imported the results by opening the Netlist design.
- Explored implementation options
- Ran implementation.
- Monitored run results and viewed command report files.
- Imported run results, and analyzed a timing path.
- Created a bitstream file.