Design Analysis and Floorplanning Tutorial

PlanAhead Design Tool

UG676 (v14.5) April 10, 2013

This tutorial document was last validated using the following software version: ISE Design Suite 14.5

If using a later software version, there may be minor differences between the images and results shown in this document with what you will see in the Design Suite.

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Revision History

Date	Version	Revision
04/10/2013	14.5	Validated with Release.

Table of Contents

Design Analysis and Floorplanning Tutorial

Overview

This tutorial introduces some of the capabilities and benefits of using the Xilinx® PlanAhead™ software for designing high-end FPGAs. The document contains a series of step-by-step exercises that highlight methods to achieve and maintain better performing designs in less time. The steps detail the following:

- Pre-implementation design and analysis capabilities
- Implementation exploration features
- Implementation results floorplanning

Note: This tutorial covers a subset of the features of the PlanAhead software product bundled with the ISE® Design Suite. Additional features are covered in detail in other tutorials.

Tutorial Objectives

This tutorial takes you through the various analysis, floorplanning, and implementation features of the PlanAhead software. The exercises cover the following topics:

- Analyze device utilization statistics to target alternate devices and choose the optimal device.
- Run Design Rule Checks (DRC) to quickly resolve constraint conflicts that would otherwise cause implementation errors.
- Use the Netlist, Logic Hierarchy, and Schematic views to explore logic.
- Perform a quick estimation of timing performance to assess design feasibility and identify potential problem areas.
- View, modify, or create constraints in the design.
- Analyze the design hierarchical connectivity and data flow, as well as identify critical logic connectivity and clock domains.
- Floorplan timing-critical logic to improve timing.

When using this tutorial, focus on the processes and functionality of the PlanAhead software to determine how you can take advantage of these features in your designs.

Tutorial Design Description

The small sample design used in this tutorial includes:

- A RISC processor CPU core
- A pseudo FFT
- Four gigabit transceivers (GTs)
- Two USB interfaces

Software Requirements

The PlanAhead tool is installed with ISE Design Suite software. Before starting the tutorial, be sure that the PlanAhead tool is operational, and that the tutorial design data is installed.

For installation instructions and information, see the *ISE Design Suite 14: Release Notes, Installation, and Licensing (UG631)*.

Hardware Requirements

Xilinx recommends a minimum of 2 GB of RAM when using the PlanAhead tool on larger devices. For this tutorial, a smaller xc7k70t design is used, and the number of designs open at one time is limited. Although 1 GB is sufficient, it can impact performance.

Preparing the Tutorial Design Files

Copy the files from the ISE software installation area:

***<ISE_install_area>*/ISE_DS/PlanAhead/examples/PlanAhead_Tutorial.zip**

Extract the zip file contents into any write-accessible location which will be referred to in this tutorial as the extraction directory, or *<Extract_dir>*.

RECOMMENDED: *The tutorial sample design data is modified while performing this tutorial. A new copy of the original `PlanAhead_Tutorial` data should be extracted each time you run this tutorial.*

Lab 1: Design Analysis

Step 1: Viewing the Device Resources

1. Launch the PlanAhead Software.

- On Windows, select the Xilinx PlanAhead 14 Desktop icon or click:

  Start > All Programs > Xilinx Design Tools > ISE Design Suite 14.1 > PlanAhead > PlanAhead

- On Linux, go to the following directory `<Extract_Dir>/PlanAhead_Tutorial/Projects`, and type **planAhead**.

The PlanAhead environment opens, as shown in FIGURE 1.

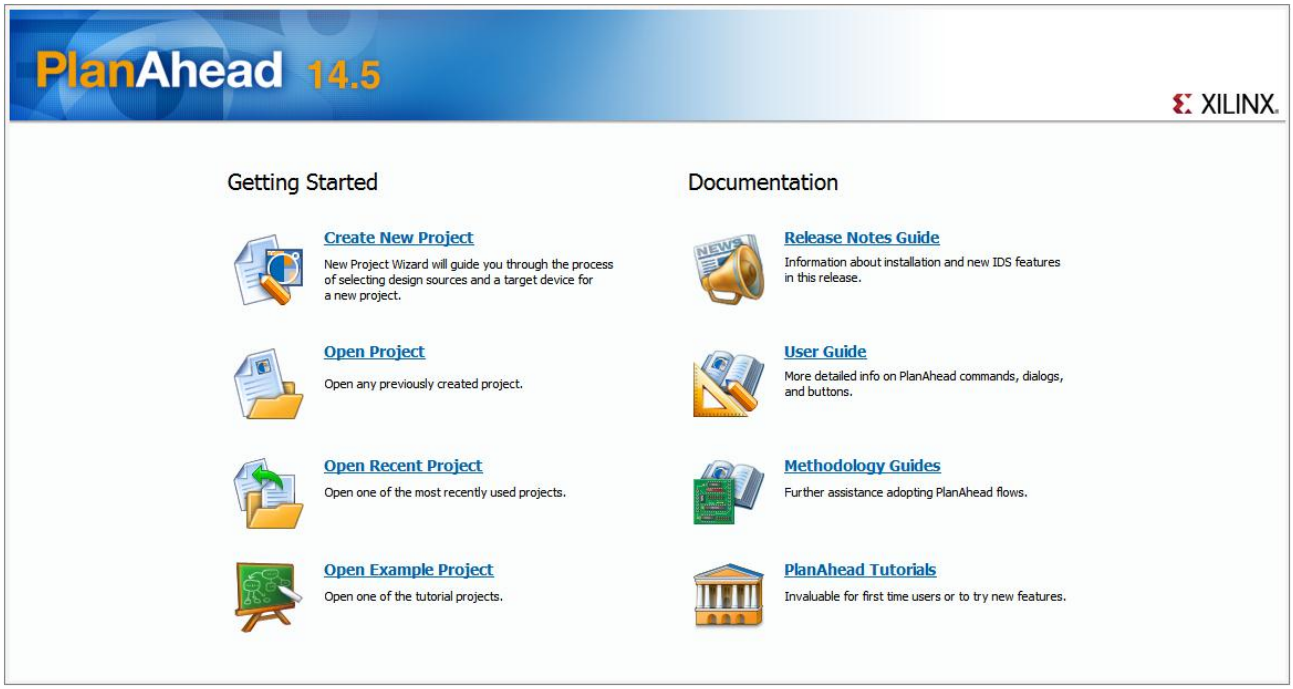


Figure 1: Getting Started Page

The PlanAhead Getting Started page contains links to open or create projects and to view documentation.

2. Select **File > Open Project**.

   Browse to: `<Extract_Dir>/PlanAhead_Tutorial/projects/project_cpu_hdl/` and open `project_cpu_hdl.ppr`.

The PlanAhead environment opens with the project open, as shown in FIGURE 2.

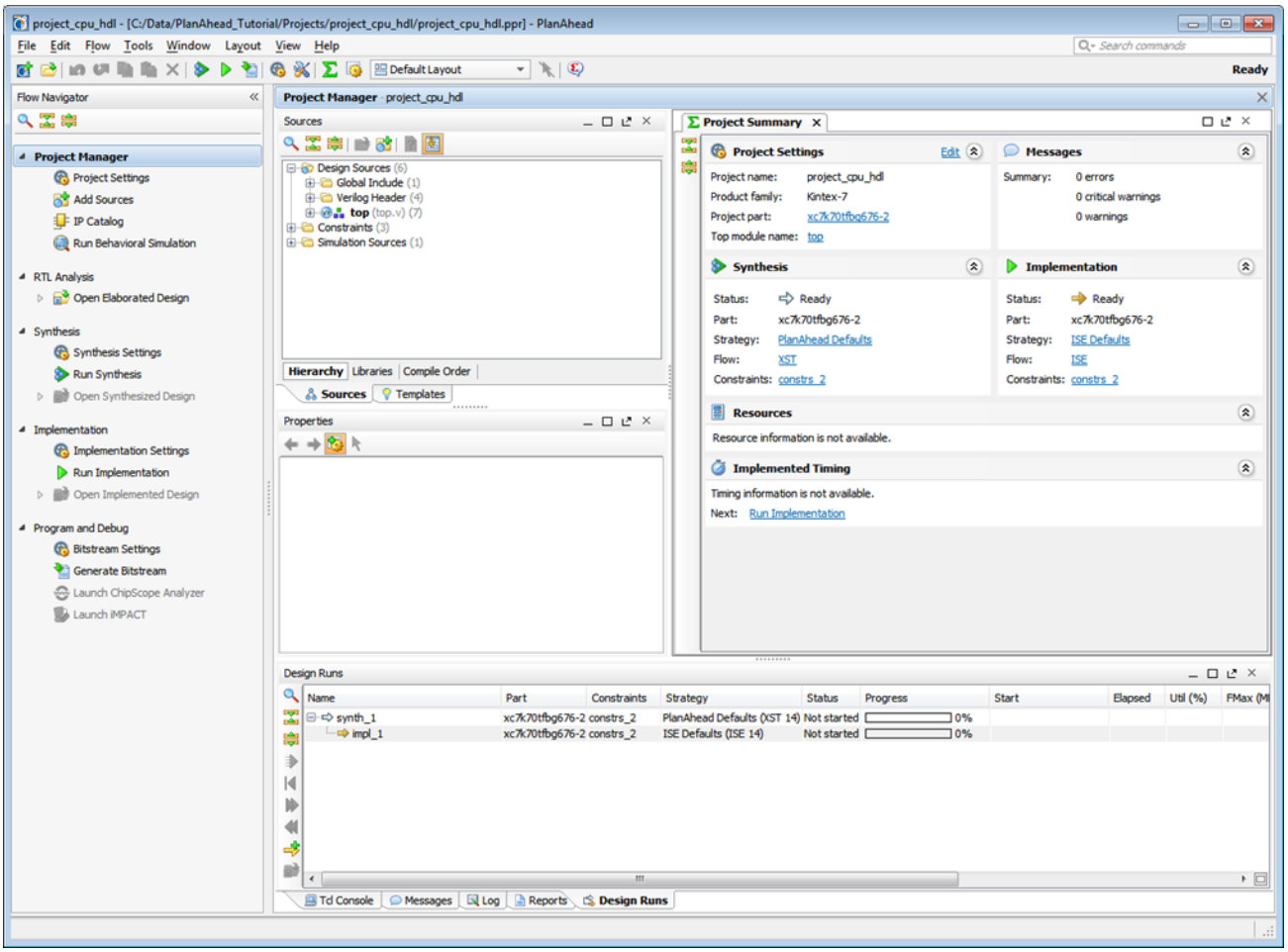


Figure 2: Default Layout View

3. In the Sources View, expand the `Constraints` folder to ensure `constrs_2` is the active constraint set, as shown in FIGURE 3.

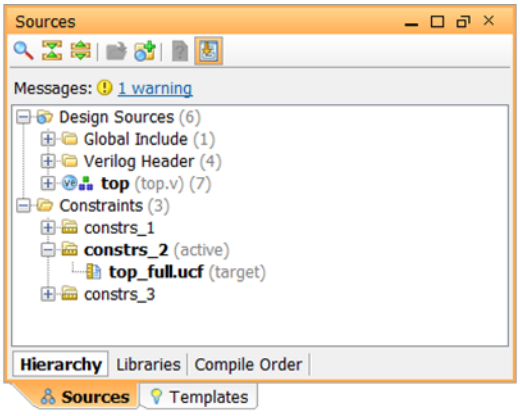


Figure 3: Sources View

If needed, select **constrs_2**, right-click to open the popup menu, and select Make active.

4. Open the **Design Runs** view and examine the runs information.

   Both Synthesis and Implementation runs are managed in the Design Runs view. Multiple runs, employing different strategies for synthesis or implementation, can be defined and managed from this view as well.

   You can see, as shown in FIGURE 4, that both Synthesis and Implementation runs show a status of **Not Started**.

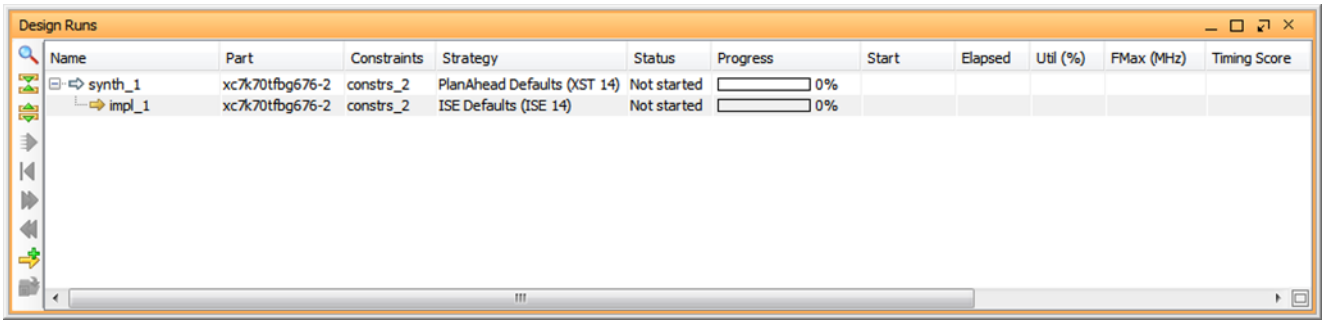


Figure 4: Design Runs View

5. In the Flow Navigator, select Run Synthesis to synthesize the design.
6. Watch the Log view for the transcript of the synthesis tool, XST.

   The run takes several minutes to complete. The Synthesis section of the Project Summary shows that the Synthesis run is in progress, as shown in FIGURE 5.

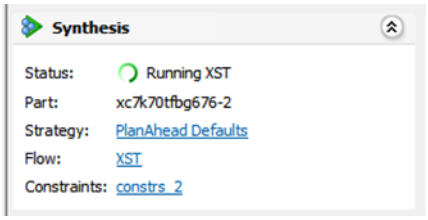


Figure 5: Synthesis Running

7. After synthesis completes, select **Open Synthesized Design** from the **Synthesis Completed** dialog and click **OK**.

The Synthesized Design opens, and the Design Runs view shows the status of XST Complete, as shown in FIGURE 6.

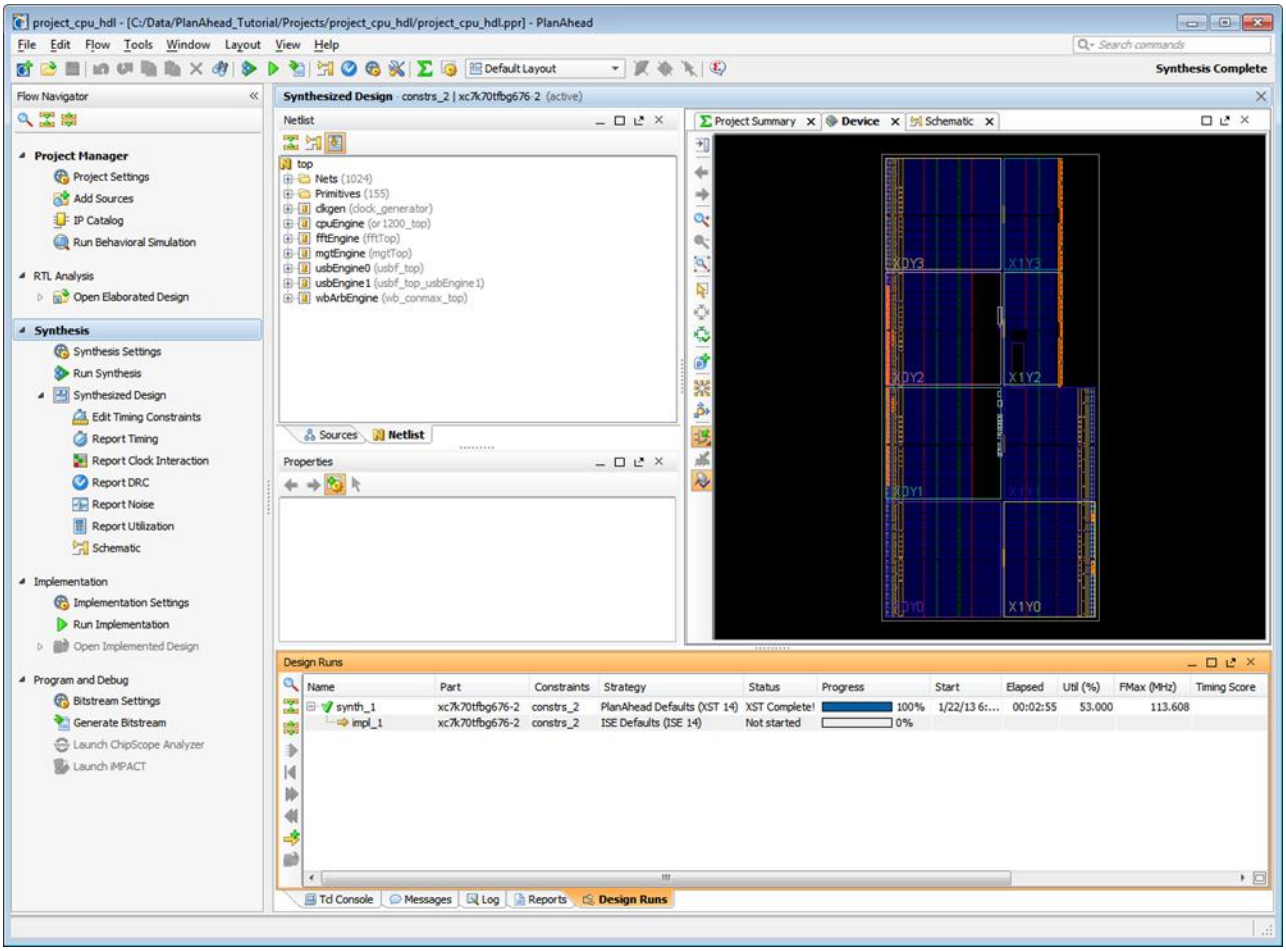
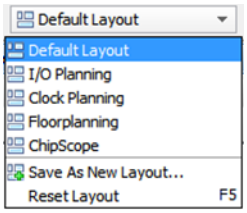


Figure 6: CPU Netlist in Netlist Design

8. In the Layout Selector, in the main toolbar, change the view layout to the Default Layout if that is not the current window



9. In the Device view, use Zoom Area by clicking and holding the left mouse button, while dragging down and to the right

   This will draw a Zoom Area rectangle and zoom into the Device view. Repeat this process as needed to zoom into the Device view close enough to see the different device resources as shown in FIGURE 7.

   In the Device view, the PlanAhead tool displays the FPGA device resources that can be used to implement the design, as a matrix of tiles. Sites are available within a tile for placement of netlist instances. The available sites include, for example, SLICEs, RAMs, MULTs, and DSPs, and vary in shape and color in the Device view to differentiate the object types contained in the site. Slices are fundamental building blocks of Xilinx FPGAs, containing LUTs and

registers, though the specific contents of a slice may vary with the device family. For more information on these terms, see the Xilinx Glossary.

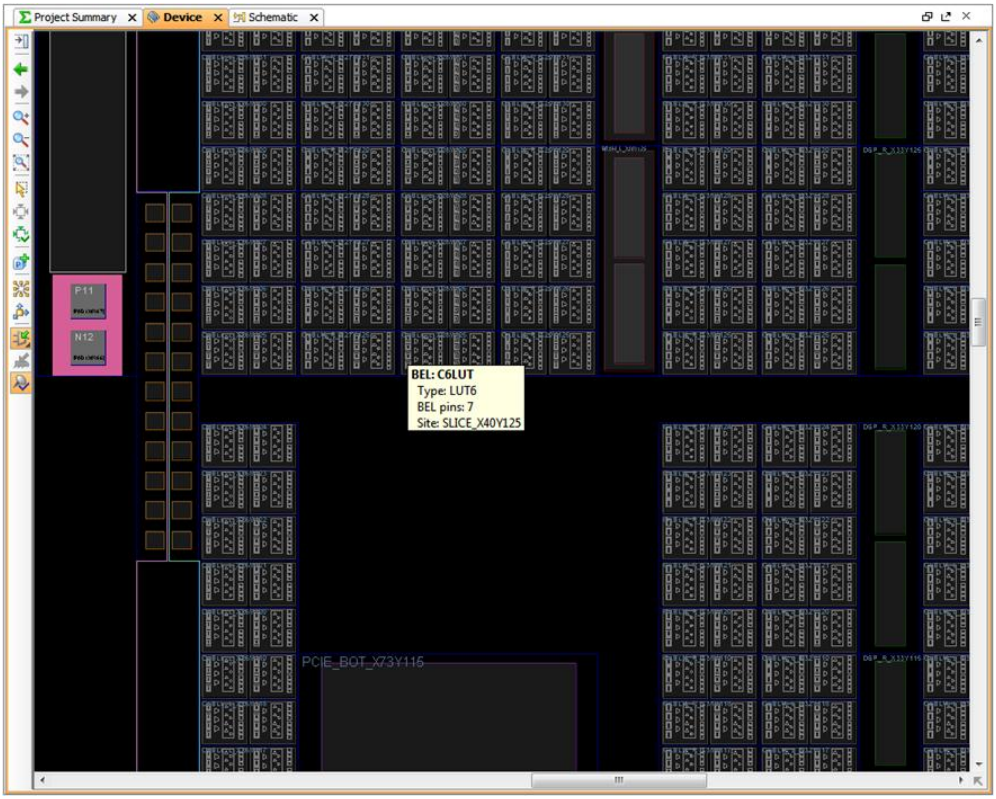
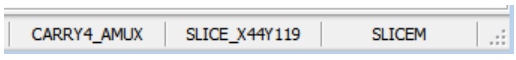


Figure 7: Zooming into the Device to View

10. Move the cursor slowly over the various device resources to view the tooltips, and take note of the following:
    - I/O port locations and I/O buffer assignments appear inside I/O banks.
    - Tall dark red tiles indicate a RAMB36 site that can also hold two RAMB18s or a FIFO layout.[1]
    - Tall green tiles indicate sites for DSP48s.
    - Square blue tiles are configurable logic blocks (CLBs) containing SLICEs.
    - SLICE coordinates appear in the status bar at the bottom right of the PlanAhead tool main window.



11. Select several different types of device resources in the Device view.
12. In the Properties view, examine the **BEL**, **Site**, and **Tile** property information.

[1] The colors mentioned here are for the Vivado IDE default color scheme. Your colors may be different

You can open the Properties view if it is not already open, by using **Window > Properties**.

13. In the Device view, click and hold the left mouse button, and drag the cursor up and to the left, or press **Ctrl+0**, to Zoom Fit the Device view to see the whole device.

Step 2: Viewing the Clock Resources

The Device view also shows the clock regions, which you can use to help guide floorplanning for the design. The Clock Regions view lists all the clock regions in the device. The Clock Region Properties view displays clock region information to indicate potential clock contentions prior to implementation. Viewing clock domains is covered later in the tutorial.

1. Select **Window > Clock Regions** to display the Clock Regions view.
2. Select one of the clock regions listed in the table.

   The clock region is cross-selected in the Device view as seen in FIGURE 8.

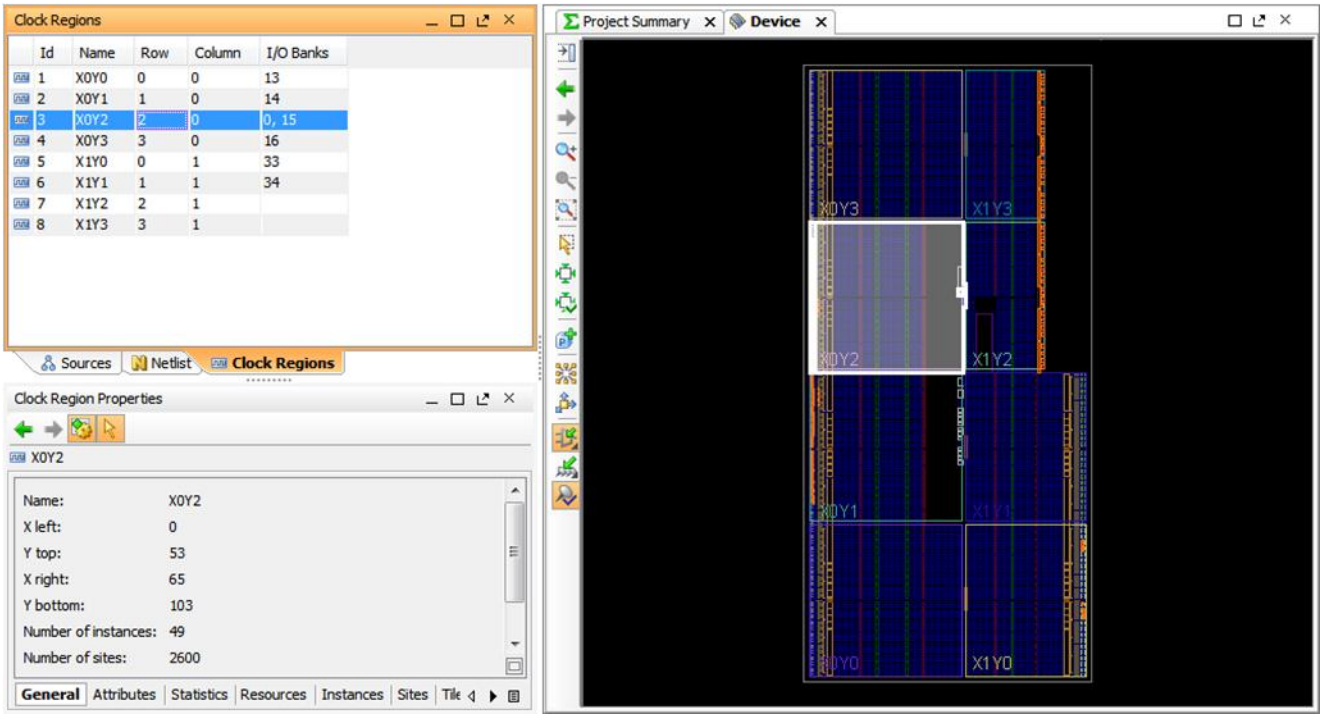


Figure 8: Viewing Clock Regions

3. Examine the **Clock Region Properties** view.
4. In the Properties view, click the Statistics tab, and scroll to examine the device resources of the selected region.

   At this point, without any logic placed onto the device, only the count of resources is available. Later, as logic is assigned to resources through placement, the utilization of the resources is also displayed.

5. In the Properties view, click the Resources tab to see details of the `BUFR` and `IDELAYCTRL` sites.
6. In the Resources tab, select one of the BUFRs, and notice it highlights in the Device view.
7. In the Device view toolbar menu, enable **Autofit Selection** to have the PlanAhead tool automatically zoom and center the selected object.
8. In either the Device view or the Properties view, right-click to open the popup menu and select **Mark** to mark the selected object.
9. In the Device view, use **Zoom Fit** to fit the whole device.

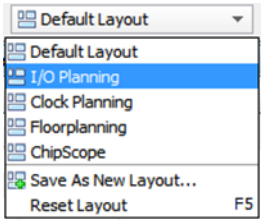
   Notice the presence of the mark allows you to locate the object even when viewing the whole device.
10. Select the **Unmark All** main toolbar button to remove the mark.
11. In the Clock Region Properties view, click the I/O Banks tab to examine the I/O Banks related to the clock region.

Note: You may need to scroll across the bottom of the Properties view to see the I/O Banks tab.

12. In the I/O Banks tab, select one of the I/O banks.

    The selected I/O bank is cross-selected in the Device view as well.
13. In the Layout Selector, in the main toolbar, change the view layout to the I/O Planning view.

    You can also select **Layout > I/O Planning** from the main menu.

    The view layout has changed to facilitate pin planning in the design. The Package view is opened in the graphical workspace, and the Package Pins view is open at the bottom of the PlanAhead tool.

    The selected I/O bank is highlighted in both the Device and Package Pins views.
14. In the Layout Selector, change the tool layout back to Default Layout.

Step 3: Exploring the Logic Hierarchy

This section discusses features of the PlanAhead tool that help you to explore and understand the hierarchy of the design.

1. Click the Netlist view, and if needed, click the Collapse All button .
2. Expand the cpuEngine module by clicking the + button next to the module.

   You see a tree hierarchy as shown in FIGURE 9.

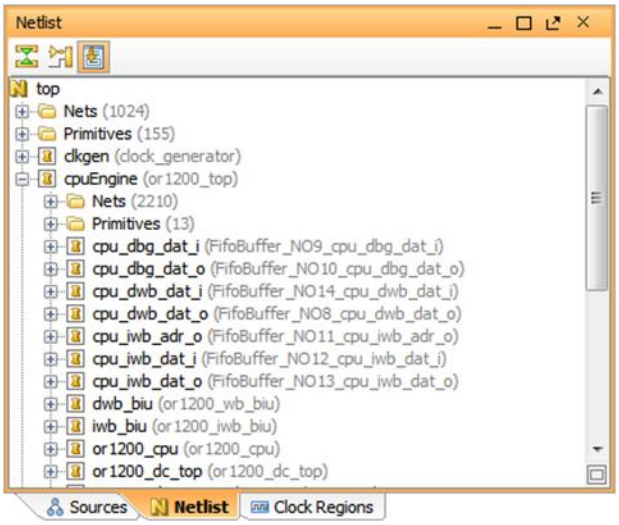


Figure 9: Expanding the Netlist View

3. In the `cpuEngine` module, expand the `Primitives` folder.

   These are the primitive logic cells immediately inside the `cpuEngine` module. They do not include the sub-modules of the `cpuEngine`, or primitives of those sub-modules.

4. Expand the `Nets` folder.

   These are the nets immediately inside the `cpuEngine` module.

5. In the Netlist view, click the **Collapse All** button to simplify the view.
6. Expand the `usbEngine0` module.
7. Select the **u4** module.
8. Right-click to open the popup menu, and select **Show Hierarchy**, or press **F6**.

The Hierarchy view opens in the graphical workspace, as shown in FIGURE 10.

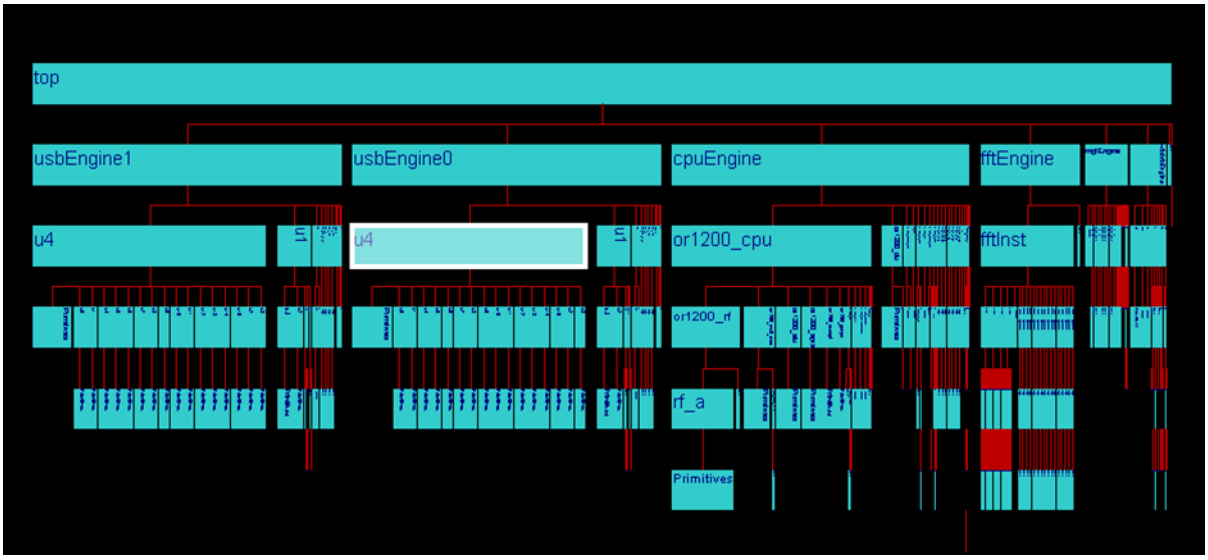


Figure 10: Hierarchy View

The selected logic module displays in the Hierarchy view. The Hierarchy view displays the hierarchical relationship of the modules and their relative sizes. The widths of the blocks in the Hierarchy window are relative to the device resources consumed by each block. It lets you see how a timing path traverses the logic hierarchy, or gauge how big a module is before floorplanning the module. You can select modules directly from this view for floorplanning. Logic selected in other views is highlighted in the Hierarchy view.

9. Select any module in the Hierarchy view, and notice that the module is selected in the Netlist and other views, as well.
10. Click the **Unselect All** main toolbar button, or press **F12**.
11. Close the Hierarchy view by clicking the **X** button in the view tab.

Step 4: Displaying Device Utilization Statistics

The PlanAhead tool provides design statistics for resource utilization to help determine the optimal device for the design. The tool helps you see how the logic resources are split between modules. It is easy to explore multiple device types to determine the best overall utilization and performance estimations.

Viewing the Resource Estimates of the Entire Design

1. From the Flow Navigator Select **Report Utilization**.

   The Report Utilization view opens, as shown in FIGURE 11, showing the resource utilization by logic type, and providing additional details for each level of design hierarchy.

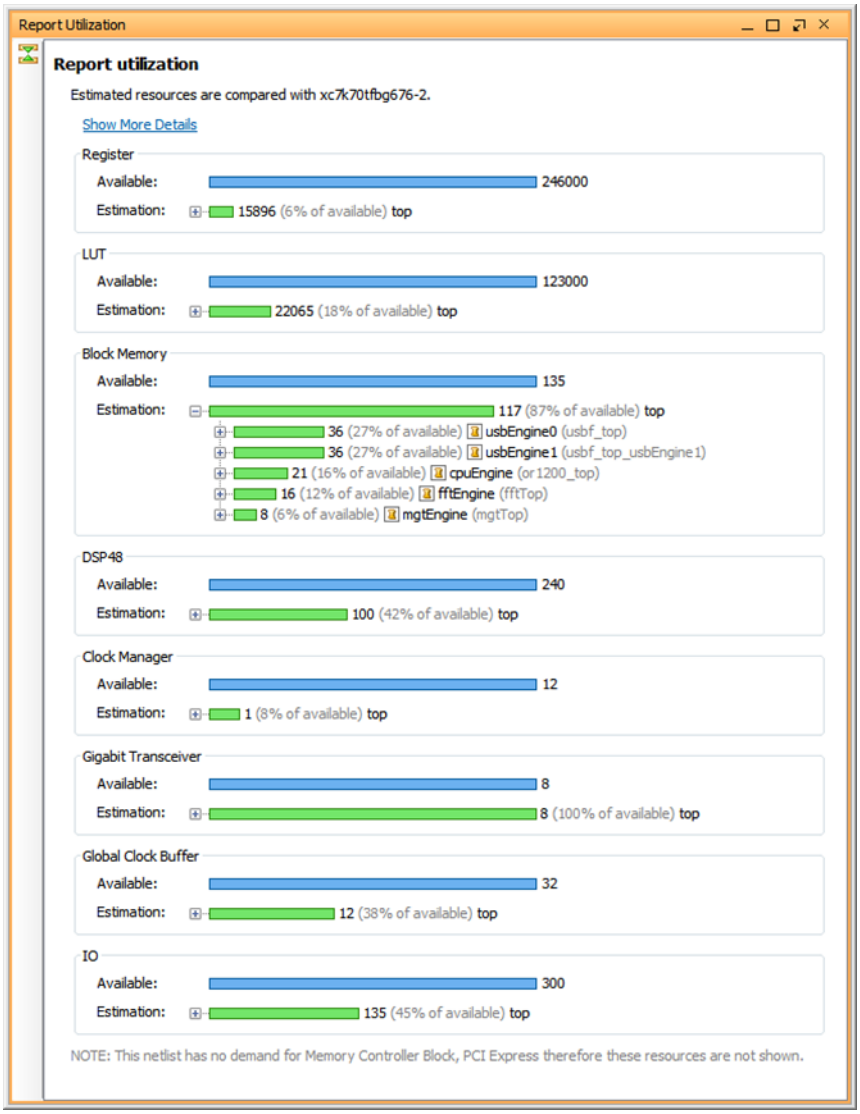


Figure 11: Report Utilization View

In the Report Utilization view, click the expand the **Plus** icon ⊞ next to **Estimation** under Block Memory (block RAM).

You see that `usbEngine0` and `usbEngine1` are the two largest consumers of block RAM, together accounting for more than half of the utilization.

2. Select **usbEngine1** from the block RAM Estimation section.

   Notice that usbEngine1 is selected in the Netlist view as well.

Exploring the Resources in a More Detailed View

The Report Utilization view has a link to "Show More Details". Clicking this link opens the Pblock Properties view to let you examine the device resources in greater details.

1. In the Report Utilization view, click the **Show More Details** link.

The Pblock Properties view displays, showing the ROOT level of the design.

The PlanAhead tool provides the ability to divide the design into smaller, more manageable physical blocks (Pblocks). Pblocks can include logic modules and primitive logic from anywhere in the design hierarchy.

The tool automatically creates a single Pblock from the top-level of the design, or the ROOT module, even when there are no other Pblocks defined. In this section you will examine the resources available in the ROOT module.

2. In the Pblock Properties view, select the Statistics tab, if necessary.
3. View the **Physical Resource Estimate**s that display in the Pblock Properties view, as shown in FIGURE 12.

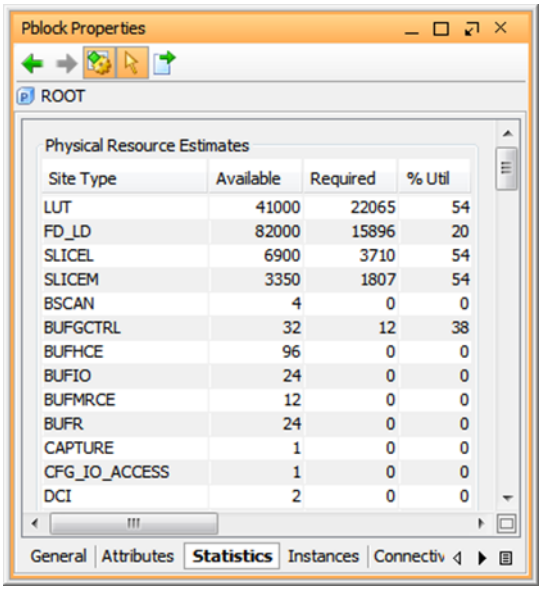


Figure 12: ROOT Module Statistics

4. Scroll down the design statistics displayed in the Pblock Properties view.

   The Statistics tab displays the device resource utilization for each type of logic element, carry chain count, longest length, Clock Report, I/O utilization, and Primitive instance and interface net counts.

Note: If this design had any RPMs, the RPM count and maximum size information would be shown as well.

5. Close the Report Utilization view.

Step 5: Running Design Rule Checks (DRC)

Xilinx recommends running the Design Rule Checker (DRC) before implementation to check for some common design issues. The ISE implementation tool DRCs are used for design sign-off, and take precedence over the DRCs in the PlanAhead software.

1. Select Report DRC in the Flow Navigator.

   The Run DRC dialog box opens. By default, all DRC checks are selected. You can expand the various DRC rule categories, and enable or disable DRCs that are appropriate for the specific design phase or area of interest, as shown in FIGURE 13.

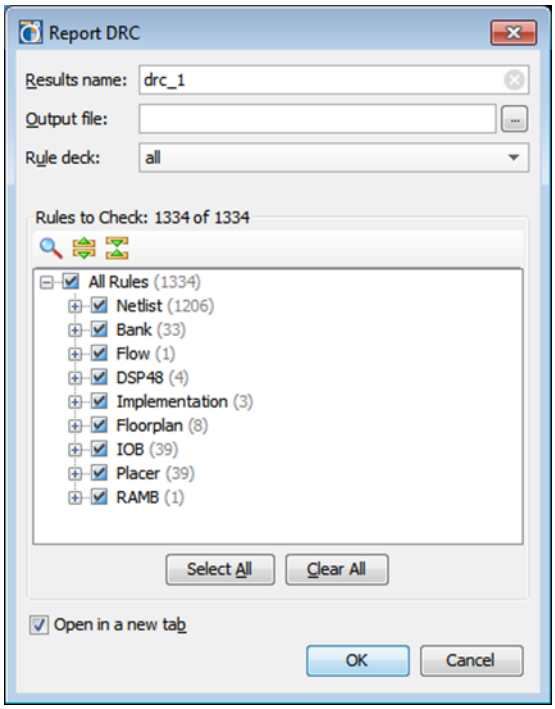


Figure 13: Report DRC

2. Click **OK** to run all rule checks.

   The DRC Results view opens and indicates that there are several DSP48 and block RAM warnings. Errors, warnings and information messages display in the DRC Results view as shown in FIGURE 14. Messages provide the following color-coding:

   - Information messages have a blue icon.
   - Warnings have a yellow icon.
   - Critical Warnings have an orange icon.
   - Errors have a red icon.

Note: DRC errors do not prevent Implementation from being run.

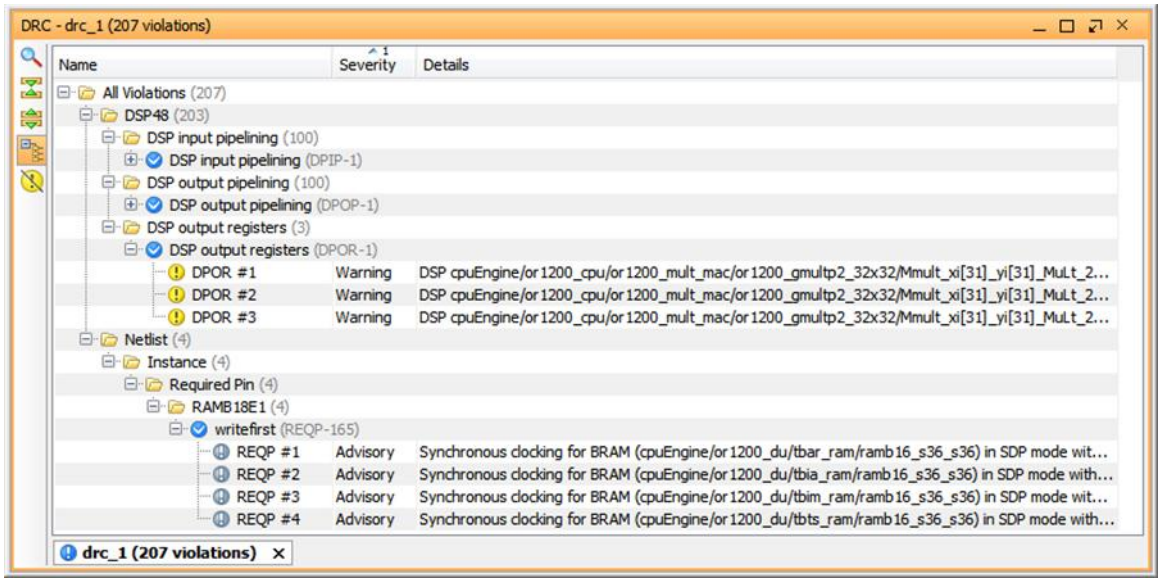


Figure 14: Design Rule Violations

3. In the DRC Results view, click the DPOR #1 Warning.

   The Violation Properties view opens and describes the violation. There are links to the specific violations in the design associated with this rule, as shown in FIGURE 15.

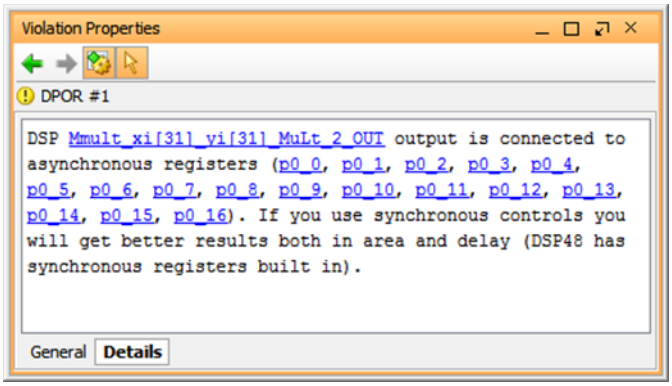


Figure 15: Violation Properties View

4. Right click in the Violations Properties view to open the popup menu.

   Notice that by default the tool will automatically select the objects in the DRC message.

5. Select the Netlist view.

   Notice that `Mmult_xi[31]_yi[31]_MuLt_2_OUT` and the related flip-flops are selected. You might need to scroll through the Netlist view to see the selected objects, as shown in FIGURE 16.

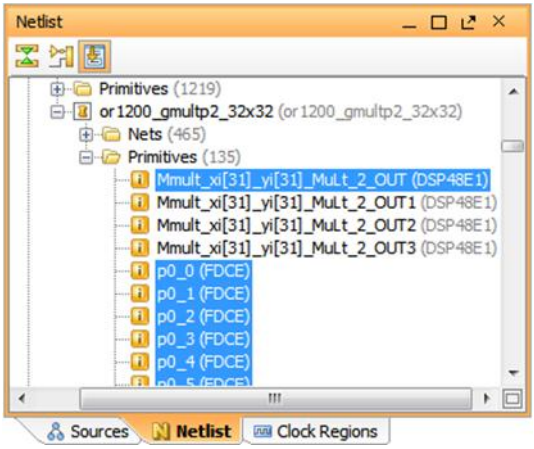


Figure 16: Violation Objects in the Netlist View

6. In the DRC Results view, expand and scroll through the list of design violations.
7. Close the DRC Results view by clicking the X button in the tab.

Step 6: Performing Timing Analysis

In this step, you will investigate timing before implementing the design.

Before running implementation, it can be helpful to perform an early static timing estimation, including estimated route delays, to determine the feasibility of successfully implementing the timing constraints. The PlanAhead tool timing engine provides an estimate of what the route delays will be, and does not report on whether the design has actually met timing (post-implementation).

IMPORTANT: *Even with a fully placed and routed design, only the TRCE timing tool indicates whether a design has met timing. The PlanAhead Report Timing command should not be used for timing sign-off.*

1. In the Flow Navigator, select Report Timing.

   The Report Timing dialog box opens to the Targets tab, as shown in FIGURE 17, in which you can specify timing paths start, through, and end points to analyze. If you do not specify targets, the Report Timing command analyzes all timing paths in the design.

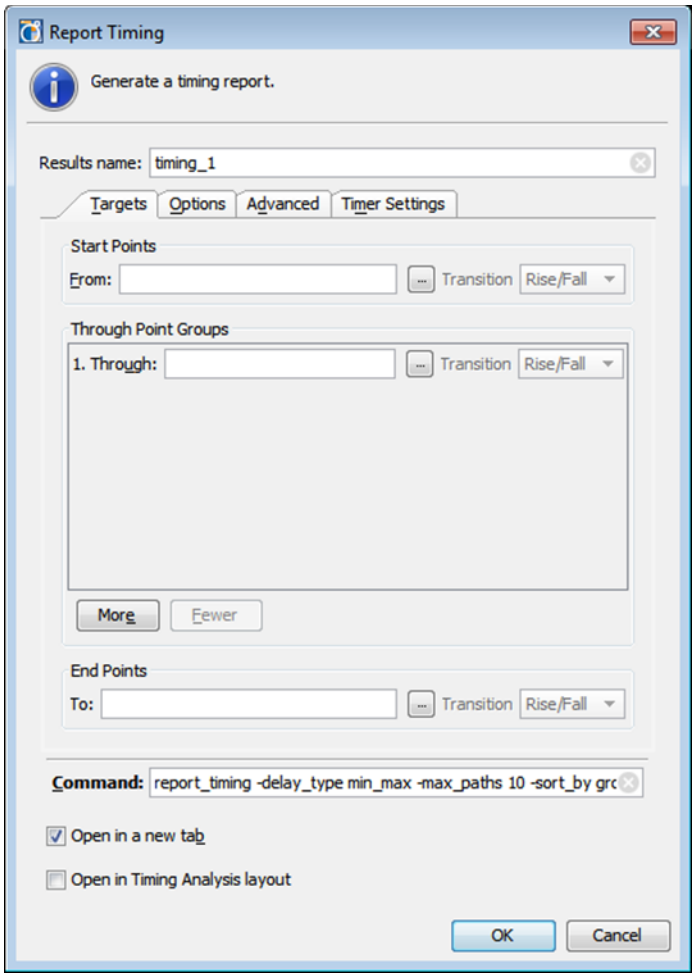


Figure 17: Report Timing

2. Select the Options tab, shown in FIGURE 18.

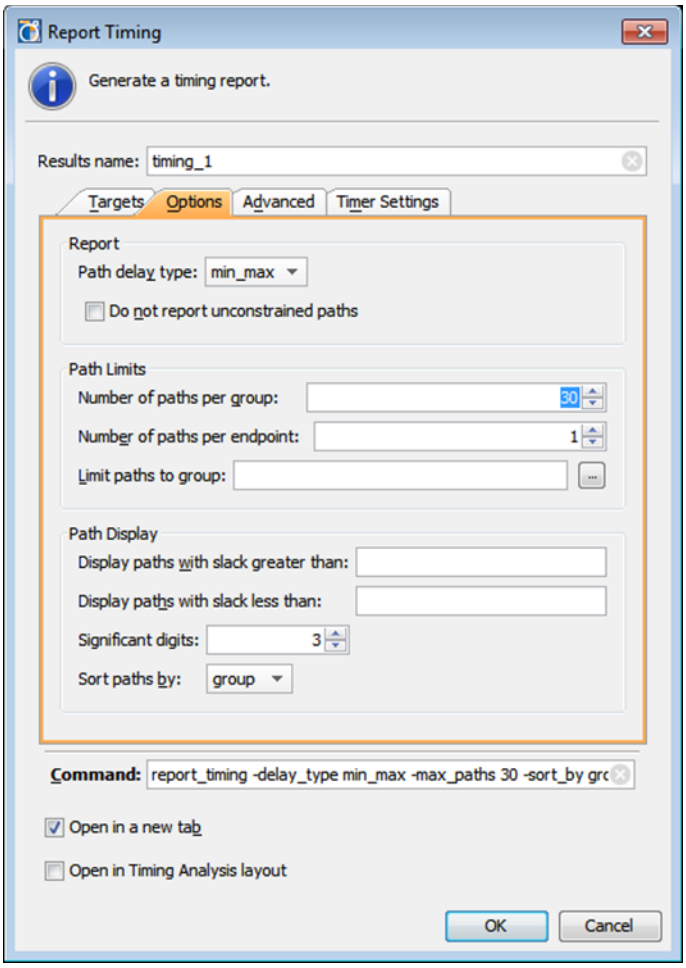


Figure 18: Report Timing Options

3. In the **Number of paths per group** field, type **30**.
4. Click the Advanced and Timer Settings tabs, and inspect the various options. Make no changes on those tabs.

   In the Timer Settings tab, the Interconnect pull-down has two values: Estimated and None. At this point in the design, prior to placement and routing, the net delays are estimated based on a routing delay model. You can also optionally exclude net delay from timing analysis.

The timing engine differs from the ISE timing engine; it cannot give you exact route delays.

5. Click **OK** to run timing analysis.

The Timing view opens as shown in FIGURE 19.

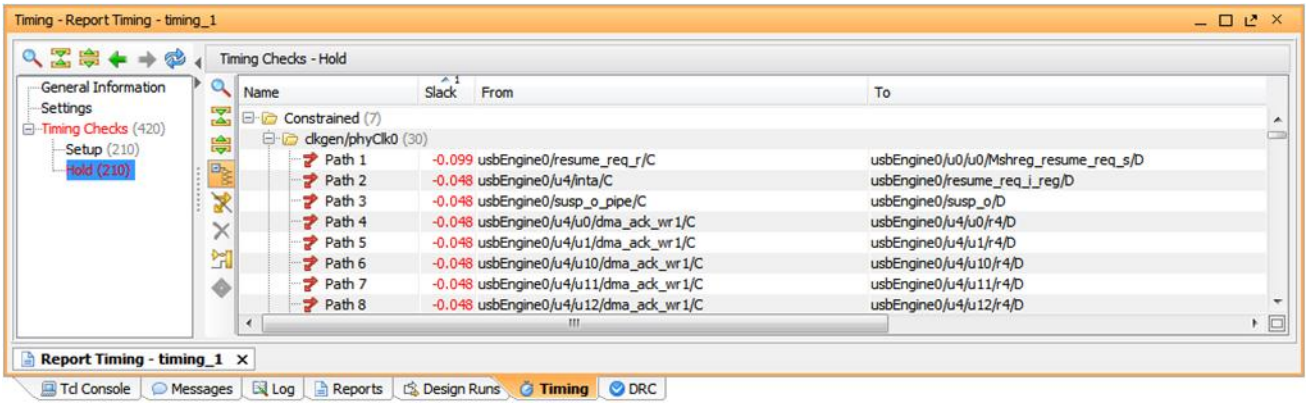


Figure 19: Timing Analysis Results

The list of paths returned by Report Timing display in the Timing view. Paths show under folders indicating the relative clock constraint. Paths with negative slack display in red. The list of paths are initially grouped by constraint. You can disable this, and list all paths without grouping, by disabling the **Group by Constraint** command on the timing report tool bar menu.

The tree view on the left displays general information, and the command settings used when Report Timing was run. It also lets you view results for either Setup or Hold analysis if available.

6. Maximize the Timing view.
7. Click **Setup** from the tree on the left side of the Timing view.
8. Scroll down the list of timing paths.

   Notice that most of the timing paths have start and end points in the cpuEngine module.
9. Click the **To** column header twice to sort the list by Source.

   The report is now reverse sorted by To column values. You can sort all of the table style views in the PlanAhead tool in the same way:

- To perform a reverse sort, click the column header twice.
- To add a secondary sort criteria, press Ctrl and select another column header.

10. Click **Hold** from the tree on the left side of the Timing view and scroll down the list of paths.

    Prior to implementation, you should focus on Setup violations, as Hold checks are dependent on routing.
11. Click **Setting**s from the tree on the left side of the Timing view and examine the timer settings.
12. Restore the Timing view, and **Close**.

Step 7: Implementing the Design

With a synthesized netlist, and preliminary DRC and timing analysis complete, you are now ready to implement the design. The PlanAhead tool integrates ISE place and route technology (MAP and PAR) to implement the design.

1. If the Sources view is hidden from view, display it by selecting **Window > Sources**.
2. In the Sources view, click the **Collapse All** button, and then expand `constrs_2`, as shown in FIGURE 20.

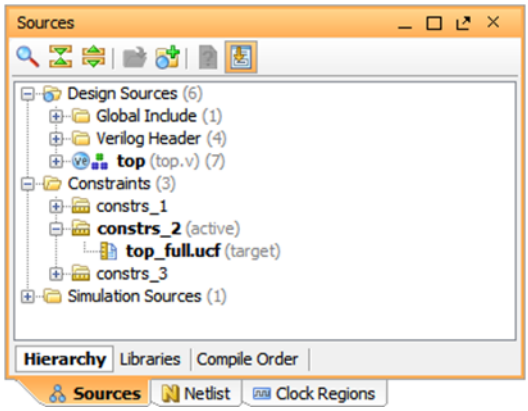


Figure 20: Active Constraint Set

When running the implementation tools, the PlanAhead software uses constraints from the active constraint set by default. It also writes constraints to the target constraint file. Make sure that `constrs_2` using `top_full.ucf` is the active constraint set.

IMPORTANT: *If a Netlist Design or Implemented Design is open with changes that have not yet been saved to disk, the in-memory changes will be used instead of the UCF on disk.*

3. Double-click **top_full.ucf** to open the file to examine the contents of the constraint file.
4. Close the file without saving any changes you might have made.

Creating Implementation Runs

PlanAhead lets you configure and run multiple Synthesis and Implementation runs in parallel or simultaneously. In the following steps you configure multiple implementation runs, but only launch one run.

1. In the Flow Navigator, right-click **Implementation** to open the popup menu.
2. Click **Create Implementation Runs**.
3. In the **Create New Runs** dialog box, click **Next**.

   The Configure Implementation Runs dialog box opens with an `impl_2` run already defined.

   You update the strategy used by that run, and add a few more, as seen in FIGURE 21

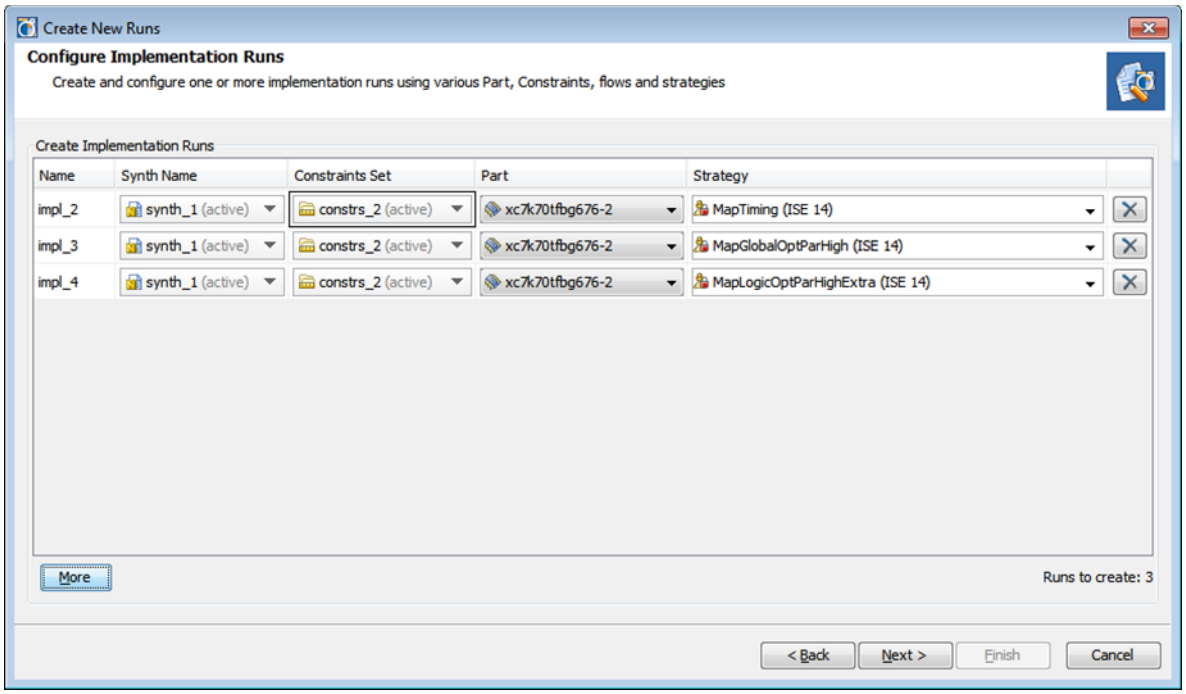


Figure 21: Configure Implementation Runs

4. Under **Strategy** for the **impl_2** run, change it from the default to **MapTiming**.
5. Click **More** several times to add new implementation runs with new strategies.

   Each new run added uses the next strategy from the list of defined strategies. You can select different strategies for the run as needed.
6. Click **Next** to review the **Launch Options** dialog box, as shown in FIGURE 22.

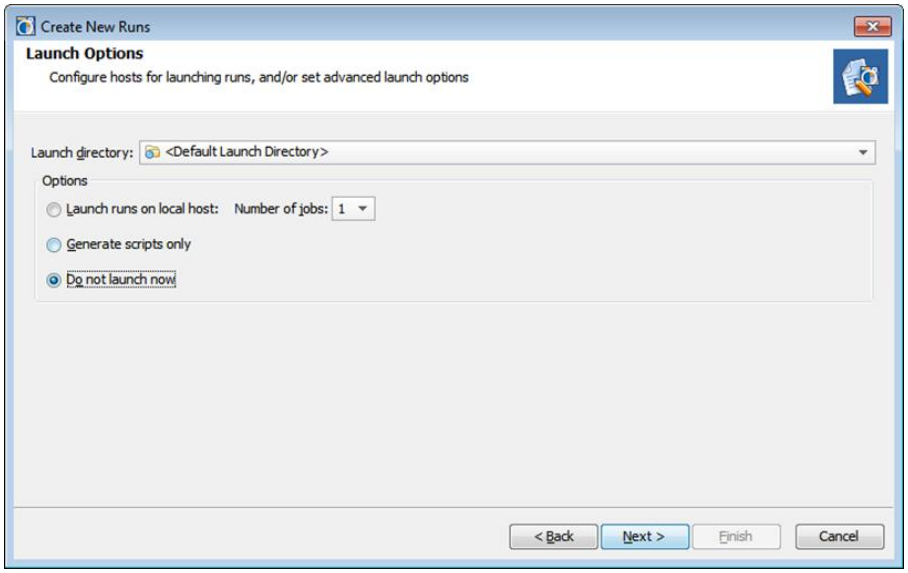


Figure 22: Launch Options

7. Select **Do not launch now**, and click **Next**.

8. Review the **Create New Runs Summary** dialog box and click **OK**.

   The new implementation runs you created are added to the Design Runs view, but are not launched at this time. You can select any of them in the Design Runs view to make them the active run, and then launch them together or individually.

9. In the Design Runs view, select **impl_1**, and ensure that it is the *active run*.

   You can use the **Make Active** command from the popup menu to make it the active run if necessary.

10. In the Design Runs view, right click, and select **Launch Runs** from the popup menu.

TIP: *You can select more than one run in the Design Runs view, and use **Launch Runs** to launch multiple runs.*

   Implementation takes several minutes to complete as it runs the design through the ISE Place and Route tools; specifically, NGDBuild, Map, PAR, TRACE, and XDL. While it is running, you can watch the Log view for a transcript of the various tools being run.

   Because implementation is run as a separate process in the background of the PlanAhead tool process, you can continue to work with your design in a number of ways in the PlanAhead tool. For instance, run some of the reports shown in the Flow Navigator under Synthesized Design, like Report Noise or Report Clock Interaction, or open and explore the Schematic view.

   Notice that as you do some of these things, implementation continues to run in the background.

11. After implementation completes, in the **Implementation Completed** dialog box, select **Open Implemented Design** and click **OK**.

12. If prompted, select **Yes** to close the Synthesized Design.

   Note: You may have disabled this prompt at some time if you elected to "never show this dialog again". To restore the prompt, go to **Tools > Options > Window Behavior**, and check the **Show** dialog before switching to a different design checkbox.

   The results for the implemented design import into the PlanAhead tool from the ISE tools.

The Device view shows the placement of each instance, and the post-place and route timing information reports from TRCE in the Timing view, as seen in FIGURE 23.

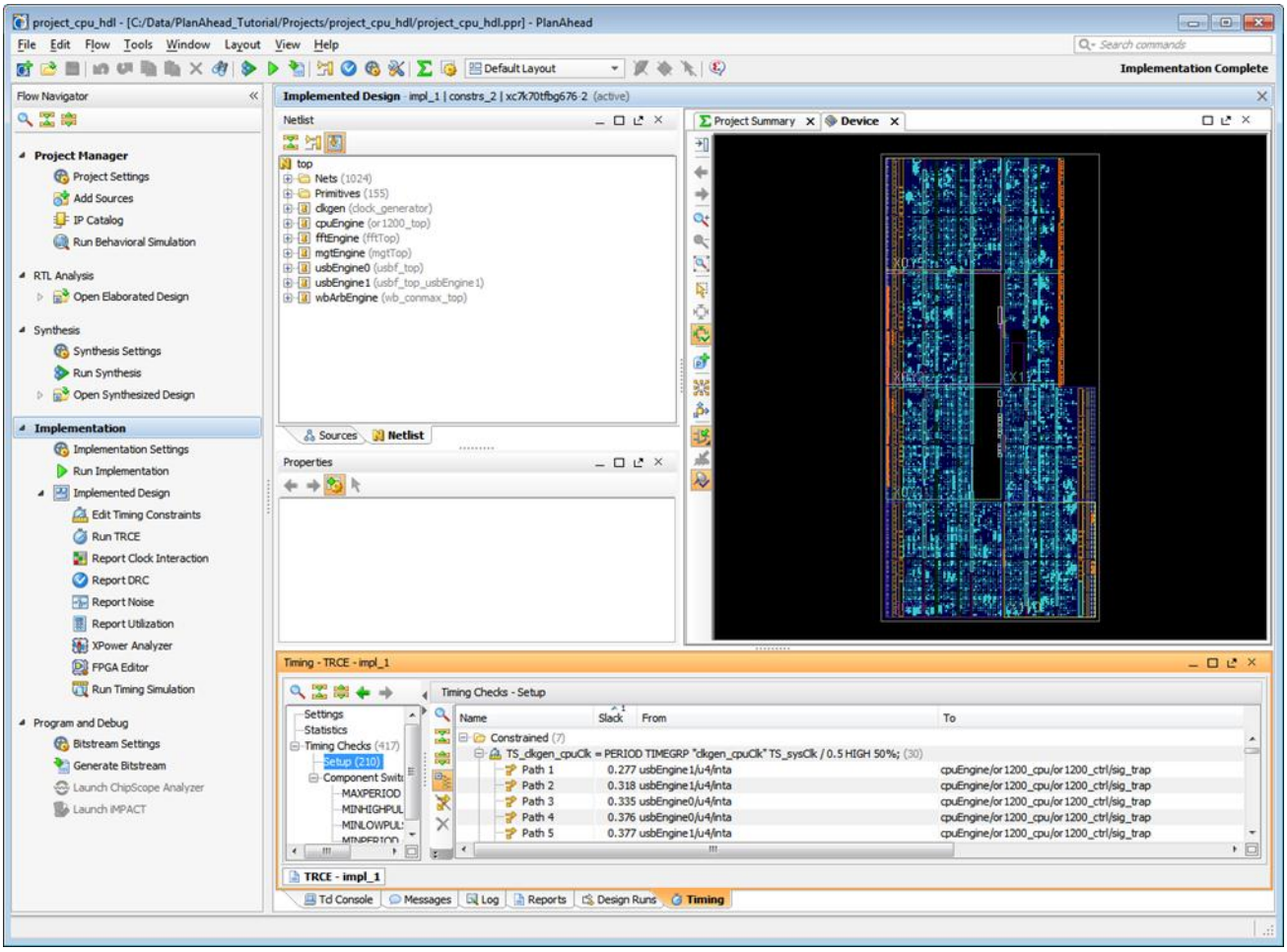


Figure 23: Implemented Design

13. Click the **Messages** view to display the Messages view.
14. Click the **Collapse All** toolbar button .
15. Expand the **Implementation** messages.

16. Use the **Expand Map** folder to see the messages generated by this tool, as shown in FIGURE 24.

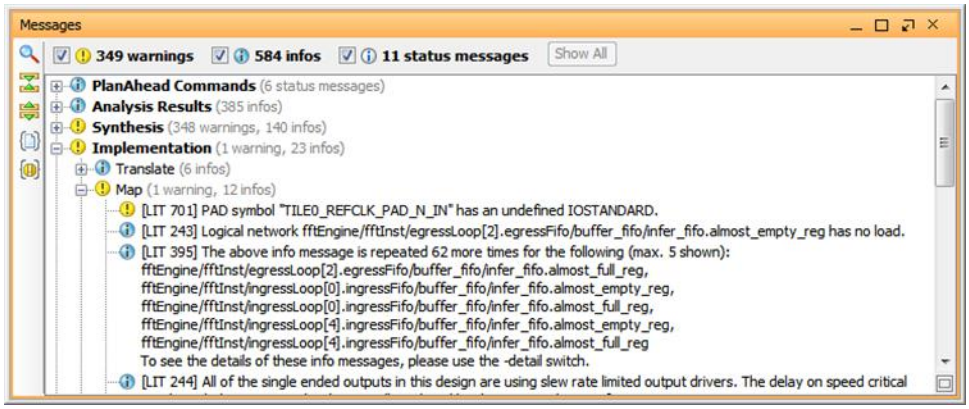


Figure 24: Implementation Messages

The Messages view collects all information, warning, and error messages from the various tools integrated into the synthesis and implementation processes.

17. Click the Reports view.
18. If the Reports view is not opened, select **Window > Reports** to display the Reports view, as shown in FIGURE 25.

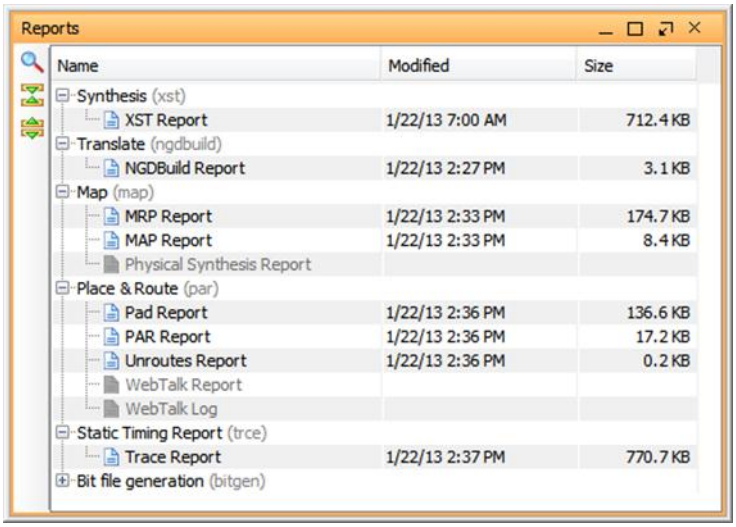


Figure 25: Implementation Reports

19. Double-click the report name to view the actual report.
20. Close the report files.

Step 8: Viewing Timing Paths

You can analyze timing results from the implementation process to help define a floorplanning strategy. You can use the path sorting and selection techniques available in the Timing view with the timing report imported from TRCE during implementation.

Marking Timing Paths

1. Click the Timing tab.
2. In the Timing view, select **Path 1**, as shown in FIGURE 26.

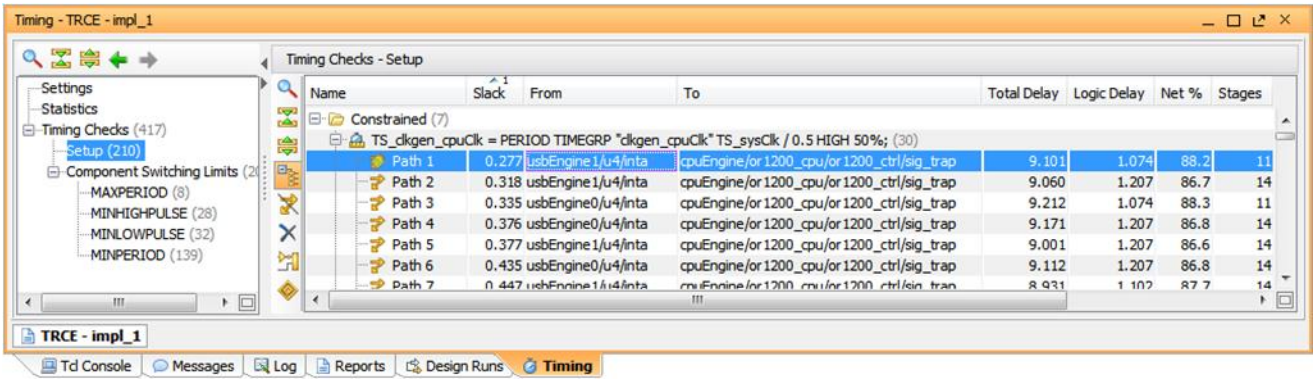


Figure 26: Analyzing Timing

3. Right-click to open the popup menu, and select **Mark**.

   The timing paths show on a constraint-by-constraint basis. When you select paths in the Timing view, the path selects in the Device view, and the Path Properties view shows the details of the timing path.

   The Mark command, marks:

   - Timing path start points with a green diamond,
   - Through points with a yellow diamond
   - End points with a red diamond.

This helps you quickly visualize the data flow through the timing path, as shown in FIGURE 27.

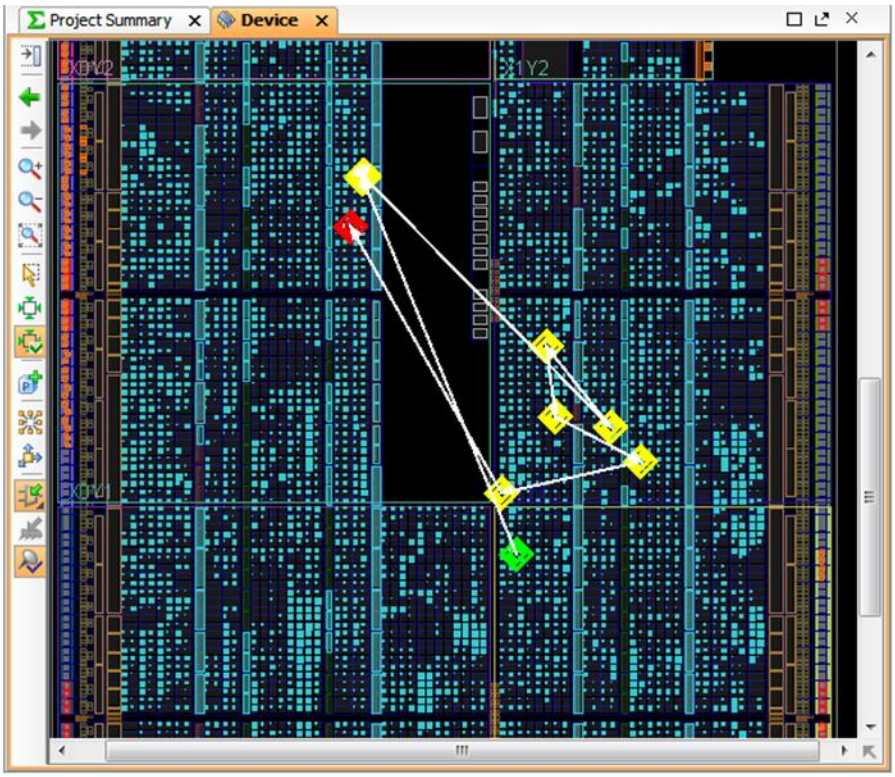


Figure 27: Marked Timing Path

4. Select the Unmark All button in the main toolbar, or View > Unmark All to clear the marks from the Device view.

   In the Timing view, the timing paths group by constraints as a default.

5. In the Timing view, click **Collapse All** to display only the reported constraints.
6. Expand the `TS_clkgen_usbClk` timespec to view the listed paths.
7. Click once in the **From** column head to sort the timing paths according to the start points.
8. Select all the paths in `TS_clkgen_usbClk` with `usbEngine1/*` as a start point. Do not grab other paths.
9. Right-click and select **Schematic** from the popup menu.

The Schematic view shows all of the instances on the selected paths, as shown in FIGURE 28.

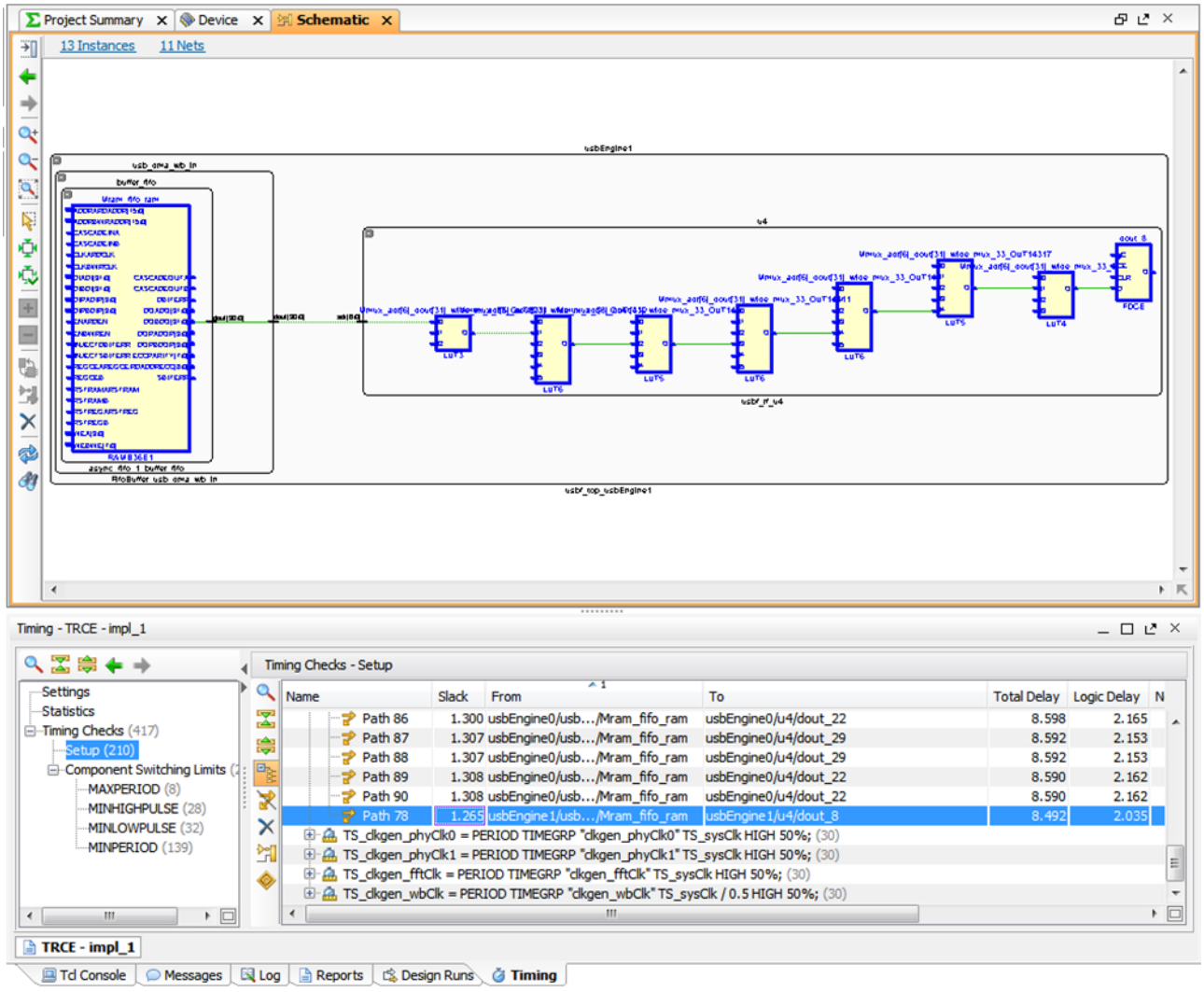


Figure 28: Schematic View of Timing Paths

10. In the Netlist view, click the **Collapse All** button.
11. In the Schematic view, right-click and use **Select Primitive Parents**.

This selects the parent modules of the currently selected instances in the timing paths. The corresponding logic modules select in the Netlist view. This helps you identify the hierarchical location of the selected timing path in the overall design, as shown in FIGURE 29.

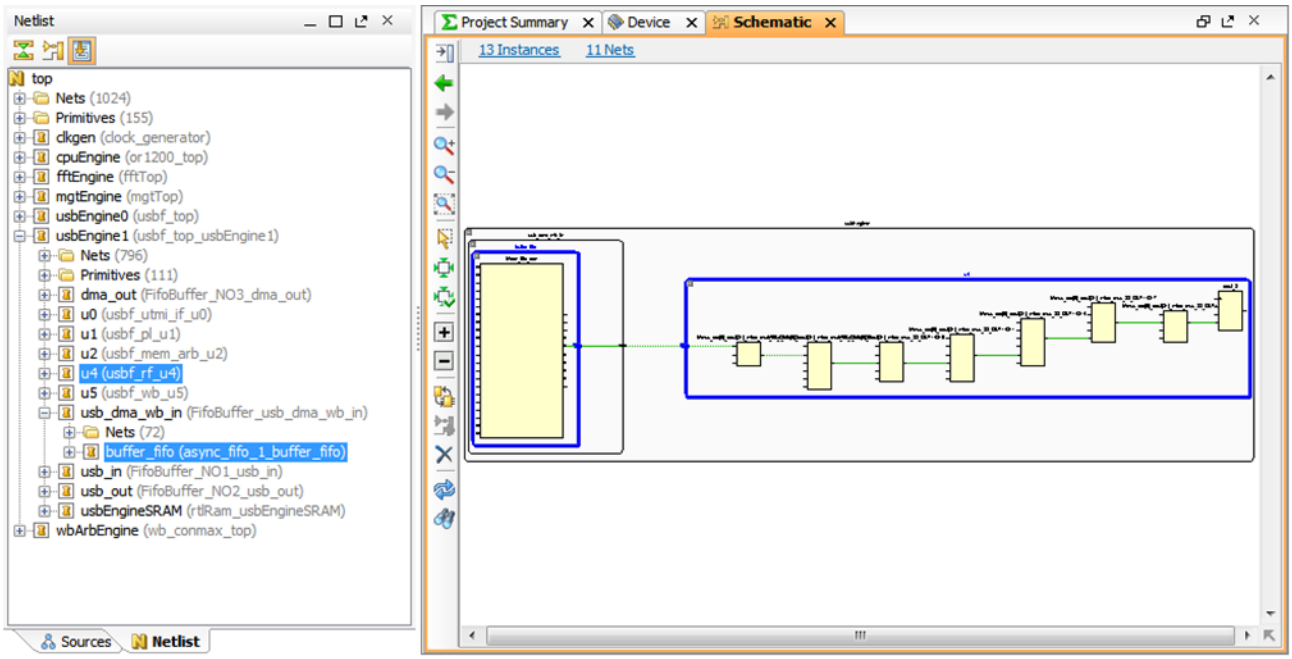


Figure 29: Schematic Primitive Parents

12. In the Netlist view, right-click to open the popup menu, and select the **Show Hierarchy** command, or press **F6.**

    The Hierarchy view opens, as shown in FIGURE 30, with the selected modules highlighted. These are the hierarchical design modules associated with the selected timing paths.

    According to the Hierarchy view, the timing path logic is mostly contained in the `usbEngine1` module, and constitutes a large percentage of that block. Also notice that `usbEngine0` is a similar module, if not identical.

    These `usbEngine` blocks are the foundation of your floorplan in the remainder of this tutorial.

13. Click the **X** button to close the Hierarchy view by.

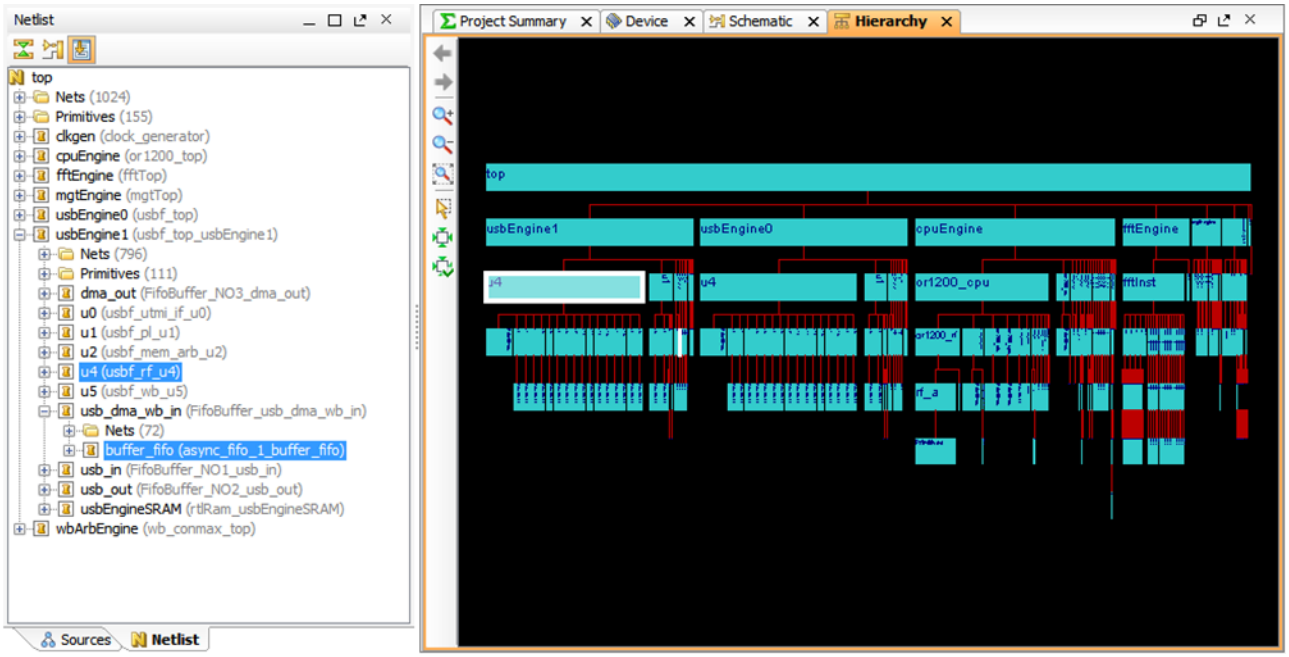


Figure 30: Viewing Hierarchy for Floorplanning

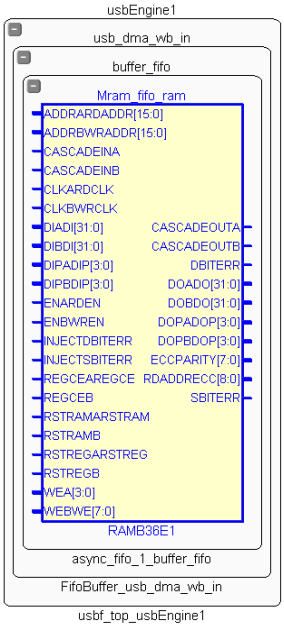
Traversing Schematic Hierarchy

1. Click to display the Schematic view that you opened previously, as shown in FIGURE 30.
2. Click the **Unselect All** button, or press **F12**.

   The levels of hierarchy are drawn with concentric rectangles. It is very easy to identify the logic modules associated with timing path logic.
3. On the left of the Schematic view, select the **RAMB36E1**.
4. In the Schematic view, right-click to open the popup menu, and select **Expand/Collapse > Collapse Outside**.

   The block Ram is isolated.
5. On the upper left of the block RAM symbol, double-click the **ADDRARDADDR[15:0]** pin.

   Double-clicking the outside of a pin expands the schematic outward from the pin. This is the same as selecting the pin and using the **Expand Cone to Primitive** from the popup menu.
6. At the top of the newly added logic, select the **infer_fifo.wr_addr_0** cell.
7. Right-click and select **Expand Cone > To Primitives** from the popup menu, or double click the selected cell.



This adds the logic connected to the selected symbol into the schematic, as shown in FIGURE 31.

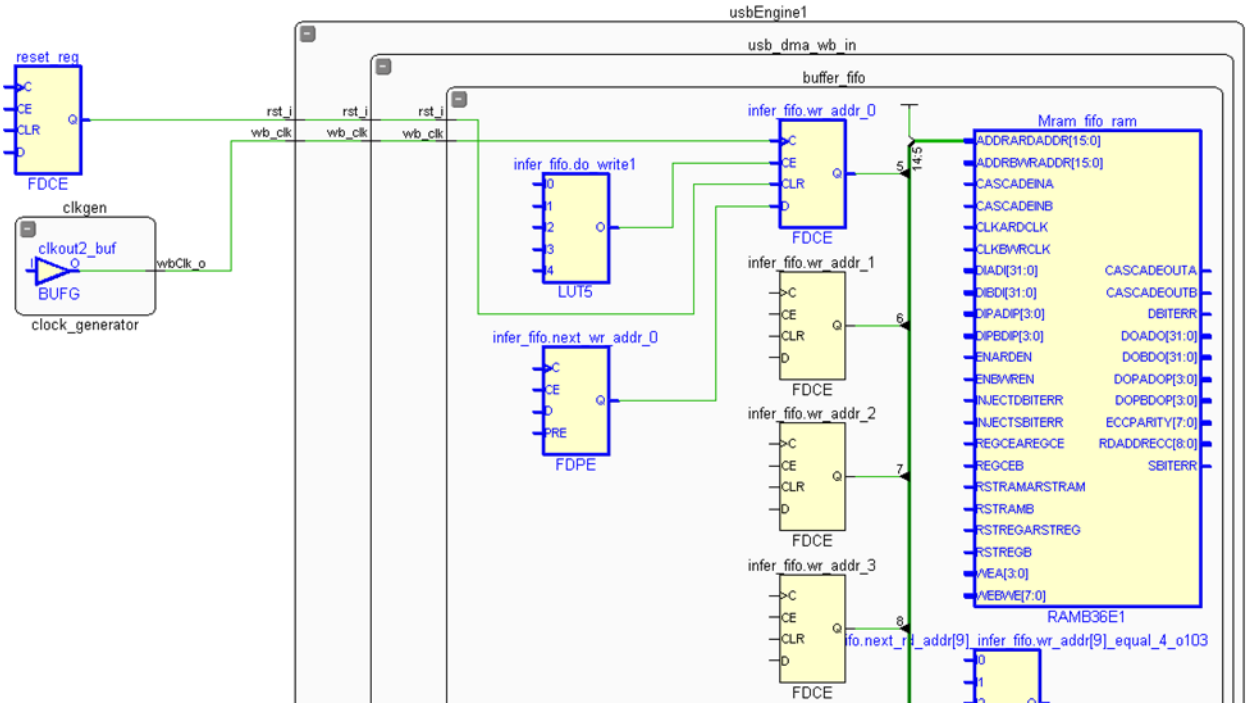


Figure 31: Interactively Expanding Logic in the Schematic View

8. In the Schematic view, select the Previous schematic button.

   You can use the **Previous** schematic and **Next** schematic toolbar buttons to browse the various views displayed in the Schematic view. Switching between views lets you toggle the various levels of schematic expansion.

   Note: The **Edit > Undo** command is not applicable to the Schematic view.

9. Close the Schematic view by clicking the **X** button.
10. Click the **Unselect All** button or press **F12**.
11. In the Netlist view, click the **Collapse All** button.

Conclusion

In this lab, you have opened the CPU HDL project, and examined various aspects of the design using tools available within the PlanAhead tool. You have examined the hierarchy of the design, and the timing report prior to implementation, and synthesized and implemented the design. Finally, you examined the messages and reports generated by the PlanAhead tool.

This concludes Lab #1. You can proceed at this time to Lab #2, or use the following steps to exit the tool:

1. Click **File > Close Project** to close the CPU HDL design.
2. Click **File > Exit** to exit the PlanAhead tool.

Lab 2: Floorplanning the Design

Step 1: Analyzing Placement and Connectivity

Examining the placement and connectivity of the design allows you to develop a strategy for floorplanning to improve placement, routing, and achieve timing closure. The PlanAhead tool has extensive logic expansion and highlighting capabilities. These features can be used to examine the placement achieved through implementation, and identify candidates for floorplanning. For example, tightly grouped and self-contained hierarchical modules may be suitable candidates for floorplanning, while modules that connect to logic scattered throughout the design and across the device may not be suitable.

Highlighting Module Placement

You can analyze the placement of hierarchical modules resulting from prior implementation runs. By examining preliminary implementation results, you can determine a floorplanning strategy to help improve placement, and achieve timing closure and routing.

1. In the Netlist view, select **usbEngine0** and **usbEngine1**.
2. Right-click and select **Highlight Primitives > Cycle Colors**.
3. Click the Device tab to view the highlighting.

   The primitives in each module highlight in a different color, as shown in FIGURE 32.

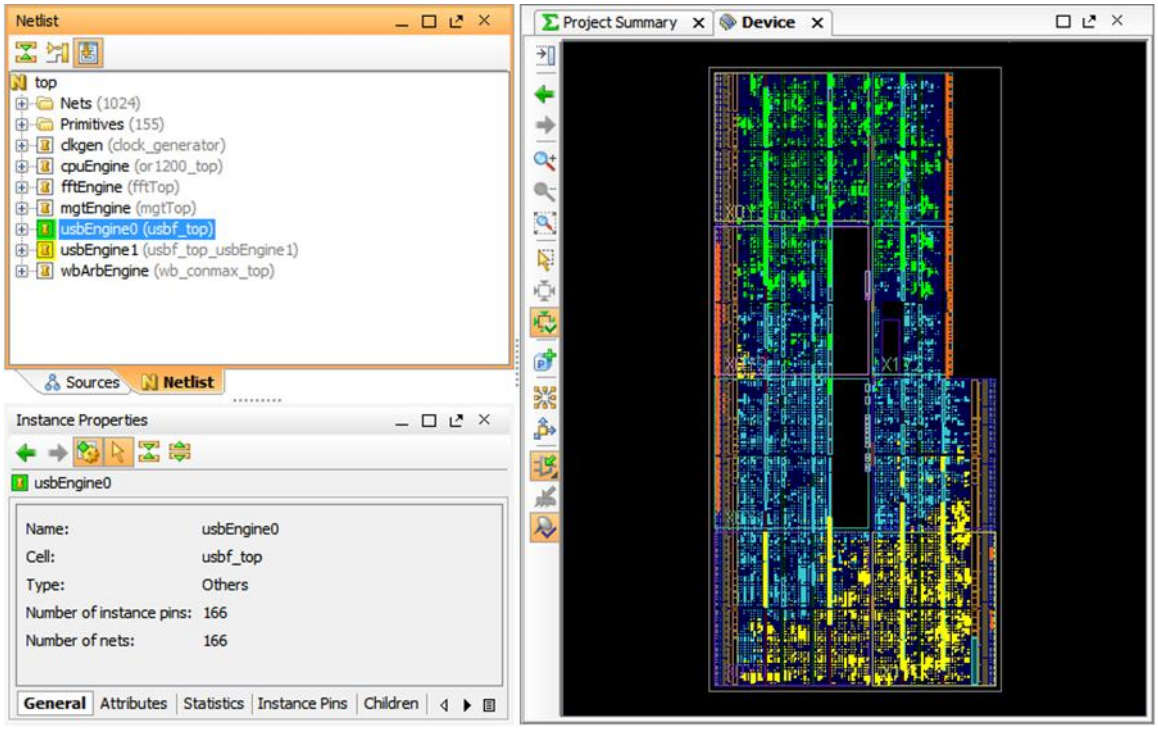


Figure 32: Highlighting Module Placement

Notice the grouped placement of the primitives within each module. Scroll around and change the Zoom level. Notice the logic is spread out. The block RAMs from the two blocks may be intermingled. These modules might benefit from floorplanning to improve timing.

4. In the Device view, click the **Device View Layers** button .
5. Uncheck the box next to **Instances**.

   Various logic elements of the Design, or resources of the Device, can be hidden to make the Device view less cluttered and easier to interpret, as shown in Figure 33.

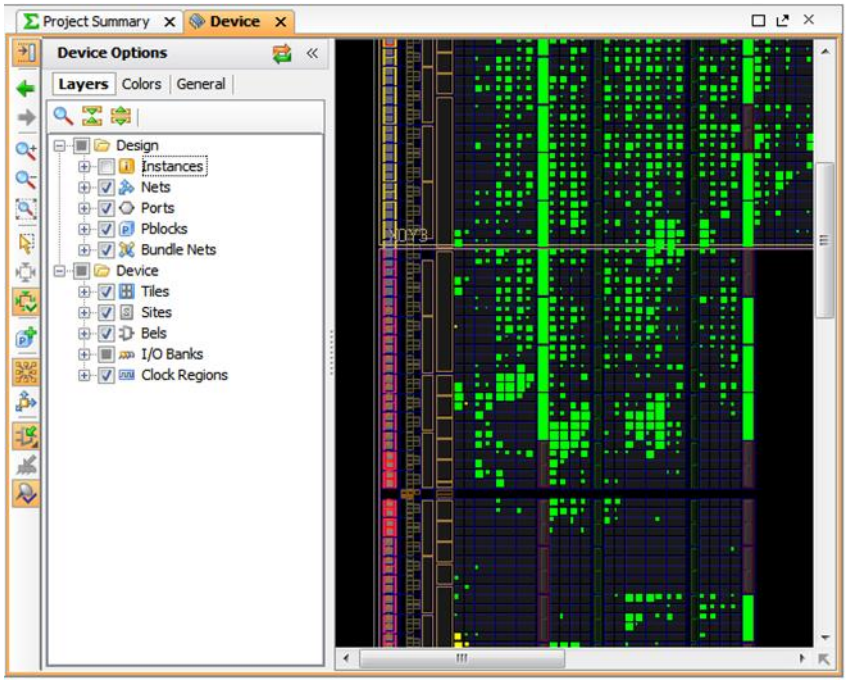


Figure 33: Enabling/Disabling Device View Options

6. Check the box next to **Instances** to restore the placement.
7. Click the **Device View Layers** button to hide the menu.
8. From the main toolbar, click the **Unhighlight All** button .

Visualizing Connectivity

You can show or hide the I/O nets in the Device view, to display connections from placed instances to the I/O Pins. This feature lets you quickly visualize logic that should be placed closer the I/O blocks on the device, and aids in floorplanning and placement of the design.

1. In the Device view, select the **Show I/O Nets** toolbar button

   Examine the connections. Look closely at any connections that cross from one side of the device to the other, or cross a long distance from port to pin. These indicate placement problems that should guide your floorplanning.

2. Click to select one of the I/O Nets.

3. Inspect the net name in the Netlist view, and examine the net properties in the Properties view, as shown in FIGURE 34.

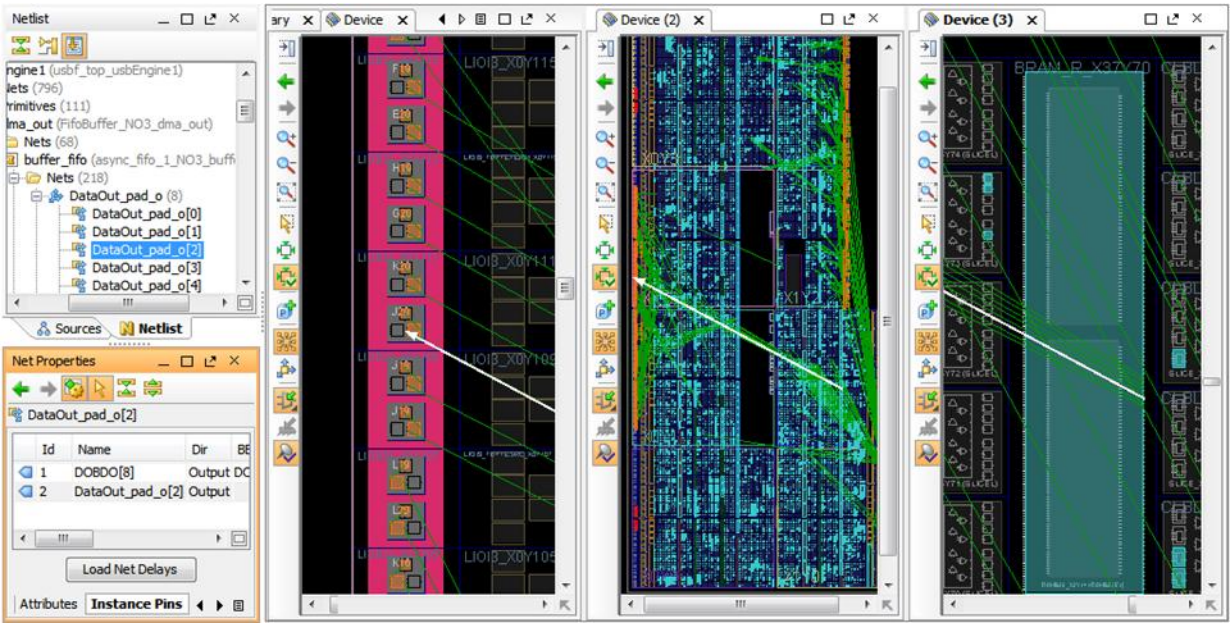


Figure 34: Device View with I/O Connectivity

4. In the Netlist view, click the Collapse All button, and select usbEngine0 and usbEngine1.
5. Right-click and select the **Show Connectivity** popup menu command.

   The interface nets that connect usbEngine0 and usbEngine1 modules to the rest of the design are highlighted, as shown in FIGURE 35.
6. Right-click and select **Show Connectivity** a second time.

   This selects all of the logic objects to which the interface nets connect, expanding outward from the connection to the primitives.
7. Right-click and select **Show Connectivity** a third time.

   This highlights all of the nets that fanout from the selected logic objects.

Note: You can use the Show Connectivity command to highlight or select a cone of logic from any source net or logic object.

8. Click the **Unselect All** button or press **F12.**

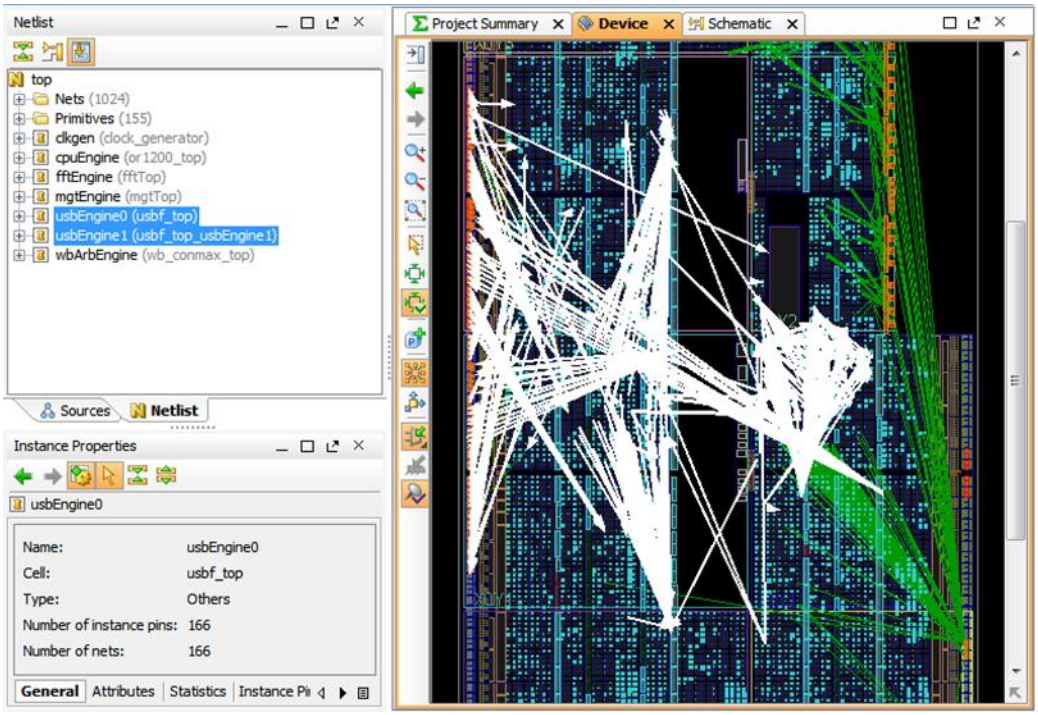


Figure 35: Show usbEngine Module Connections

Step 2: Using Placement Constraints

This step shows how to:

- Search for logic based on primitive type
- Fix placement constraints to prevent logic from being moved in subsequent placement iterations
- Clear the placement of all cells to clear the device for floorplanning.

Finding Cells and Fixing LOCs

1. Select **Edit > Find**.
2. Change the Instances search Criteria to be **Type > is > Block Memory**, as shown in FIGURE 36.

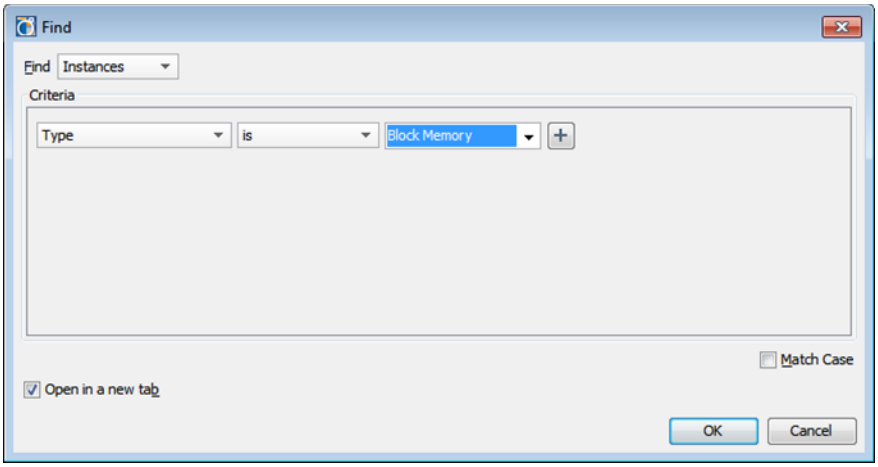


Figure 36: Find Dialog Box

3. Select **OK**.
4. Select any block RAM in the Find Results view.

   The block Ram is selected in the Device view. If the block RAM is too small to see, you can enable the **Auto-Fit Selection** button for the PlanAhead tool to zoom into, and center the selected object.
5. In the Find Results view, press the Shift key and select the first and last block RAM, or press Ctrl+A to select all block RAMs.

   You see all the block RAMs selected in the Device view.
6. Right-click to open the popup menu, and then select **Fix Instances**.
7. In the main toolbar, select the **Unselect All** button.
8. Zoom in and notice that "Fixed" cells display in a different color than unfixed cells, as seen in FIGURE 37.

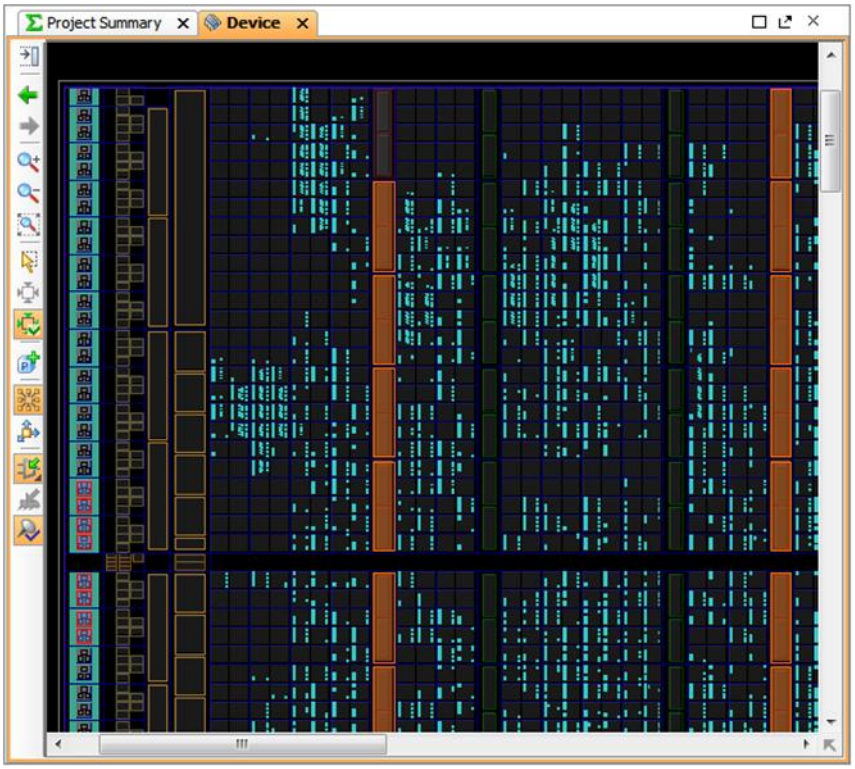


Figure 37: Fixed Block RAMs

IMPORTANT: *Both fixed and unfixed cells are placed. Fixed and Unfixed are terms that describe the way the PlanAhead tool views placed cells in the design.*

- *A Fixed cell is placed by you, or another designer, or was imported from a constraints file. The PlanAhead tool determines that these placed cells are fixed, and are not moved unless explicit direction is provided to do so.*
- *The PlanAhead tool places Unfixed cells during implementation. These placed cells are unfixed, or loosely placed, by the PlanAhead tool, and can be moved as needed in design iterations.*

If you save the design at this point, the **File > Save Constraints** command writes the placement constraints (LOC) to the target constraints file (UCF) for the active constraint set. The placement locks for subsequent implementation attempts.

TIP: *You can use the **Save Constraints As** command to create a new UCF file, leaving the original constraints intact.*

If the design has unsaved changes, PlanAhead prompts you to save upon closing the Implemented Design.

Clearing Placement Constraints

Having fixed the placement for certain cells, you now clear the placement of all cells from the device, to prepare for floorplanning the design.

The **Clear Placement Constraints** dialog box selectively removes placement constraints. The PlanAhead tool provides filters for you to remove placement of specific logic elements selectively.

1. Select **Tools > Floorplanning > Clear Placement**.
2. In the **Clear Placement Constraints** dialog box, select the **Instance placement** radio button, and click **Next**.

   The **Instance Types to Unplace** dialog box presents a list of logic types from the currently selected cells, and lets you selectively clear or keep LOC constraints by logic type.

   Notice that, in FIGURE 38, Clock and IO logic is not selected by default. The I/O and clock related resources are separate from the fabric logic because they do not change as often, and; therefore, might not need to be unplaced.

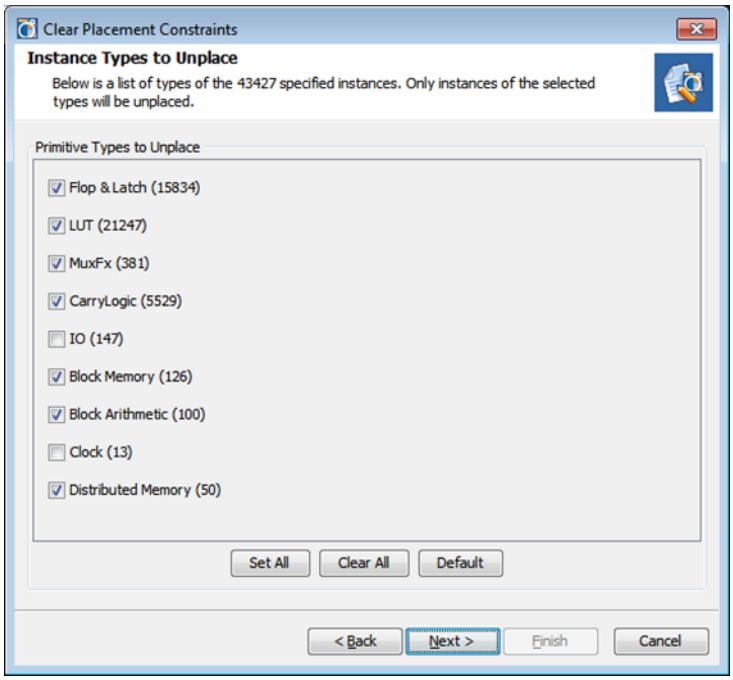


Figure 38: Instance Types to Unplace

TIP: *If you have anything selected when you run the **Clear Placement** command, the **Unplace Instances** dialog box opens before the **Instance Types to Unplace** dialog box. This lets you choose to unplace the selected cells, the unselected cells, or all cells.*

3. Choose **Select all logic types but IO**, to unplace everything but the ports.
4. Click **Next**, as shown in FIGURE 39, to display the **Fixed Placement** dialog box.

   This dialog box displays only when you select fixed cells to be unplaced. In this design the block RAMs are fixed, but you unplace them here.

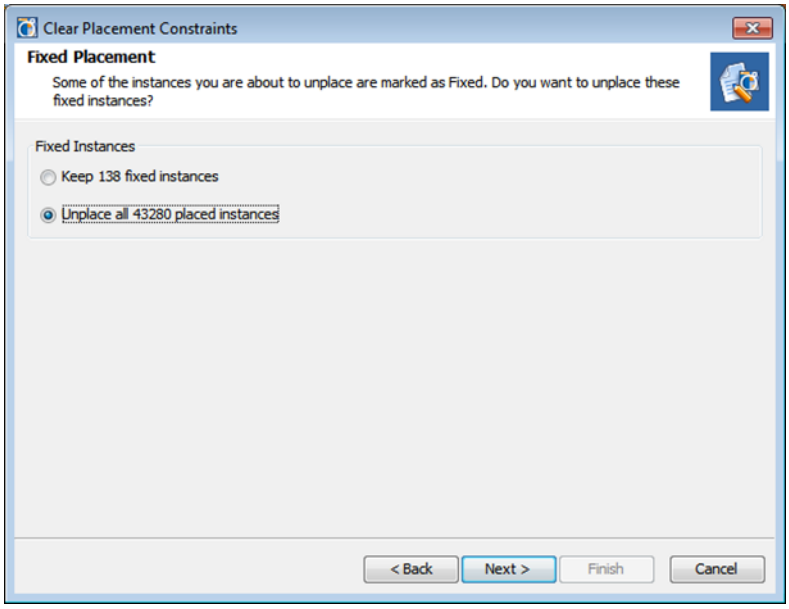


Figure 39: Unplace Fixed Cells

5. Select the radio button next to **Unplace all 43280 placed instances**[2] .
6. Click **Next** to display the **Clear Placement Summary** page.
7. Click **Finish** to clear the placement constraints from the design.
8. In the Netlist view, click the **Collapse All** button. 

[2] The number of placed instances in your design can vary.

Step 3: Floorplanning with Pblocks

The floorplanning process requires the definition of associated groups of logic, called physical blocks, or Pblocks. In this step you will:

- Use various features of the PlanAhead tool to redefine the netlist hierarchy into a physical hierarchy of Pblocks.
- Place the Pblocks and examine the connectivity between them to visualize the design data flow.
- Arrange the Pblocks as a floorplan of the design on the device, and save the placement to the constraints file.

Creating Pblocks

1. From the main menu, select **Tools > Floorplanning > Auto-create Pblocks**.

   The **Auto-create Pblocks** dialog box opens with a list of Pblocks to generate from the netlist hierarchy. The number of blocks to generate, and the minimum primitive count for each block determines the list of blocks. You can change these values as needed so that you are floorplanning the largest blocks in the design. In this case, you use the defaults provided.

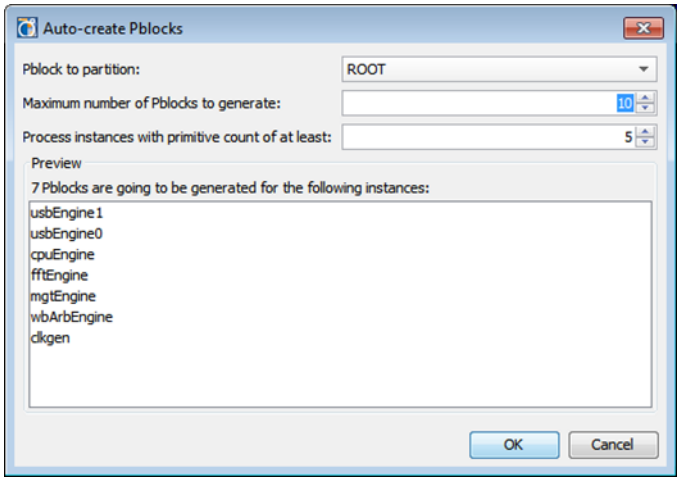


Figure 40: Auto-create Pblocks

2. Click **OK** to accept the default Pblocks.
3. From the View Layout drop-down in the main toolbar menu, select the **Floorplanning** layout

   The Physical Constraints view opens, and lists the newly-created Pblocks.

   In the Netlist view the icon next to the hierarchical modules that are defined as Pblocks changes from  to  , to show that the module is placed in a Pblock.

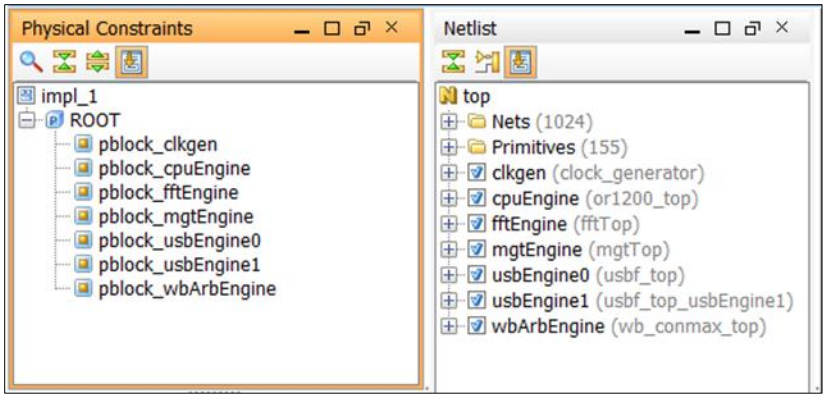


Figure 41: Pblocks in the Physical Constraints View

Placing Pblocks

1. From the main menu, select **Tools > Floorplanning > Place Pblocks**.

   The **Place Pblocks** dialog box opens as shown in FIGURE 42. This dialog box lets you specify the SLICE utilization ratio for all Pblocks, or for each Pblock separately.

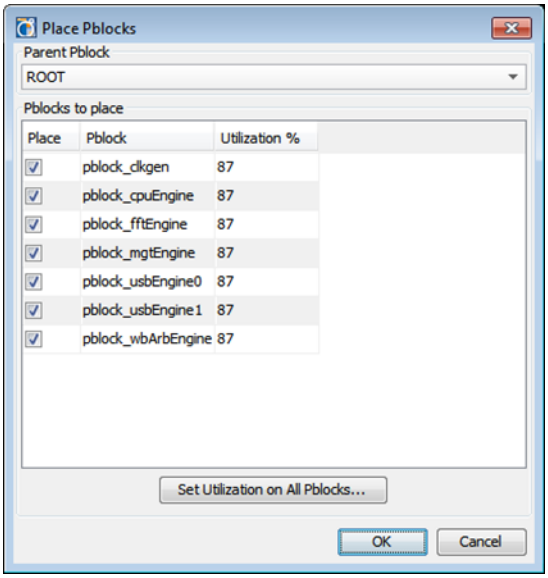


Figure 42: Place Pblocks

IMPORTANT: *The Place Pblocks command is intended to quickly size and place selected Pblocks. Pblocks are sized based upon SLICE logic only. Other non-SLICE logic is not considered in determining the Pblock size. Therefore, the Pblocks created using the Place Pblocks command might need to be resized later to successfully complete implementation.*

2. Click OK to accept the default values, and place the Pblocks.

The tool sizes and places the Pblocks into the Device view as shown in FIGURE 43.

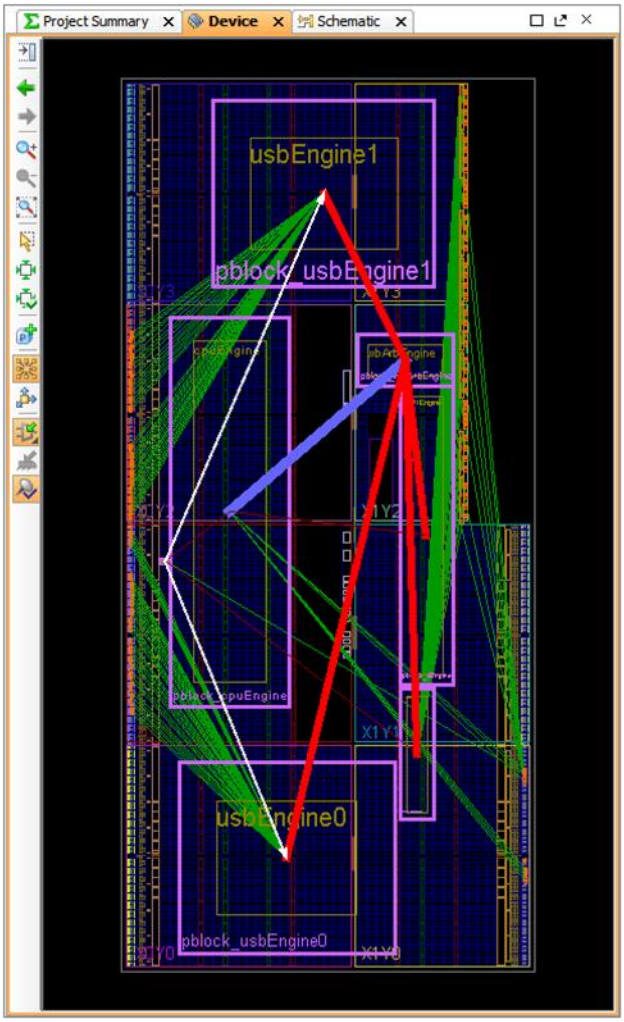


Figure 43: Initial Placement of Pblocks

TIP: *The placement of Pblocks is dependent upon a number of factors, including some randomization of the placement seed, therefore your placement results might differ from what is shown here.*

The bundle net connections between Pblocks and the I/O connections help you visualize the data flow between modules in the design, and highlights areas where potential routing congestion could occur. You can manually rearrange the Pblocks to untangle the connectivity.

If they are not displayed, in the **Device view Options** enable the **Bundle Nets** to display them, and enable the **Show/Hide I/O Nets** toolbar button to show the I/O connections.

The color of the bundle nets also indicates the number of nets shared between two Pblocks. In FIGURE 43, the red bundles indicate between 60 and 200 connections, and the light blue bundle indicates between 200 and 500 connections.

You can see and change the color definition of bundle nets by using the **Tools > Options** command, opening the **Colors** dialog box, and selecting the Bundle Nets tab.

3. In the Device view, select a bundle net.

   The Bundle Nets Properties view displays the list of nets contained within the bundle between two Pblocks, as shown in FIGURE 43 PAGE, 46.

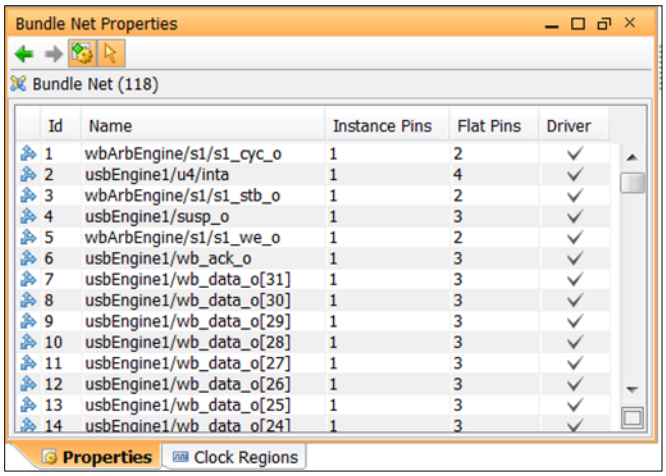


Figure 44: Bundle Net Properties

Finding Global Clocks

In this step, you use the **Find** command to locate and select the USB Global Clock (usbClk) to identify the clocked Pblocks.

Effective floorplanning is often dependent on proper placement of the synchronous elements from different clock domains. You can highlight clock domains to visualize connectivity and ensure that Pblocks are properly placed to effectively utilize clock resources on the device. To learn more about clock resources and clock management, refer to the *Xilinx 7 Series FPGAs Clocking Resources User Guide (UG472)*, or to the appropriate guide for the target device.

1. Select **Edit > Find**.
2. In the **Find** dialog box, set the following options:
   - Find: **Nets**
   - First field: **Type**
   - Second field: **is**
   - Third field: **Global Clock**
3. Ensure to check the **Unique Nets Only** checkbox, and click **OK**.
4. In the Find Results view, click the **Name** column header once to sort the column, and select **clkgen/usbClk_o**.

Notice the selected net, highlighted in white in FIGURE 43 PAGE, 46., leading from the `clkgen` Pblock to the two `usbEngine` Pblocks.

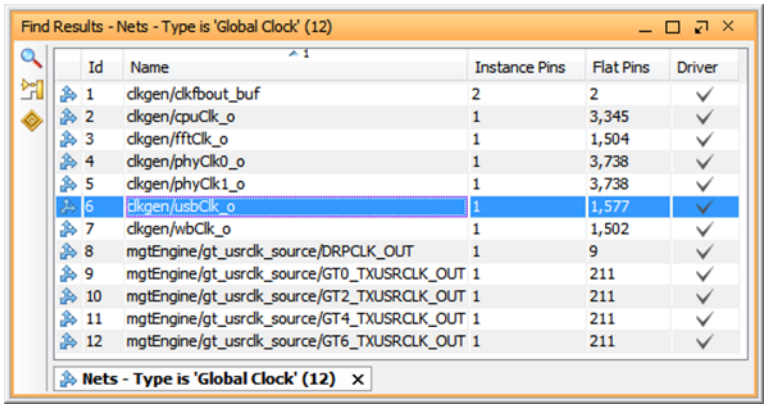


Figure 45: Selecting the Global Clock

Moving and Resizing Pblocks

With an initial placement of the Pblocks, you can begin to rearrange the Pblocks to better visualize the data flow through the design. This requires moving the Pblocks on the device, and possibly resizing the Pblocks.

To better focus on the two `usbEngine` blocks that you identified for floorplanning, select and clear the other Pblocks from the Physical Constraints window.

1. In the Physical Constraints window, select `pblock_cpuEngine`, `pblock_fftEngine`, `pblock_mgtEngine`, `pblock_clkgen`, and `pblock_wbArbEngine`.
2. Right-click and open the popup menu, then select the **Delete** command.

   This deletes the selected Pblocks, leaving only the `usbEngine0` and `usbEngine1` Pblocks. The other Pblocks helped you understand the data flow through the different modules of the design, but you do not need them for the final floorplan.
3. In the Physical Constraints view, select the `usbEngine0` Pblock, or select it directly in the Device window.
4. Move the Pblock by dragging it to a location on the lower half of the Device view.

   The placement you choose should seem appropriate based on the displayed connections between the Pblocks and to the I/O ports. To reduce timing delay, you should place the Pblock near the I/O ports to which it is connected.

When you place the Pblock in its new location, the **Move** dialog box, shown in FIGURE 46, prompts you to select which resource types in the new location to enable for use by the Pblock.

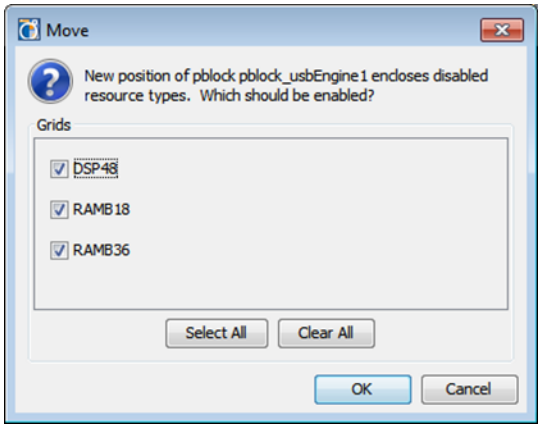


Figure 46: Move Pblock

5. Select **OK** to include all resource types in the moved Pblock.
6. Select the `usbEngine1` Pblock in the Physical Constraints view, or select it directly in the Device window.
7. Move it by dragging it to the top half of the Device view.

   Again, the placement of the Pblock should be based on its connections, and you will again be prompted by the **Move** dialog box as seen in FIGURE 46.

   With the `usbEngine` blocks placed approximately where you want them, in the upper and lower half of the Device view, you must now resize the Pblocks to include the required resources.
8. In the Physical Constraints view, select the usbEngine0 Pblock, or select it directly in the Device window.
9. Right-click in the Device view to open the popup menu, and select the Set Pblock Size command.

   The cursor turns to a cross-hair.
10. Draw a rectangle over **clock region X0Y1**, on the left side the Device view.

    The **Set Pblock** dialog box opens. If you have sized the rectangle along the clock region borders, you are prompted to confirm the entire Clock Region as the resource for the Pblock.

If not, the tool prompts you to indicate the specific device resources available for use by the Pblock, as shown in FIGURE 47.

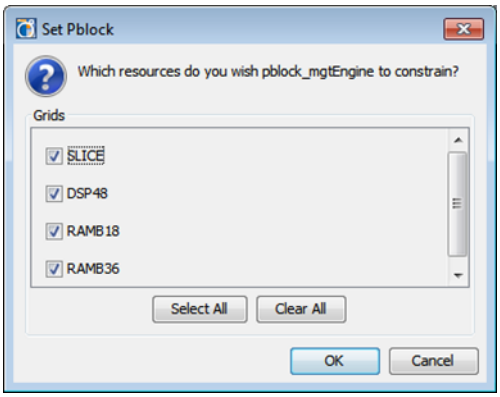


Figure 47: Set Pblock Size

11. Click **OK** to accept either.

    If a **Choose LOC mode** dialog box, as seen in FIGURE 48, opens during the move or resize, it means that some logic cells were placed inside the Pblock, and they are now being moved or resized out of the Pblock.

    For this design some registers are embedded in the I/O pads. The placement of these cells was not cleared during **Clearing Placement Constraints** because I/O placement was not cleared.

    If a Pblock covers these I/Os, but then is moved or resized so they are not covered, the PlanAhead tool prompts you to decide how these placement constraints should be handled.

12. For this tutorial, leave the LOCs in their original positions. Accept the default and click **OK**.

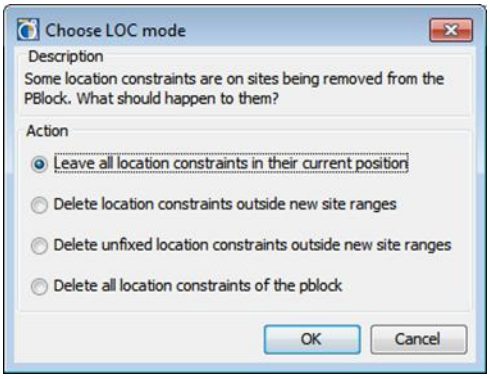


Figure 48: Choose LOC Mode

13. Look at the Pblock Properties view, and click the Statistics tab.

The Statistics tab of the Pblock Properties window, as seen in FIGURE 49, shows the Physical Resource Estimates for the Pblock. These statistics display the following:

- The different site types available on the device in the area covered by the Pblock
- The amount of resources required by the logic assigned to the Pblock
- The current utilization %.

The red values indicate there are insufficient resources available to meet the requirements of the design logic assigned to the Pblock. In this case, the Pblock must be resized to increase its resources, or the design will not complete implementation.

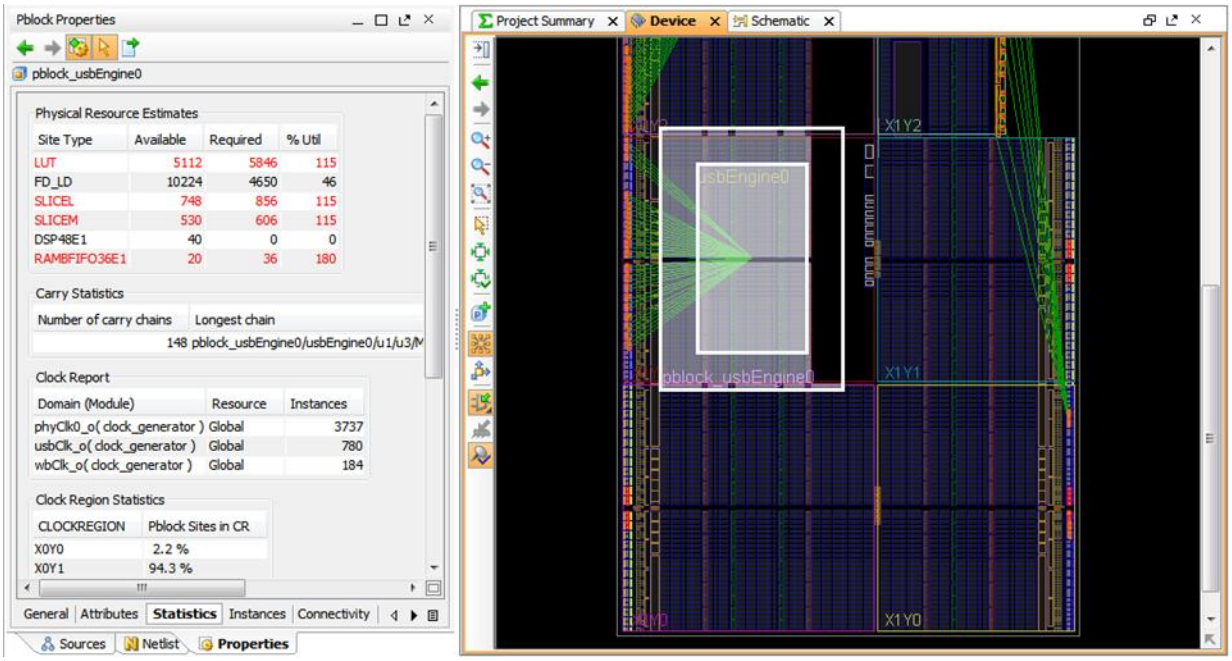


Figure 49: Pblock with Insufficient Resources

14. Scroll down to the bottom of the Pblock Properties view and examine the information provided.
15. Resize the `usbEgine0` Pblock to cover **Clock Regions X0Y0 and X0Y1**, and click **OK** to accept the Clock Regions as the Pblock range.

    The Physical Resource Estimates in the Pblock Properties view should now reflect sufficient resources for the required logic.
16. Select the `usbEngine1` Pblock and resize it to cover the two Clock Regions above the `usbEngine0` Pblock, `X0Y2` and `X0Y3`.

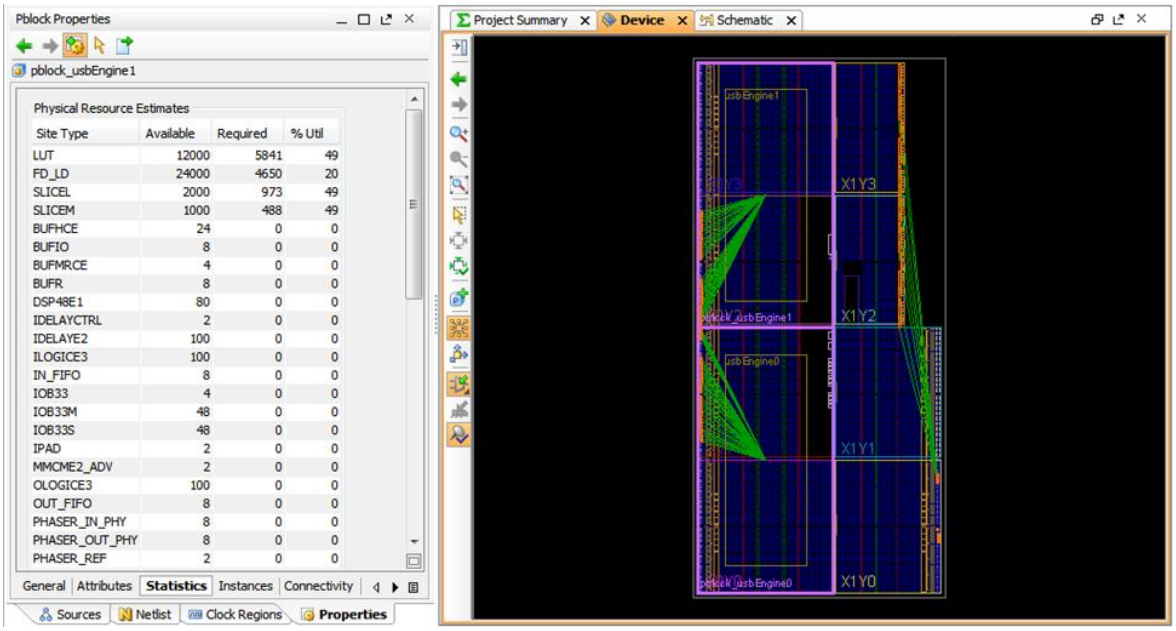


Figure 50:Pblocks with Sufficient Resources

Your design should now look like FIGURE 50. The two Pblocks are placed and sized appropriately, and you are now ready to run the floorplan through place and route. However, you first need to save the Pblock constraints.

17. Select **File > Save Constraints As**, as shown in FIGURE 51, and click **OK**.

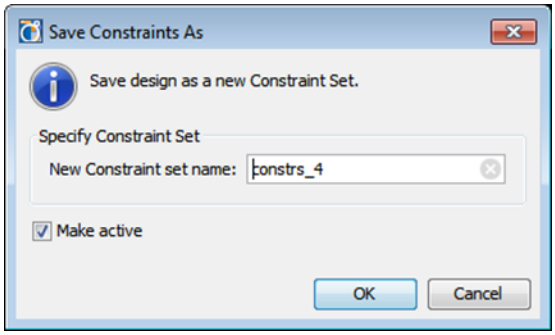


Figure 51: Save Constraints As

When you save as this configuration you leave the current implementation constraints alone, and save the new floorplan constraints to a new constraint set. This preserves the prior implementation results, while allowing you to move forward with your new floorplan.

TIP: *Notice the dialog default settings will create a new constraint set and make it active for the next run. This method will preserve your original constraints files*

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18. In the top right of the Implemented Design view banner, click **X** to close the view.
19. Click **OK** to exit, and click **No** if prompted to save.

    The Implemented Design closes, and the PlanAhead tool returns to the Project Manager.

Step 4: Implementing the Floorplan

The PlanAhead tool saves the floorplan in the `top_full.ucf` constraints file in the new constraint set, `constrs_4`. You can now implement the design with the floorplan constraints to improve the timing of the design.

1. In the Sources view, double-click `top_full.ucf` in `constrs_4` to open the file in the Text Editor.

   Notice the format of the original UCF constraints file was maintained. The tool added the `AREA_GROUP` constraint at the bottom of the file.

2. Scroll to the bottom of the file and notice the new `AREA_GROUP` lines.

   These lines constrain the hierarchical modules, and logic from those modules, to regions of the device, and to resources within those regions.

3. Close the `top_full.ucf` file in the Text Editor.

   Recall that you created multiple implementation runs earlier in this tutorial, in CREATING IMPLEMENTATION RUNS. You now use one of those runs to implement the design with the floorplan constraints.

4. In the Design Runs view, select the `impl_2` run.

5. With the run selected, look at the Implementation Properties view.

   The Implementation Properties view displays the properties of the selected run, as shown in FIGURE 52. If the Properties view is not open, you can use the **Window > Properties** command to open it.

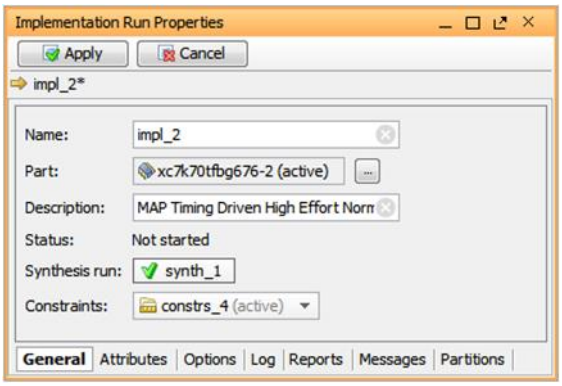

Figure 52: Implementation Properties

6. Change the **Constraints** field to select the `constrs_4` constraint set.

Note: If you did not complete, or save the floorplan from the previous steps, constraint set `constrs_3` includes a completed floorplan in the `top_fpln.ucf` constraints. You can select constrs_3 here if needed.

7. In the Implementation Properties view, click the **Apply** button as shown in FIGURE 52.

8. With `impl_2` selected in the Design Runs view, right-click to open the popup menu and select **Make active**.
9. From the Flow Navigator menu, select **Run Implementation**.

   This launches the implementation run with the `usbEngine` blocks placed according to your floorplan. The **Implementation Completed** dialog box displays when the run is finished.
10. In the **Implementation Completed** dialog box, select **Open Implemented Design**, and click **OK**.

    The design has been implemented with the floorplan you created for the `usbEngine` blocks. You can see this by highlighting the blocks as you did earlier in this tutorial.
11. In the Netlist window, select `usbEngine0` and `usbEngine1`.
12. Right-click for the popup menu, and select **Highlight Primitives > Cycle Colors**.

    You can see the new placement implemented as a result of the floorplan strategy you developed in this tutorial. You can compare it to the prior placement results from the first implementation pass. See FIGURE 53 for current results, and Figure 32 for prior results.

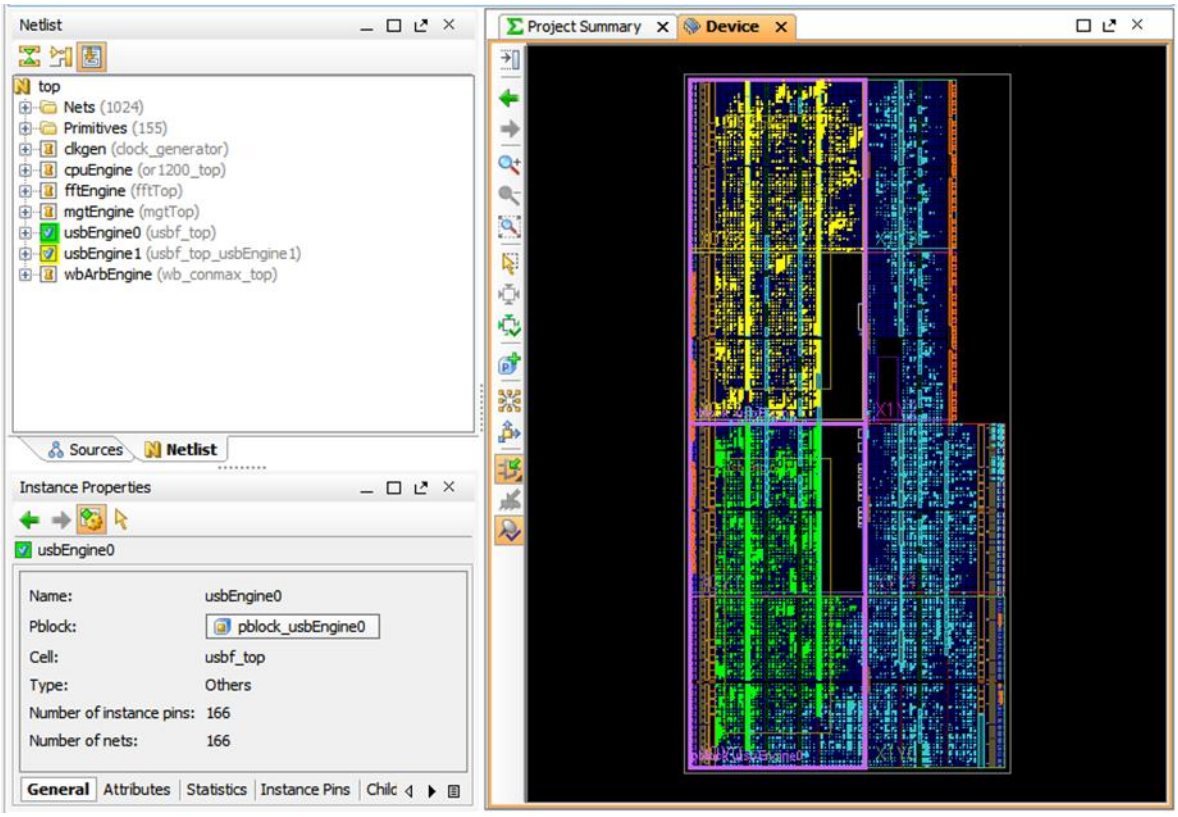

Figure 53: Implemented Floorplan

13. Select **File > Exit** and click **OK** to confirm.

    The PlanAhead tool closes.

Conclusion

In this tutorial, you used the PlanAhead software to explore and analyze the synthesized design and targeted device prior to running the implementation tools. This enabled you to find potential design issues and errors early in the design cycle, rather than discovering issues during implementation. In addition, you used the graphical presentation of design resource estimates, design rule violations, timing estimation, constraints, and connectivity to help you understand your design and any potential areas with issues.

After running the design through the synthesis and implementation tools, you:

- Viewed implementation results and examined timing results.
- •Analyzed critical path objects in the schematic, and selected the parent modules of those path objects.
- Highlighted module placement and displayed the connectivity of the modules using the Show Connectivity command.
- Analyzed placement and routing of critical timing paths.
- Floorplanned the possible placements based upon the hierarchy of the design.
- Implemented the floorplanned design.