

# ChipScope Pro Tutorial:

## *Using IBERT with ChipScope*

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This document applies to the following software versions: ISE Design Suite 14.5 through 14.6





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## Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/24/2012	14.1	Revalidated for the current release. Editorial updates only; no technical content updates.
07/25/2012	14.2	Revalidated for the current release. Editorial updates only; no technical content updates.
10/16/2012	14.3	Revalidated for the current release. Editorial updates only; no technical content updates.
12/18/2012	14.4	Revalidated for the current release. Replaced Figure 1 and some editorial corrections made.
02/28/2013	14.5	Updated to Kintex-7 KC705 board with 2D Eye Scan sweeping and plotting.

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# Tutorial: Using an IBERT Core with ChipScope Pro Analyzer

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## Introduction

In the course of this tutorial you will:

- Create, customize, and generate an Integrated Bit Error Ratio Tester (IBERT) core design using the standalone CORE Generator™ tool.
  - Interact with the design using ChipScope™ Pro Analyzer. This includes importing the bitstream file into ChipScope Pro Analyzer, configuring the device, and interacting with the IBERT/Transceiver IP cores.
  - Perform a sweep test to optimize your transceiver channel and to plot data using the IBERT sweep plot GUI feature that was introduced in software version 14.5.
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## Prerequisites

A basic knowledge of Xilinx® tool flows.

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## Setting Up

### Parts Required

Ensure that you have the following software and hardware:

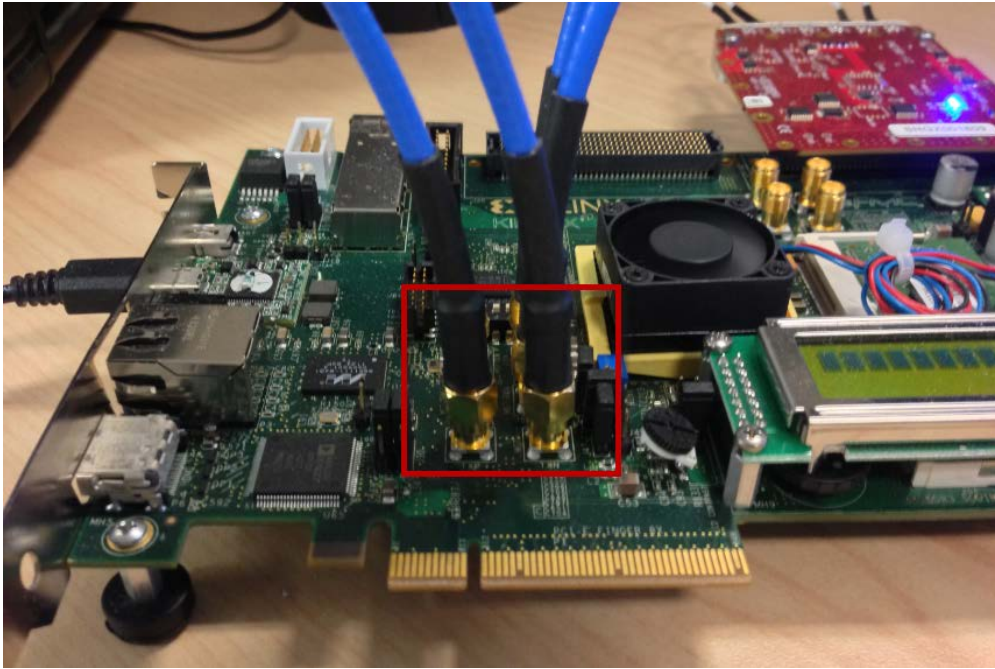
- Xilinx ISE Design Suite 14.5 (Logic, DSP, Embedded, or System Edition)
- Kintex-7 KC705 board
- JTAG USB cable delivered with the KC705 board
- Two SMA (Sub-miniature version A) cables

### Connecting the Board and Cables

1. Connect the USB cable from the USB JTAG connector on the board to your computer system.
2. Connect the two SMA cables:

- a. Connect one SMA cable from J19 (TXP) to J17 (RXP).
- b. Connect the other SMA cable from J20 (TXN) to J66 (RXN).

The relative locations of connectors on the board are shown in Figure 1.



**Figure 1: SMA Cable Connections**

3. Turn the KC705 power switch on.

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## Design Description

You can customize the ChipScope Pro Analyzer IBERT core and use it to evaluate and monitor the functionality of transceivers for a variety of Xilinx devices. The focus for this tutorial is on Kintex®-7 GTX transceivers. The design includes pattern generators and checkers implemented in FPGA logic, as well as access to the ports and dynamic reconfiguration port (DRP) attributes of the GTX transceivers. Communication logic is included to allow the design to be runtime-accessible through JTAG. The IBERT core is a self-contained design. When generated, it runs through the entire implementation flow, including bitstream generation.

The IBERT design is auto-generated according to your specific customization in the Xilinx CORE Generator tool, so no additional example design is required for this tutorial.

Figure 2 shows a block diagram of the interface between the IBERT Kintex-7GTX core interfaces with Kintex-7 transceivers.

- **DRP Interface and GTX Port Registers:** IBERT provides you with the flexibility to change GTX transceiver ports and attributes. Dynamic reconfiguration port (DRP) logic is included, which

allows the runtime software to monitor and change any attribute in any of the GTX transceivers included in the IBERT core. When applicable, readable and writable registers are also included. These are connected to the ports of the GTX transceiver. All are accessible at runtime using the ChipScope Pro Analyzer tool.

- **Pattern Generator:** Each GTX transceiver enabled in the IBERT design has both a pattern generator and a pattern checker. The pattern generator sends data out through the transmitter.
- **Error Detector:** Each GTX transceiver enabled in the IBERT design has both a pattern generator and a pattern checker. The pattern checker takes the data coming in through the receiver and checks it against an internally generated pattern.

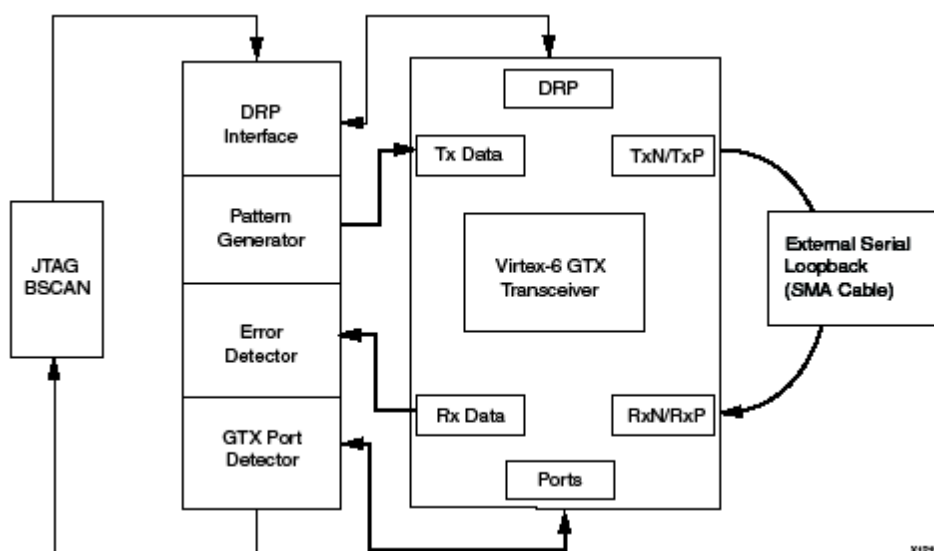
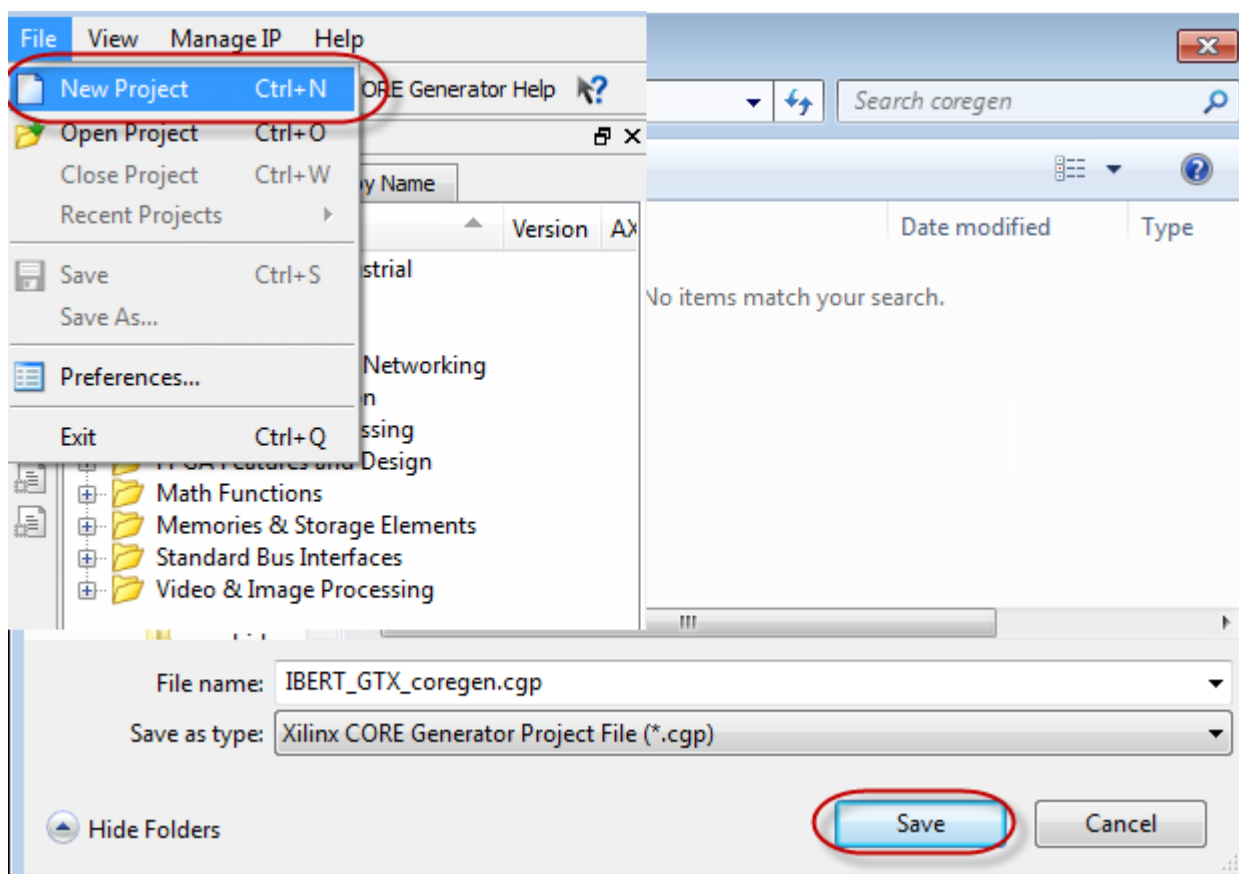


Figure 2: IBERT Design Flow

## Step 1: Creating, Customizing, and Generating an IBERT Design

1. Open the Xilinx CORE Generator tool.
2. Click **File > New Project** and save the project as **IBERT\_GTX\_coregen**, as shown in Figure 3.



**Figure 3: Creating and Saving a Project in the CORE Generator Tool**

3. When you save the project, the Project Options dialog box opens.
  - a) With the Part option selected:
    - Set Family to **Kintex7**.
    - Set **Device** to **-xc7k325** (the device on the KC705 board).
    - Set **Package** to **ffg900**.
    - Set **Speed Grade** to **-2**.
  - b) Use the default settings for all other project options (Generation and Advanced).
  - c) Click **Apply**, then **OK**.
4. Select the IBERT IP core to generate.  
In the IP Catalog pane, double-click **Debug & Verification > Debug > IBERT 7 Series GTX (ChipScope Pro-IBERT)**.
5. In the board configuration settings dialog box for the core, shown in Figure 4, locate the **Board Configuration Settings** drop-down menu and select **kc705 bank117**

**Note:** If you do not see the drop-down items shown in Figure 4, you might have selected the wrong device in step 2, above.

**Note:** The **Board Configuration Settings** drop-down menu includes **User Defined**, along with three other pre-configured board settings that target a KC705 board, including the one you selected. Each of the pre-configured board selections provides all the pre-settings you need. This is useful when you want to evaluate your design environment quickly, or when you want to explore certain pre-configured board functions. In addition, you can use the pre-settings as a template for your own User Defined settings. The User Defined option requires that you familiarize yourself with parameters such as clock, pin location, and protocol type. When you choose a pre-configured board selection, this is not necessary.

**IBERT 7 Series GTX (ChipScope Pro - IBERT)**

Component Name:

Board Configuration Settings: **kc705 bank117**

Generate Bitstream

When using ISE, enable 'Generate Bitstream using ISE tools' checkbox

☒ Generate Bitstream using ISE Tools

When using Vivado, source the generated v\_rdi\_implement.tcl

System Design

☐ Add RXOUTCLK probe

GTX Naming Style:  ex. MGT0\_113 / MGTREFCLK0\_113

System Clock

☒ Use External clock source

☐ Enable Diff Term

Frequency:  MHz

P Pin Location:

N Pin Location:

Pin Input Standard:

Silicon Version

Silicon Version:

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**Figure 4: Board Configuration Settings Dialog Box**

- Click **Next** and review the pre-configured parameters.



7. When finished, click **Generate** to start generating the IBERT design. It might take a few minutes to generate the core.

After the IBERT design is generated, a **Readme chipscope\_ibert** pop-up box appears.

8. Take a look at the various files that are generated and click **Close**.

You just finished creating a project file in the CORE Generator tool, and you customized and generated the IBERT design. Next, you will learn how to interact with this design using ChipScope Pro Analyzer.

## Step 2: Interacting with the Design Using ChipScope Pro Analyzer

In this tutorial step, you use ChipScope Pro Analyzer to interact with the IBERT design that you created in Step 1. You perform some analysis using various input patterns and loopback modes, while observing the bit error count.

1. Start ChipScope Pro Analyzer.
2. In the menu bar, click **JTAG Chain > Server Host Setting > set appropriate Server**.  
**Note:** By default, the **Server** is set to **localhost:50001**.
3. In the menu bar, click **JTAG Chain > Digilent USB JTAG Cable**.
4. The ChipScope Pro Analyzer [new project] dialog box opens. Accept the default settings.
5. The ChipScope Pro Analyzer dialog box opens. Accept the default settings.

### Configuring the Device

1. In the ChipScope Pro Analyzer main window, in the New Project pane, right-click **DEV: 0 MyDevice0 (XC7KC705T)**, and select **Configure** from the resulting menu.
2. In the pop-up dialog box, click **Select New File**, browse to the `example_chipscope_ibert.bit` file, and click **OK** to start downloading the bit file onto the KC705 board.
3. In the ChipScope Pro Analyzer main window, in the New Project pane, expand **DEV: 0 MyDevice0 (XC7KC705T)** and double-click **IBERT Console**.

**Note:** The ChipScope Pro Analyzer - IBERT V6TX Project Settings prompt might appear at this point, asking if you want to set up the core with settings from the current project. If you see this prompt, click **Yes**.

4. With initial settings on the loopback modes, the interactive IBERT Console window appears, as shown in Figure 5.

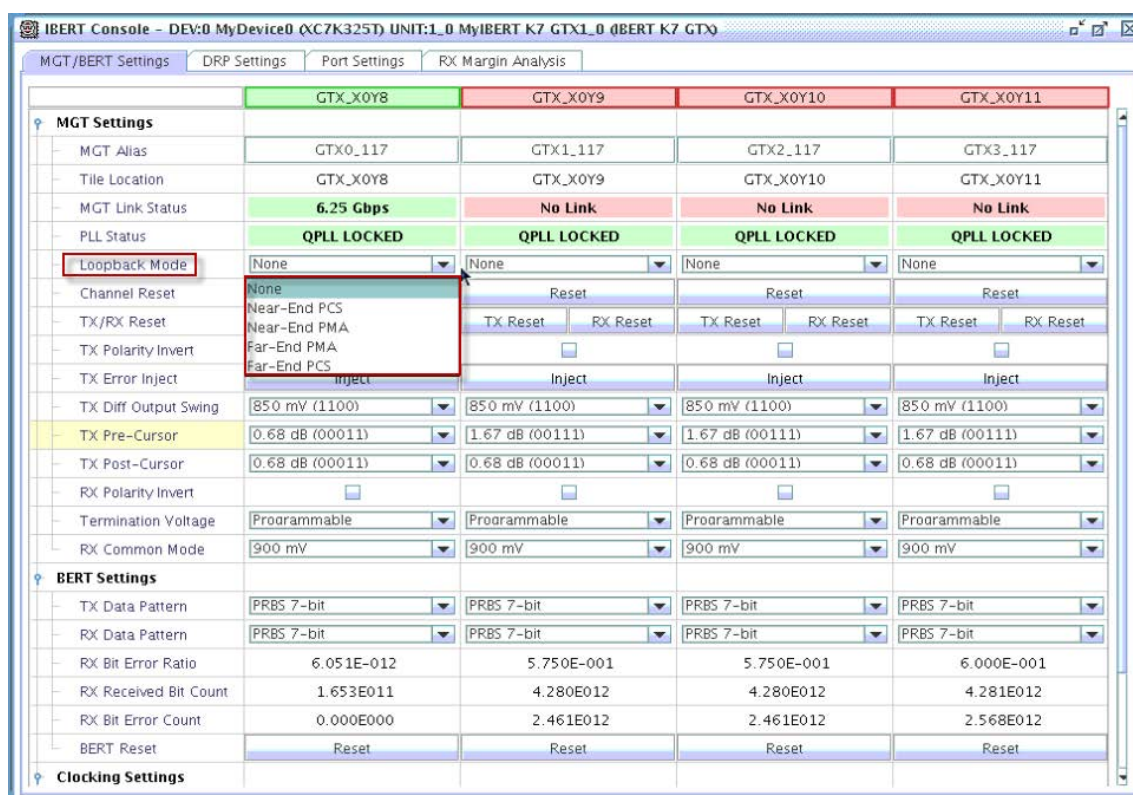


Figure 5: IBERT Console Window for Kintex-7 FPGA GTX Transceivers

## IBERT Console Window Key Features

Note the four settings tabs at the top of the console window. Associated with each is a table in which the rows typically describe a function that you can control dynamically or that can serve as a status monitor.

For example, you can configure the Loopback Mode function by selecting one of the available settings from the pull-down menu.

Look at the Loopback Mode setting, which controls the loopback mode of a particular GTX transceiver channel. Each GTX/GTH transceiver features several loopback modes to facilitate testing:

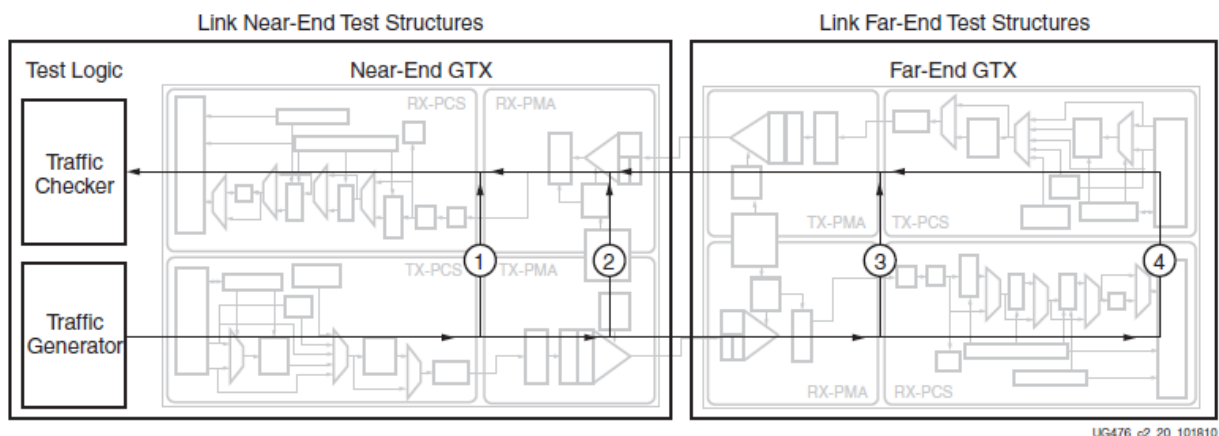
- Near-End PCS Loopback (path 1)

The RX elastic buffer must be enabled and RX\_XCLK\_SEL must be set to RXREC for Near-End PCS loopback to function properly. While in Near-End PCS loopback, the RX XCLK domain is clocked by the TX PMA parallel clock (TX XCLK).

- Near-End PMA Loopback (path 2)
- Far-End PMA Loopback (path 3)

The TX buffer must be enabled and TX\_XCLK\_SEL must be set to TXOUT for Far-End PMA loopback to function properly. While in Far-End PMA loopback, the write side of the TX buffer is clocked by the RX PMA parallel clock (RX XCLK).

- Far-End PCS Loopback (path 4)



**Figure 6: GTX Loopback Path**

In the IBERT console, you can see that only the GTX\_X0Y18 transceiver channel has established a 6.25 Gbps line rate link between the TX and RX channels. This is because it is the only channel being looped back between TX and RX by SMA cables. The other three channels display as **No Link**.

The GTX\_X0Y18 transceiver is the only channel in KC705 BANK 117 that can be looped back using SMA cables, as shown in the KC705 schematics (Figure 7).

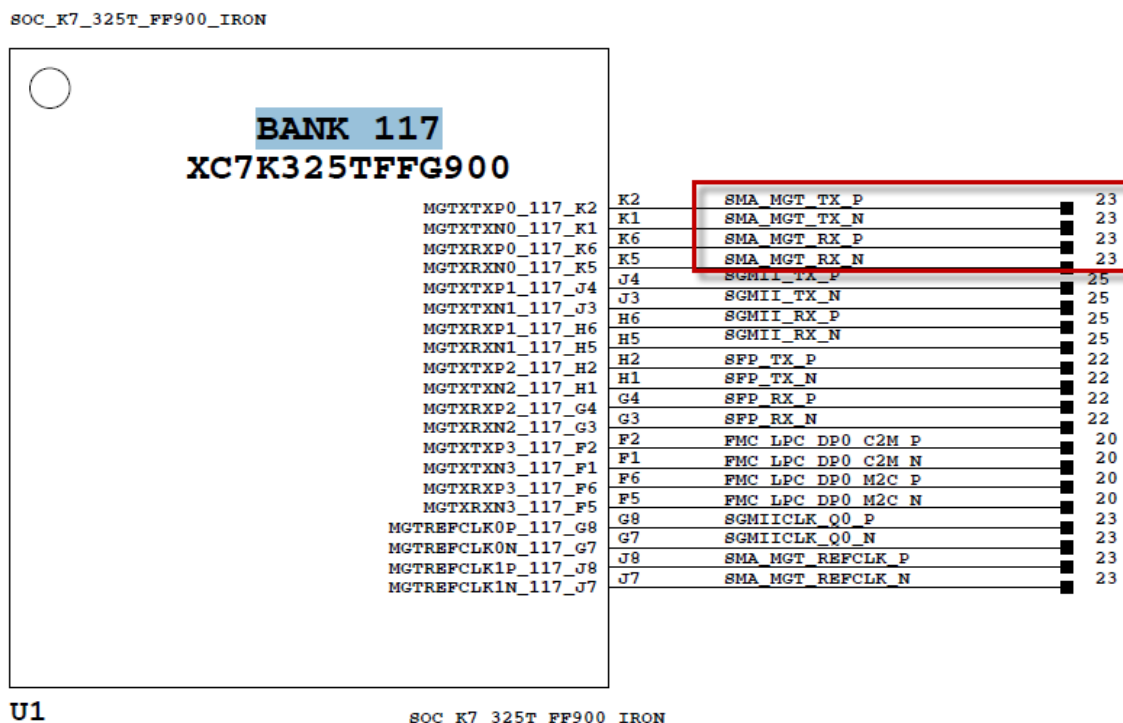


Figure 7: KC705 Schematics for Loopback using SMA Cables

For more details about the IBERT Console Window for Kintex-7 GTX Transceivers, see the *ChipScope Pro Software and Cores User Guide, UG029* at <http://www.xilinx.com/tools/cspro.htm>.

## Step 3: Performing a Sweep Test

### Overview

For Kintex-7 GTX, Virtex-7 GTX/GTH/GTZ, and Artix-7 GTP, you can perform RX Margin Analysis with two different scan algorithms using ChipScope Pro Analyzer:

- 2D Full Scan: Scans all horizontal and vertical offset sampling points within the "eye".
- 1D Bathtub: Scans all horizontal sampling points through the 0 vertical row offset.

For this tutorial, we will focus on the 2D Full Scan algorithm only.

In this final step, you perform a sweep test on a channel using various transceiver settings. You:

- Open the Sweep Test Settings panel and review sweep test parameters.
- Set up to run the sweep test.
- Run the sweep test.
- Plot the data using the IBERT Sweep Plot GUI.

## Opening the Sweep Test Panel and Reviewing Sweep Parameters

From the **IBERT** Console, click the **RX Margin Analysis** tab to open the panel in which you can set parameters for the sweep test.

Figure 8 shows the Sweep Test Panel Parameters and Options and the Sweep Test Settings panel. Some key options are circled in red.

In the Sweep Test Settings panel you can set up a channel test that sweeps through a variety of transceiver settings.

The TX and RX settings are for the same GTX transceiver. The Sweeping through both TX and RX settings works only if the transceiver is set to one of the near-end or external loopback modes.

You can use the Sweeping through RX parameters only when the corresponding TX endpoint for the link resides in a different device or a different transceiver in the same device.

Note that the Rx Margin Analysis panel is divided into four areas:

- MGT/Parameter Settings
- Scan Settings
- Test Controls
- Test Results

In this section of the tutorial, you perform a sweep test of the GTX\_X0Y18 transceiver channel.

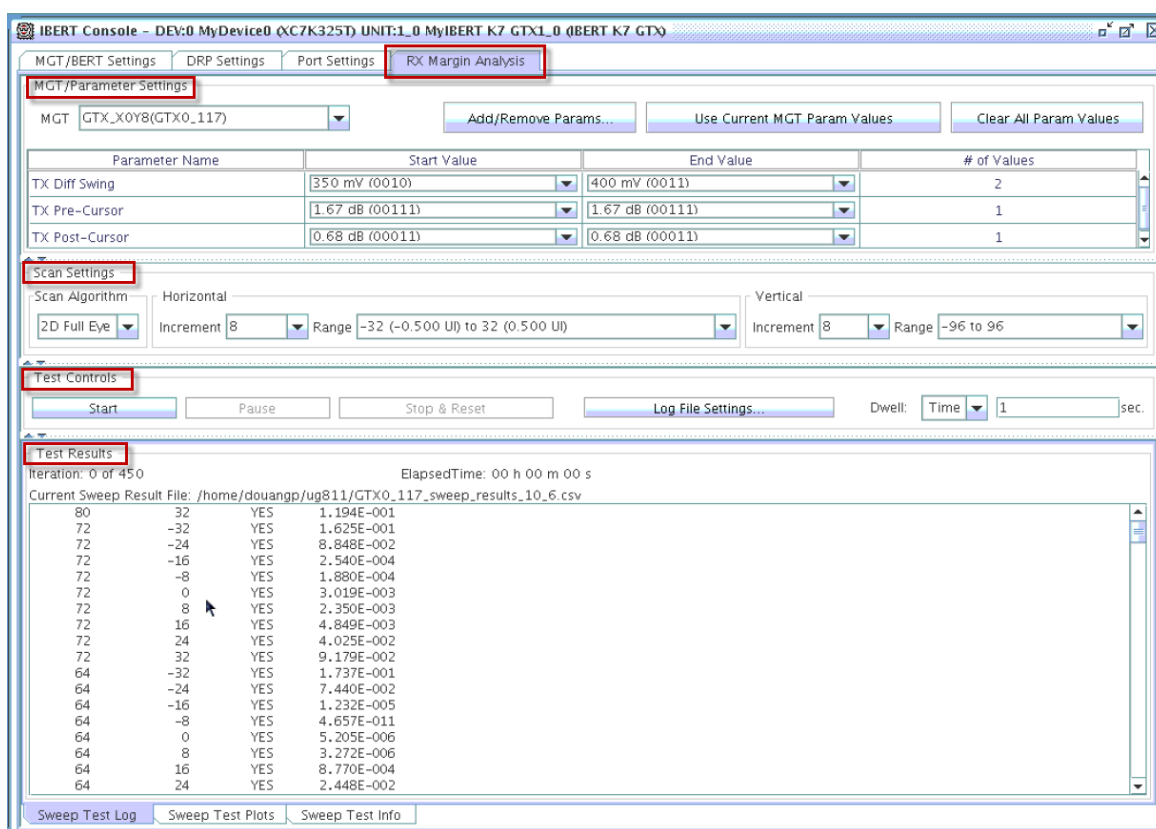


Figure 8: Sweep Test Settings Pane

## Setting Up to Run the RX Margin Analysis Test

1. From the IBERT Console, be sure the RX Margin Analysis tab is selected, as shown in Figure 8.
2. Select the **GTX\_X0Y18 (GTX0\_117)** transceiver.
3. Click **Add/Remove Parameters**. The Add/Remove Ports/Attributes dialog box opens.
4. In the Add/Remove Ports/Attributes dialog box, shown in Figure 9, select the parameters listed below and place them in the order shown:
  - **TX Diff Swing**
  - **TX Pre-Cursor**
  - **TX Post-Cursor**
5. Click **OK** to return to the IBERT Console window.

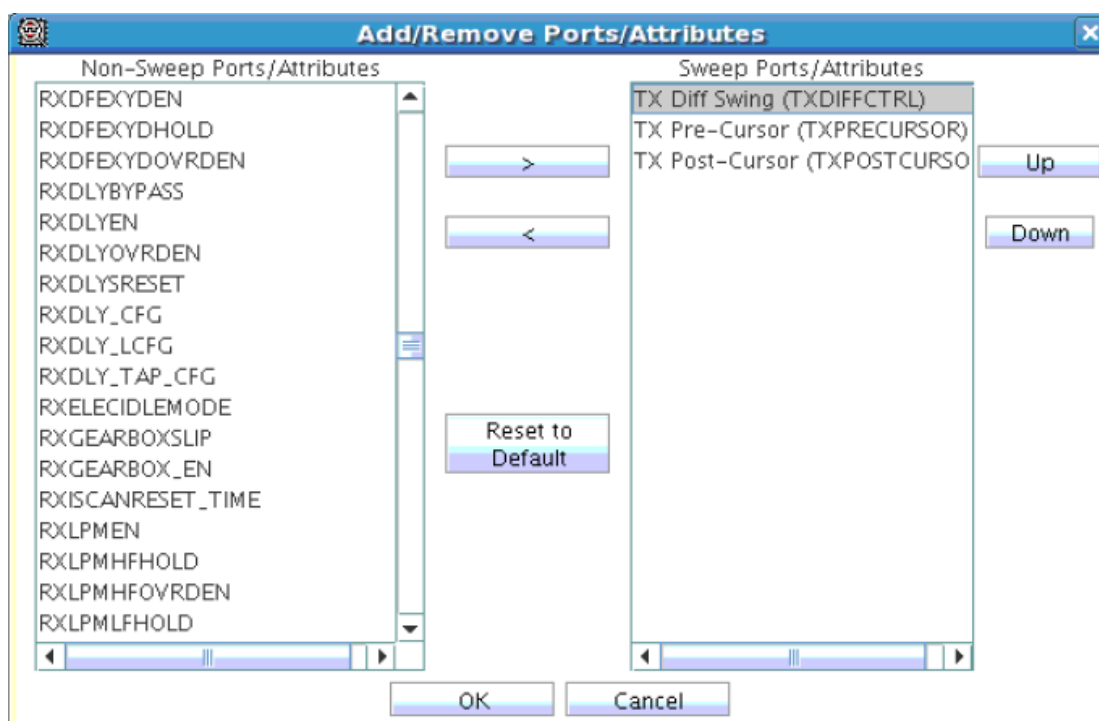


Figure 9: Sweep Settings Options

**Note:** The specified order of the parameters in the **Sweep Ports/Attributes** list dictates how the parameters are swept. The values of the parameters near the top of the list are swept less frequently than those near the bottom. In other words, the parameters near the top are in the outer loops of the sweep algorithm, while those near the bottom are in the inner loops of the sweep algorithm.

6. In the IBERT Console window, with the RX Margin Analysis tab selected, verify the Start and Stop values for each of the sweep parameters:

Parameter	Start Value	Stop Value
TX Diff Swing	<b>350 mV (0010)</b>	<b>400 mV (0011)</b>
TX Pre-Cursor	1.67 dB (00111)	1.67 dB (00111)
TX Post-Cursor	0.68 dB (00011)	0.68 dB (00011)

**Note:** In this tutorial, the only parameter to be swept is TX Diff Swing. Others are set to constant values.

- In the **Scan Settings Area > Scan Algorithm**, select **2D Full Eye**.
- Verify that the **Horizontal Range** is set to -32 (-0.500 UI) to 32 (0.500 UI) with an increment of 8 second dwell time per iteration.  
**Note:** The Sampling Point Region represents the horizontal point within the eye to sample.
- Verify that the **Vertical Range** is set to -96 to 96 with an increment of 8 second dwell time per iteration.
- In the Test Controls area, verify that **Iteration Dwell Time** is set to 1.

## Running the RX Margin Analysis Test and Viewing the Results

Click **Start** to begin sweeping test data. You can view test results in real time or in a log file. With these settings, this may take about ?xx mins.

- To view the test results in real time:

Select the Sweep Test Log tab at the bottom of the IBERT Console to examine and observe sweep test results. For these sweep parameter settings, there are total of 450 iterations (Total Sample Points \* Total Number of Sweep Values = Horizontal Range/8 \* Vertical Range/8 \* TX Diff Swing \* TX Pre-Cursor \* TX Post-Cursor) =  $9 * 25 * 2 * 1 * 1 = 450$ .

- To view the test results log file:

The test results are written to a sweep test results file, which enables you to perform analysis later, offline. Click the **Log File Settings** button under the Test Controls panel to open a dialog box in which you can set both the location and name of the file.

Let the test run through all 130 iterations.

## Plotting the Data with the IBERT Sweep Plot GUI

Next, create a 2D-Eye Scan plot and visually compare the transceiver margin with different settings of the TX Diff Swing parameters using the sweep data results obtained from previous steps.



## About the IBERT Sweep Plot GUI

The IBERT Sweep Plot GUI:

- Lets you plot sweep test results directly inside the console window after the sweep data is available.
- Helps you analyze the sweep data from the transceiver more efficiently, without having to use external spreadsheet software.
- Serves as a standalone mode by launching and reading in single or multiple sweep data files (comma-separated values). Performs data analysis similar to the integrated mode. The standalone mode is helpful when you do not have access to a board and would like to analyze sweep data offline. The integrated mode requires that you connect to a live board locally or remotely.

## Plotting the 2D Eye Scan Data

1. Click the Sweep Test Plot tab at the bottom of the Sweep Test Settings Panel to plot the 2D Eye Scan data.

Two plots display as shown in Figures 10 and 11. Some of the display options you can take advantage of include:

- Plot single or multiple plots.
- Move Left, Right, or BER Markers to examine a margin of each plot.
- Display or hide plots (right-click the plot number to the right of the plot graph).
- Assign or change the line color.

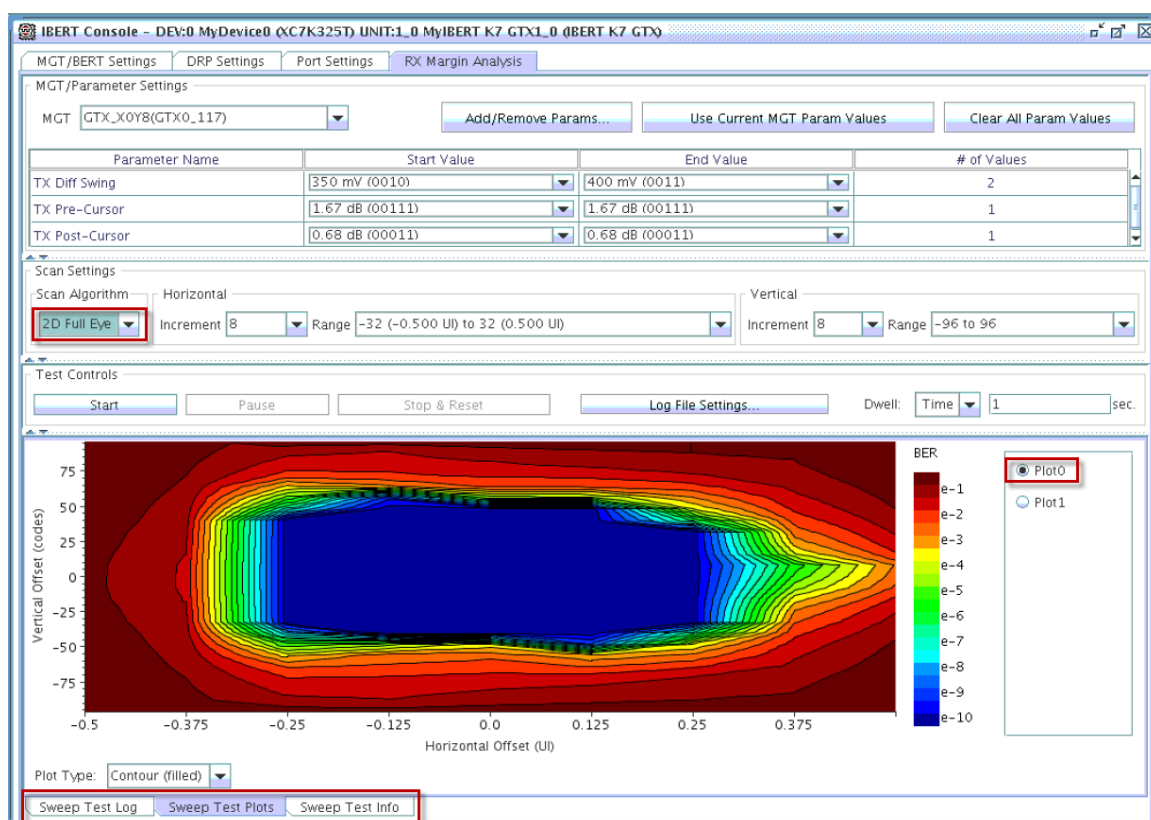


Figure 10: Sweep Test Plots Display (Plot 0)

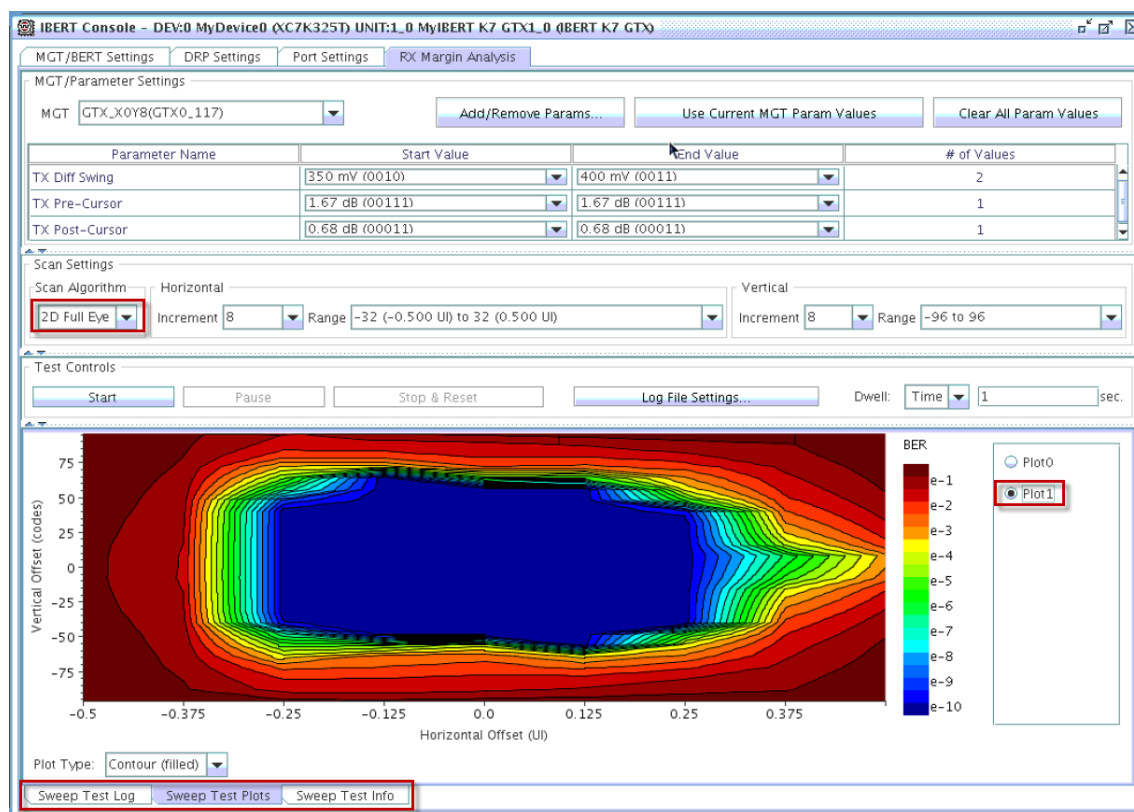


Figure 11: Sweep Test Plots Display (Plot 1)

- Click **the Sweep Test Info** tab, shown in Figure 12: Sweep Test Info Tab Display, and find the widest eye opening and/or highest margin.

You can sort on any of the column headers. In this tutorial, if you look closely, you will find that Plot 1 with the TX Diff Swing set to 400 mV has a bigger eye compared to Plot 0 with 350 mV.

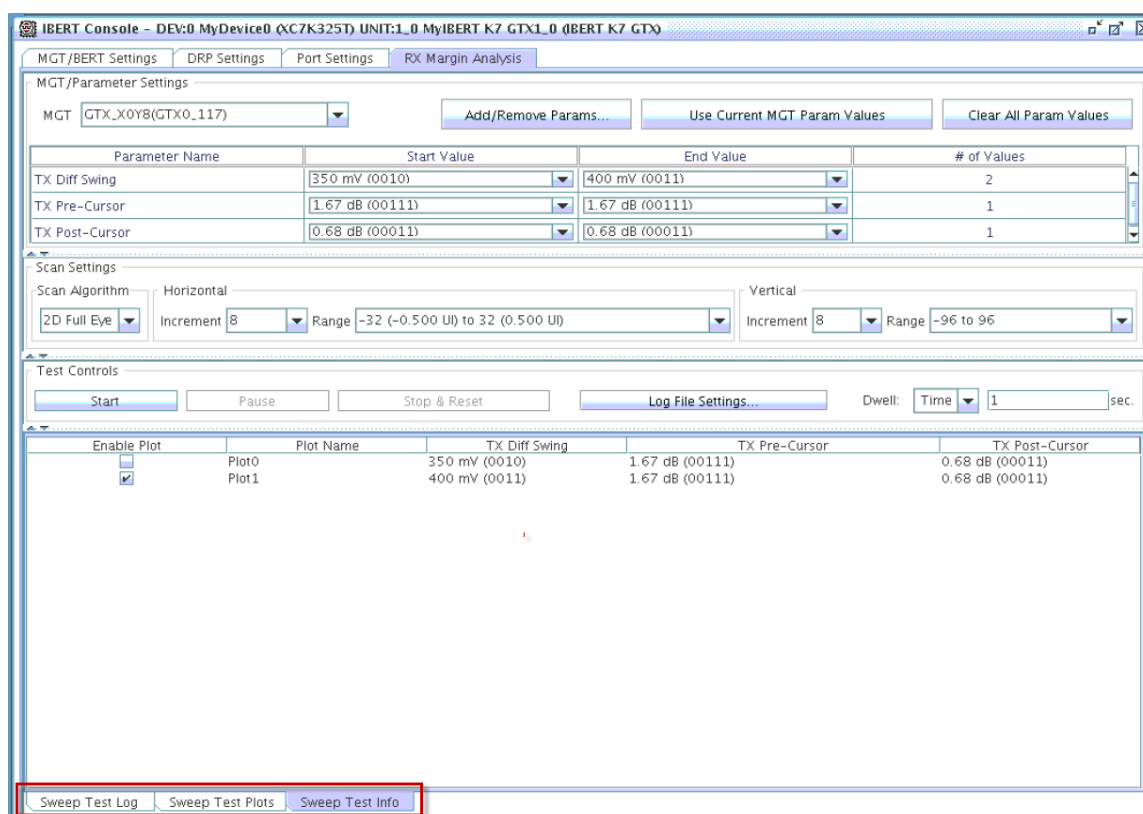


Figure 12: Sweep Test Info Tab Display

For additional information on running sweep tests, see the *ChipScope Pro Software and Cores User Guide, UG029* at <http://www.xilinx.com/tools/cspro.htm>.



## Appendix

# Additional Resources

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## Xilinx Resources

- Xilinx® Documentation: <http://www.xilinx.com/support/documentation>
- Xilinx Glossary: [http://www.xilinx.com/support/documentation/sw\\_manuals/glossary](http://www.xilinx.com/support/documentation/sw_manuals/glossary)
- Xilinx Support: <http://www.xilinx.com/support>

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## ChipScope Documentation

- ChipScope™ Pro Software and Cores User Guide (UG029):  
[http://www.xilinx.com/support/documentation/sw\\_manuals/xilinx14\\_5/chipscope\\_pro\\_sw\\_cores\\_ug029.pdf](http://www.xilinx.com/support/documentation/sw_manuals/xilinx14_5/chipscope_pro_sw_cores_ug029.pdf)
- Using Xilinx ChipScope Pro ILA Core with Project Navigator to Debug FPGA Applications (UG750): [http://www.xilinx.com/support/documentation/sw\\_manuals/xilinx14\\_5/ug750.pdf](http://www.xilinx.com/support/documentation/sw_manuals/xilinx14_5/ug750.pdf)

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## Board Documentation

UG810, "KC705 Evaluation Board for the Kintex-7 FPGA"

[http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ug810\\_KC705\\_Eval\\_Bd.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ug810_KC705_Eval_Bd.pdf)

UG476 "7 Series FPGAs GTX/GTH Transceivers"

[http://www.xilinx.com/support/documentation/user\\_guides/ug476\\_7Series\\_Transceivers.pdf](http://www.xilinx.com/support/documentation/user_guides/ug476_7Series_Transceivers.pdf)

KC705 Schematic

[http://www.xilinx.com/support/documentation/boards\\_and\\_kits/kc705\\_Schematic\\_xtp132\\_rev1\\_1.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/kc705_Schematic_xtp132_rev1_1.pdf)

