

High Bandwidth Memory Demo Script

Introduction

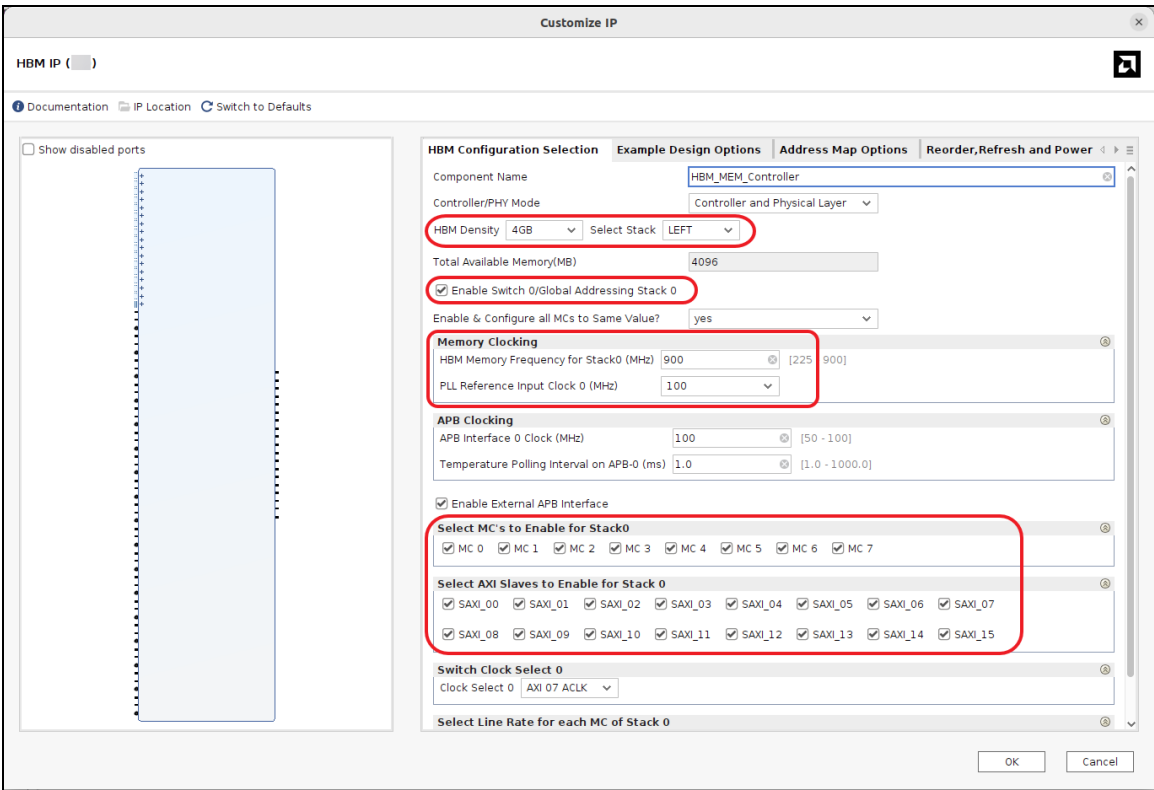
In this demonstration, you will access the high bandwidth memory (HBM) available in the Virtex™ UltraScale+™ device by customizing the AXI High Bandwidth Memory Controller IP core. You will also generate and implement its example design. This type of memory is used when there is a need for high bandwidth in the design.

Preparation:

- Required files: \$TRAINING_PATH/HBM/demo directory
- Required hardware: None
- Supporting materials: "High Bandwidth Memory" module

High Bandwidth Memory

Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> • Launch the Vivado Design Suite. 	
<ul style="list-style-type: none"> • Click the Create Project link in the Quick Start section of the Getting Started page. 	<ul style="list-style-type: none"> • The New Project link in the Getting Started page allows you to create a new Vivado Design Suite project.
<ul style="list-style-type: none"> • Create a new project using the New Project Wizard with the following details: <ul style="list-style-type: none"> • Project name: <i>HBM_demo.xpr</i> • Project location: \$TRAINING_PATH/HBM/demo • Enable Do not specify the sources at this time. 	<ul style="list-style-type: none"> • By default, the Vivado IDE creates the project name as <i>project_1</i>.
<ul style="list-style-type: none"> • Click the Parts tab if it is not selected. • Select Virtex UltraScale+ HBM from the Family drop-down list. • Select the xcvu37p-fsvh2892-2L-e as the part number. • Click Finish to create the project. 	<ul style="list-style-type: none"> • Selecting the Virtex UltraScale+ FPGA board is necessary to enable high bandwidth memory (HBM).
<ul style="list-style-type: none"> • Select IP Catalog under Project Manager in the Flow Navigator. 	<ul style="list-style-type: none"> • Open the IP catalog.

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<ul style="list-style-type: none"> In the IP catalog, expand Memories and Storage Elements > Integrated Memory Interface and double-click HBM IP. 	<ul style="list-style-type: none"> Open the AXI HBM Controller IP for customization.
<ul style="list-style-type: none"> Examine the links under the headline. 	<p>The GUI offers general information:</p> <ul style="list-style-type: none"> Link to documentation IP location on host Switching to default settings
<ul style="list-style-type: none"> Select the HBM Configuration Selection tab in the right frame. Use HBM_MEM_Controller as the component name. 	
<ul style="list-style-type: none"> This tab has a lot of options that can be customized: 	<ul style="list-style-type: none"> Component Name HBM Density Select Stack Clocking Select MC's to Enable for Stack0 Select AXI Slaves to Enable for Stack0 Switch Clock Select 0 Select Line Rate for each MC of Stack0

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<ul style="list-style-type: none"> Select 4GB from the HBM Density drop-down list. The Total Available Memory (MB) field gets updated accordingly, after HBM density is selected. Select LEFT from the Select Stack drop-down list to choose the physical position of the stack of the HBM. 	<ul style="list-style-type: none"> The HBM density option selects the number of stacks to be configured. The HBM memory in the Virtex UltraScale+ (VU37P) device have up to two stacks: one on the right and one on the left. Note that this stack option will not be available if you select 8 GB as the HBM density as both the stacks will be used in this case.
<ul style="list-style-type: none"> Select the Enable Switch 0/Global Addressing Stack 0 option to enable global addressing. 	<ul style="list-style-type: none"> Selecting this option allows the flexibility of global addressing at the cost of latency, but if this is disabled, each AXI port can only access the 2 GB pseudo channel assigned to it.
<ul style="list-style-type: none"> Under the Memory Clocking section, make sure that the HBM Memory Frequency for Stack0 (MHz) field is set to 900 MHz. Set the PLL Reference Input Clock 0 field to 100 MHz. 	<ul style="list-style-type: none"> These options specify the data rate at which HBM stack 0 memory is desired to operate and the PLL reference clock frequency used to generate HBM stack 0 memory clock respectively. You can change this as per requirements. Similar settings can be done for stack 1 if the HBM density is chosen as 8 GB.
<ul style="list-style-type: none"> Select all the memory channel controllers, if they are not selected already, in the Select MCs to Enable for Stack 0 section. Similarly, select all the AXI slaves under Select AXI slaves to Enable for Stack 0 section. 	<ul style="list-style-type: none"> The memory controller section lists all of the memory channel controllers in each stack, and each can be individually enabled or disabled for power savings.
<ul style="list-style-type: none"> Keep the default settings for the Switch Clock Select 0 and Select Line Rate for Each MC of Stack 0 sections. 	<ul style="list-style-type: none"> The IP automatically defaults to a clock that is roughly in the middle of the enabled memory channels. However, this can be changed as per requirements. For each memory channel, there are two AXI ports available. Based on the selection of the memory channel, the corresponding AXI ports are enabled and are selected for use in the switch clock. The second option selects the memory channel operating frequency. div4 is full speed and div8 is half speed.

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<ul style="list-style-type: none"> Select the Example Design Options tab and review the default settings. 	<ul style="list-style-type: none"> This tab specifies the AXI clock frequency to be used for all enabled AXI interfaces in the example design. The MMCM primitive is instantiated per stack in the example design to generate the AXI clock. The AXI Clock Frequency (MHz) setting specifies the MMCM output clock frequency whereas the AXI Input Clock Frequency (MHz) setting specifies the MMCM input clock frequency.
<ul style="list-style-type: none"> Select the Address Map Options tab and review the default settings. 	<ul style="list-style-type: none"> By selecting the Custom Address Map option, you can define the mapping from the AXI addresses to HBM memory addresses; otherwise it takes the default settings.
<ul style="list-style-type: none"> Select the Reorder, Refresh, and Power Savings Options tab and review the default settings. 	<p>This tab has the reorder, refresh, and power-saving options.</p> <ul style="list-style-type: none"> These options are only available if you are not using a custom address map.
<ul style="list-style-type: none"> Select the Reliability Options tab and review the default settings. 	<ul style="list-style-type: none"> This tab handles all the ECC and parity-related options.
<ul style="list-style-type: none"> Click OK to generate the IP. 	
<ul style="list-style-type: none"> In the Generate Output Products dialog box, select Out of Context per IP and then click Generate. Click OK once the output products are generated. 	<ul style="list-style-type: none"> Generate the core files. Synthesis of the core will be performed. What is the purpose of each of these output files?
<ul style="list-style-type: none"> Review the Hierarchy and IP Sources tabs. 	<ul style="list-style-type: none"> By default, the following IP products are generated: <ul style="list-style-type: none"> Instantiation template Synthesis Simulation DCP Stub
<ul style="list-style-type: none"> In the Sources window, under Design Sources, right-click HBM_MEM_Controller and select Open IP Example Design. 	<ul style="list-style-type: none"> This creates the IP example design that will be stored in a different directory. The original design will be untouched.

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<ul style="list-style-type: none">In the Open Example Design dialog box, browse to the <code>\$TRAINING_PATH/HBM/demo</code> directory to store the example design.Click OK.	<ul style="list-style-type: none">A new Vivado Design Suite session opens with the IP example design.
<ul style="list-style-type: none">Observe the design hierarchy.Review the other tabs as well.Close the Vivado project once done.	<ul style="list-style-type: none">The generated example design includes all files for synthesis, simulation, and implementation.Note that <i>example_top_syn</i> is the top-level name for the new project.

Summary

In this demo, you walked through the customization of the AXI High Bandwidth Memory Controller core and accessed the HBM memory. This core provides configurable access to the HBM stack with up to 16 AXI3 slave ports, each with its own independent clocking. You also generated an example design.