

# Report Clock Networks Demo Script

## Introduction

This demonstration script provides high-level instructions on the Clock Networks Report available in the AMD Vivado™ Design Suite.

### Preparation:

- Required files: \$TRAINING\_PATH/Report\_Clock\_Network/demo/KCU105/verilog
- Required hardware: None

## Report Clock Networks

Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> <li>• Launch the Vivado Design Suite.</li> <li>• Unzip the project using the Tcl Console:  <pre>exec unzip \$::env(TRAINING_PATH)/ Report_Clock_Network/demo/ KCU105/verilog.zip -d \$::env(TRAINING_PATH)/ Report_Clock_Network/demo/ KCU105/verilog</pre> </li> </ul>	
<ul style="list-style-type: none"> <li>• Open the <b>wave_gen.xpr</b> project located from the following directory:  <pre>\$TRAINING_PATH/Report_Clock_Network/demo/KCU105/verilog</pre> </li> </ul>	<p>A synthesized design is provided for this demo.</p> <p>The synthesized design allows the user to analyze the design with various reports.</p> <p>The open synthesized design allows the user to enter or edit any timing constraints to be applied to the design. The generated reports enable the user to examine clock interaction and clock structure.</p>
<ul style="list-style-type: none"> <li>• Open the synthesized design.</li> </ul>	<p>Report Clock Networks can be accessed only when the Synthesized or Implemented design is open.</p>

Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> <li>Open the schematic of the <b>clk_gen_i0</b> cell from the Netlist window.</li> <li>Expand <b>clk_gen_i0 &gt; clk_core_i0 &gt; inst.</b></li> </ul>	<p>The schematic view of a module allows the user to analyze the propagation of a clock through all the instances from source to load.</p> <p>The loads or the endpoints displayed in the report are sorted by type.</p> <p>You can cross probe the nets and pins of the module and review the clock structure.</p>
<ul style="list-style-type: none"> <li>Click <b>Report Clock Networks</b> under Synthesized Design from the Flow Navigator.</li> </ul> 	<p>The Clock Networks report enables the user to get the clear structure of clocks from source to load in the design, including user-generated clocks.</p> <p>The Clock Networks report displays a hierarchical tree view of clock network topology.</p> <p>Alternatively, you can use the following Tcl command to obtain the Clock Networks report.</p> <pre>report_clock_networks -name {network_1}</pre>
<ul style="list-style-type: none"> <li>Leave the result name as default <i>network_1</i>.</li> <li>Check the newly opened Clock Networks tab at the bottom.</li> </ul>	<p>Reports the network fanout of each clock net in the open synthesized design.</p>

Action with Description	Point of Emphasis and Key Takeaway
	
<ul style="list-style-type: none"> <li>View the complete hierarchy of the clock network.</li> </ul>	<p>Observe the fanout of all the clock objects.</p> <p>clk_pin_p is the primary clock that drives the number of loads and is not constrained. Hence it falls under the Unconstrained section of the report.</p> <p>The clk_pin_p is propagated to the mmcm3_adv_inst module which in turn generates the clocks CLKFBOUT, CLKOUT0, and CLKOUT1 automatically.</p>
<ul style="list-style-type: none"> <li>Expand mmcm3_adv_inst &gt; CLKFBOUT.</li> </ul>	<p>The CLKFBOUT drives the buffer clkf_buf (BUFGCE) which is a BUFG for clock feedback.</p>
<ul style="list-style-type: none"> <li>Expand mmcm3_adv_inst &gt; CLKOUT0.</li> </ul>	<p>CLKOUT0 drives the buffer clkout1_buf, which then drives various loads like FDPE, FDRE, and RAMB18E2.</p> <p>From the schematic view, observe that the buffer clkout1_buf connects to the clk_rx pin of clk_gen_i0 cell.</p> <p>The number of loads driven by the clock can also be viewed from the report.</p>

Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> <li>Expand <code>mmcme3_adv_inst</code> &gt; <code>CLK_OUT1</code>.</li> </ul>	<p>CLKOUT1 is the clock generated automatically by MMCM.</p> <p><code>clk_samp</code> is a generated clock using clock buffer (BUFGCE). You need to define this generated clock by using the <code>create_generated_clock</code> command.</p> <p>The timing engine in the Vivado Design Suite does not automatically derive the timing for such manually gated clocks and it needs to be specified, unlike MMCM output clocks.</p>
<ul style="list-style-type: none"> <li>Close the Clock Networks report and the synthesized design.</li> <li>Close the Vivado Design Suite.</li> </ul>	

## Summary

In this demo you learned how to use the Clock Networks report to generate a clock tree structure of all available clocks in the design.

References:

- Supporting materials
  - Vivado Design Suite User Guide: Design Analysis and Closure Techniques* (UG906)