

# Timing Summary Report Demo Script

## Introduction

This demonstration script provides high-level instructions on the key features of the Timing Summary report generated by the AMD Vivado™ Design Suite.

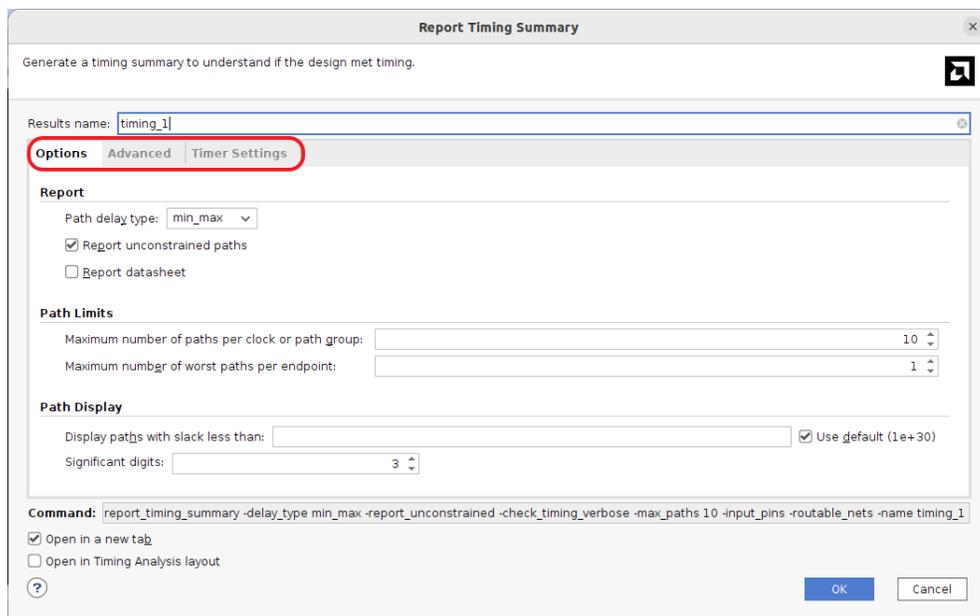
### Preparation:

- Required files: \$TRAINING\_PATH/Timing\_Summary\_Report/demo/KCU105/netlist
- Required hardware: None

## Timing Summary Report

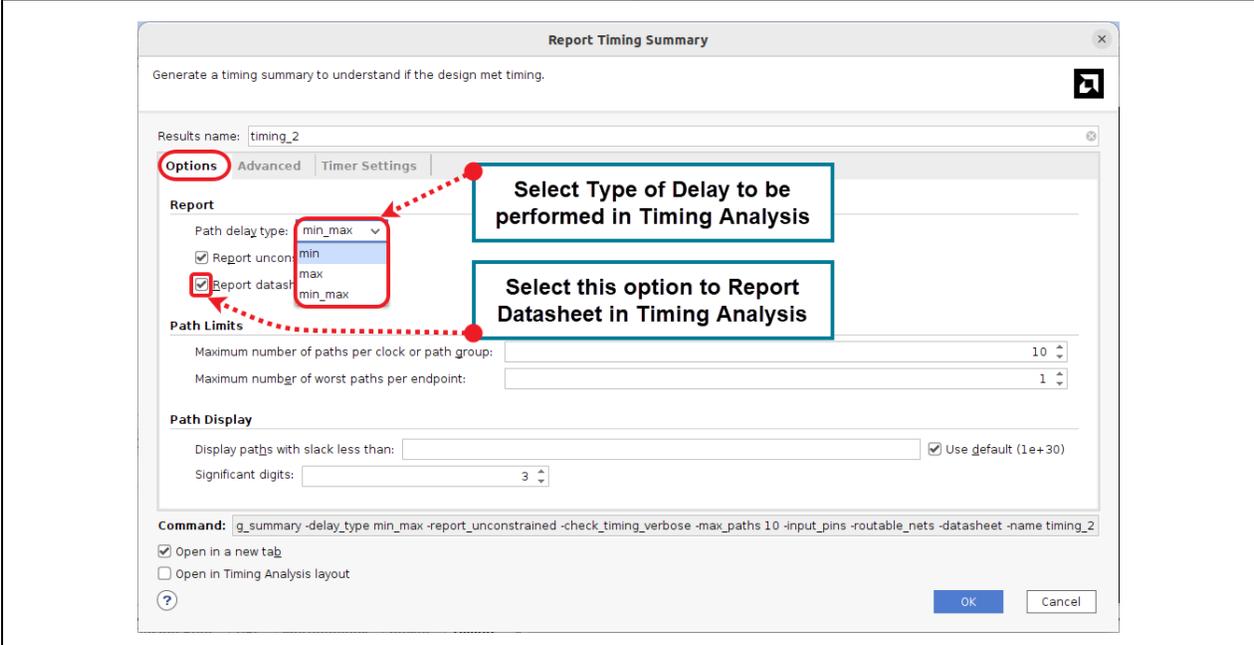
Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> <li>• Launch the Vivado Design Suite.</li> <li>• Unzip the project using the Tcl Console:  <pre>exec unzip \$::env(TRAINING_PATH)/Timing_Summary_Report/demo/KCU105/netlist.zip -d \$::env(TRAINING_PATH)/Timing_Summary_Report/demo/KCU105/netlist</pre> </li> </ul>	
<ul style="list-style-type: none"> <li>• Open the <b>wave_gen.xpr</b> project located from the following directory:  <pre>\$TRAINING_PATH/Timing_Summary_Report/demo/KCU105/netlist</pre> </li> </ul>	<ul style="list-style-type: none"> <li>• An implemented design is provided for this demo.</li> </ul>
<ul style="list-style-type: none"> <li>• Open the implemented design.</li> <li>• Ignore any critical warnings and click <b>OK</b>.</li> </ul>	<ul style="list-style-type: none"> <li>• The Timing Summary report was generated with the default options when the implementation was run.</li> <li>• When you open the implemented design, a saved Timing Summary report automatically opens up at the bottom.</li> <li>• This report has already been saved and cannot be rerun.</li> <li>• The Timing Summary report includes hyperlinks and enables the user to cross-probe the timing report to the Device and Schematic viewers.</li> </ul>

Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> <li>Click <b>Report Timing Summary</b> under Implemented Design from the Flow Navigator.</li> </ul>	<ul style="list-style-type: none"> <li>The Report Timing Summary dialog box allows customization of the report to be generated.</li> </ul> <p>The dialog box has three tabs:</p> <ul style="list-style-type: none"> <li><b>Options</b></li> <li><b>Advanced</b></li> <li><b>Timer Settings</b></li> </ul> <p><b>Note:</b> If the Results name field is left empty, the Timing Summary report will be displayed in the Tcl Console, not the Results window.</p>

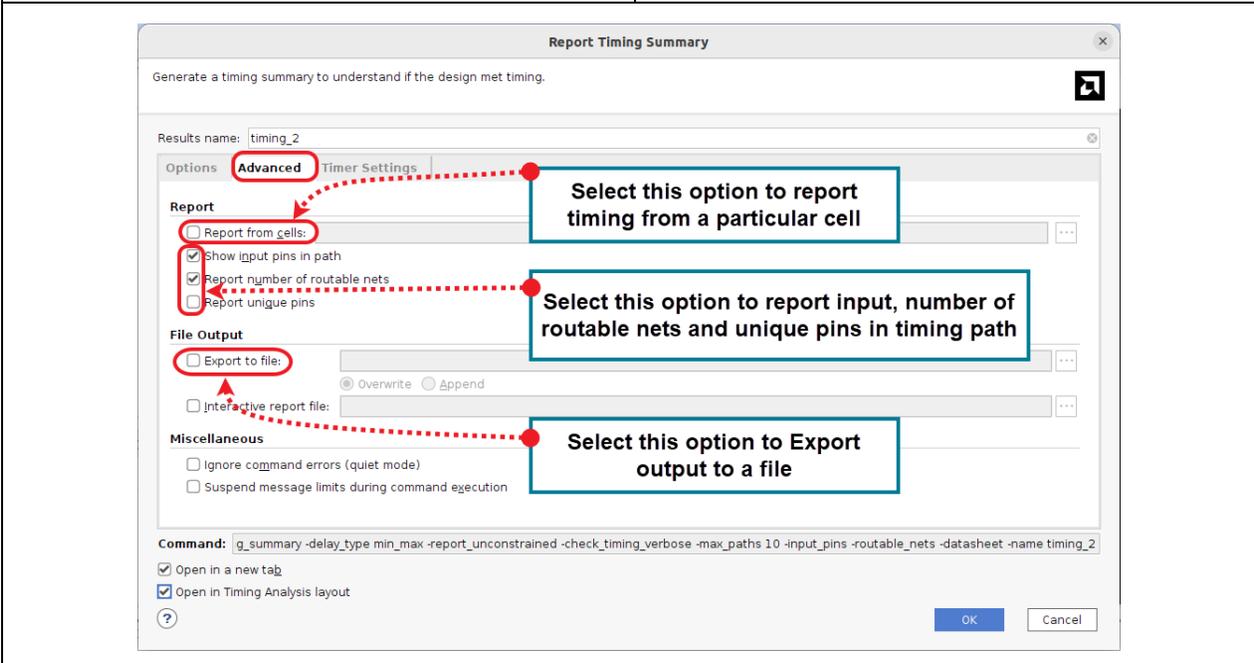


Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> <li>Select the <b>Options</b> tab and introduce the settings available.</li> </ul>	<ul style="list-style-type: none"> <li>The Options tab has three sections:                             <ul style="list-style-type: none"> <li><b>Report</b></li> <li><b>Path Limits</b></li> <li><b>Path Display</b></li> </ul> </li> <li>The Report section has settings to enable the inclusion of unconstrained paths and data sheet information.</li> <li>The <b>Path delay type</b> is very important. It has three valid values, <b>min</b> (complete a hold check on reported paths only), <b>max</b> (complete a setup check on reported paths only), and <b>min_max</b> (complete both a setup and hold check).</li> <li>By default, unconstrained paths are reported unless the check box is de-selected. The data sheet section in the Timing Summary report displays <b>worst case setup</b> and <b>hold</b> requirements for input and output ports and I/O data buses.</li> <li>The Path Limits section controls how many paths and worst paths per endpoint are included in your report. By default, the worst 10 delay paths per clock or path group are reported (not all paths are reported). Likewise, not all paths per endpoint are shown (only the single longest path).</li> <li>The Tcl command to regenerate this report is shown in the Command field.</li> </ul>

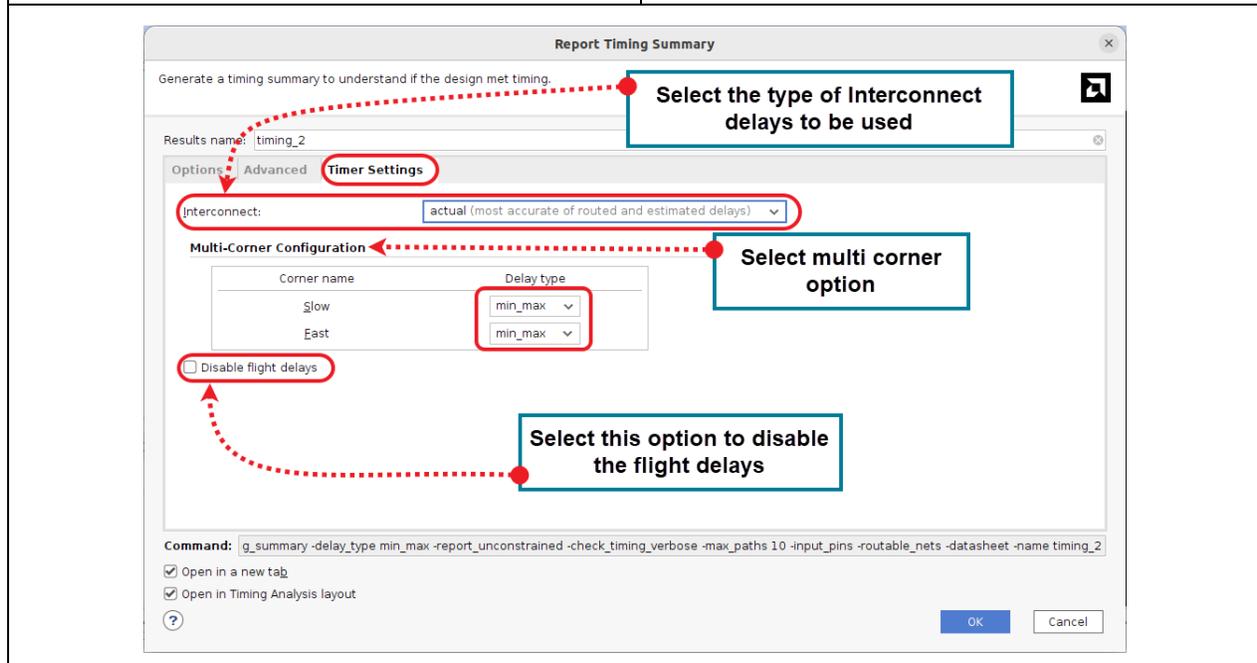
Action with Description	Point of Emphasis and Key Takeaway
-------------------------	------------------------------------



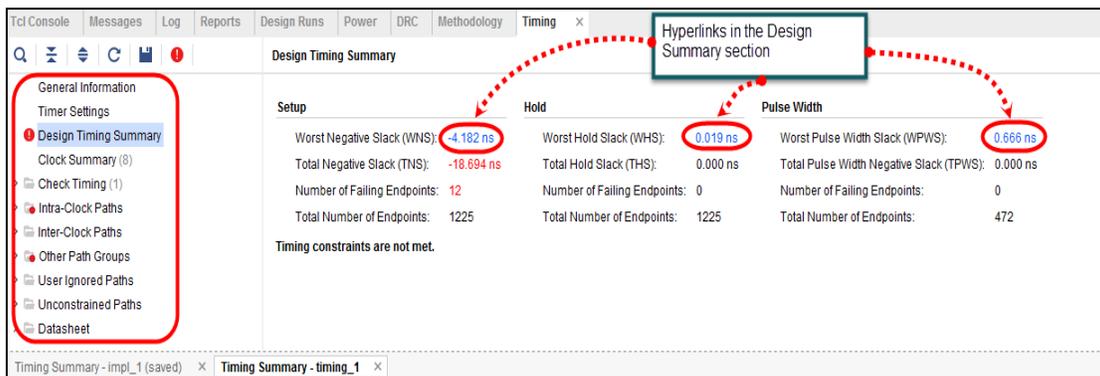
- Select the **Advanced** tab and introduce the settings available.
- The Advanced tab has less often used options such as displaying the input pins of cells in the timing path and allowing designers to write the Timing Summary report to a text file.



Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> <li>Select the <b>Timer Settings</b> tab and introduce the settings available.</li> </ul>	<ul style="list-style-type: none"> <li>The Timer Settings tab enables the user to perform what-if timing analysis via customizing how the Vivado timing engine performs.</li> <li>The Interconnect option allows the user to select <b>estimated</b> (synthesis), <b>actual</b> (post-implementation), or <b>none</b> (zero delay only) interconnect delays in timing analysis. The multi-corner configuration settings enable the user to use fast or slow corner timing information in the report.</li> </ul>
<ul style="list-style-type: none"> <li>Introduce the valid values available for slow and fast corners.</li> <li>The values selected for multi-corner (i.e., both fast and slow) specify the type of delays to be used during timing analysis.</li> </ul>	<ul style="list-style-type: none"> <li>The <b>Fast</b> timing corner corresponds to the fastest process, highest voltage, and lowest temperature. The <b>Slow</b> timing corner corresponds to the slowest process, lowest voltage, and highest temperature.</li> <li>By default, both setup (max) and hold (min) checks are performed for both fast and slow timing corners.</li> <li>If you select the <b>None</b> value for any timing corner, the timing analysis for that timing corner is disabled.</li> </ul>



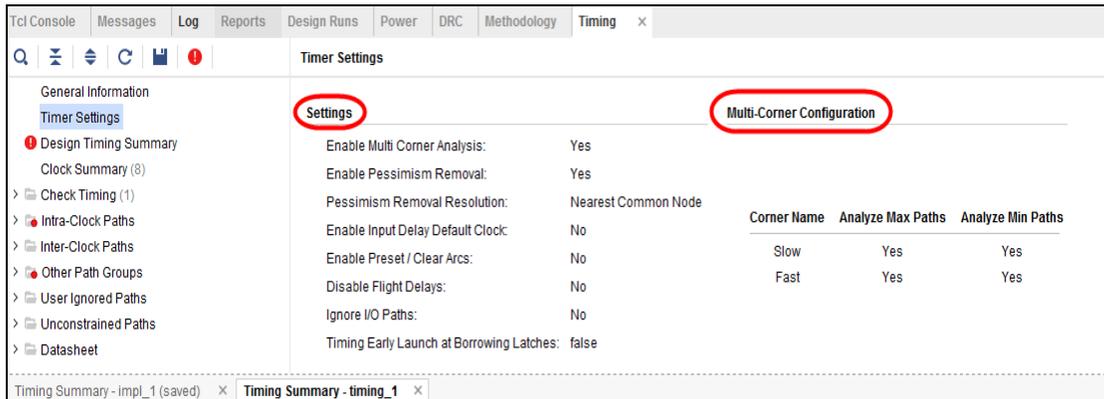
Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> <li>Verify the equivalent Tcl command being used.</li> <li>Click <b>OK</b> in the Report Timing Summary dialog box.</li> </ul>	<ul style="list-style-type: none"> <li>The Timing Summary report opens at the bottom of the GUI in the Results window.</li> <li>The Design Timing Summary section provides a brief summary of whether the design meets your timing objectives. It has three areas: <b>Setup</b>, <b>Hold</b>, and <b>Pulse Width</b>.</li> </ul>
<ul style="list-style-type: none"> <li>Introduce each area of the Design Timing Summary section.</li> </ul>	<ul style="list-style-type: none"> <li>The Setup area reports all checks related to max delay analysis (i.e., setup, recovery, and data checks).</li> <li>The Hold and Pulse Width area reports all checks related to min delay analysis and pulse switching limits.</li> </ul> <p><b>Note:</b> We recommend that designers verify that all timing constraints are met after implementation.</p>



**Note:** The timing numbers may vary depending on the version of the Vivado Design Suite and the OS.

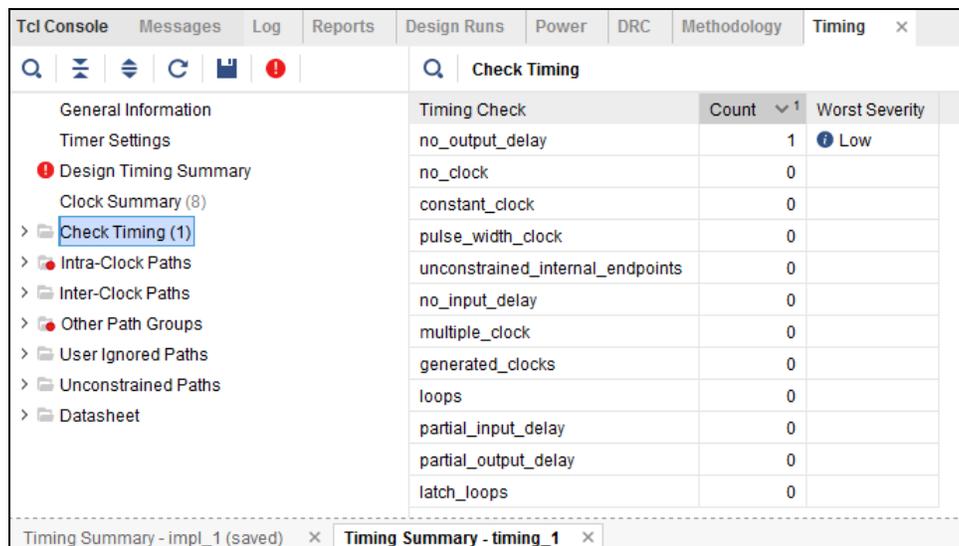
<ul style="list-style-type: none"> <li>Select the <b>Timer Settings</b> section of the Timing Summary report.</li> </ul>	<ul style="list-style-type: none"> <li>The Timing Settings section contains a list of the Vivado timing engine settings used to generate the timing report.</li> <li>Specifically, it displays the options selected to enable or disable multi-corner analysis, pessimism removal, etc.</li> </ul>
--	--

<b>Action with Description</b>	<b>Point of Emphasis and Key Takeaway</b>
--------------------------------	---

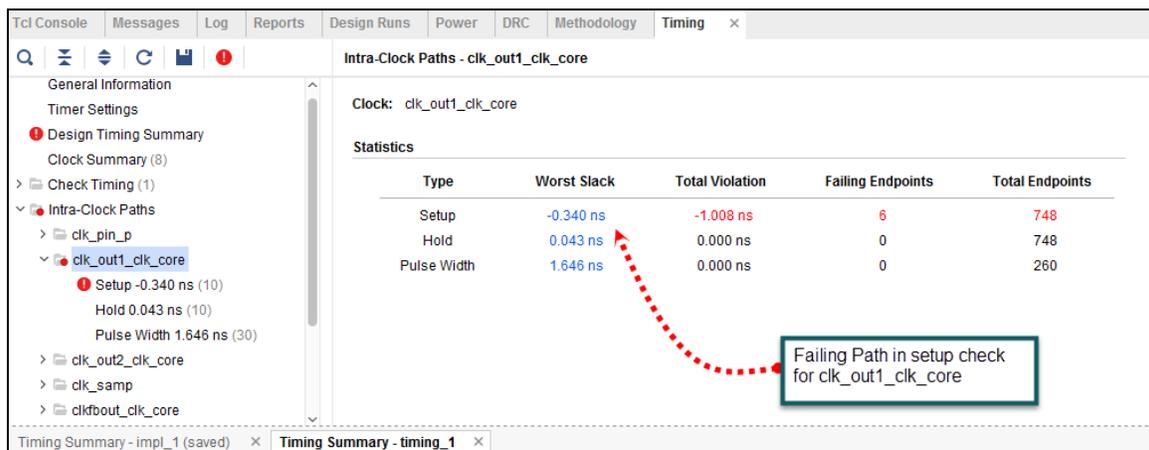


**Note:** The timing numbers may vary depending on the version of the Vivado Design Suite and the OS.

- |  |   |
|--|---|
| <ul style="list-style-type: none"> <li>• Select the <b>Check Timing</b> section of the Timing Summary report.</li> </ul> | <ul style="list-style-type: none"> <li>• The Check Timing report contains information about missing timing constraints or paths with incorrect constraints that should be reviewed.</li> <li>• This report displays ports with missing input and output delay constraints, objects with missing clock definitions, unconstrained internal end points, etc.</li> <li>• Are there any missing timing constraints in this design?</li> </ul> |
|--|---|

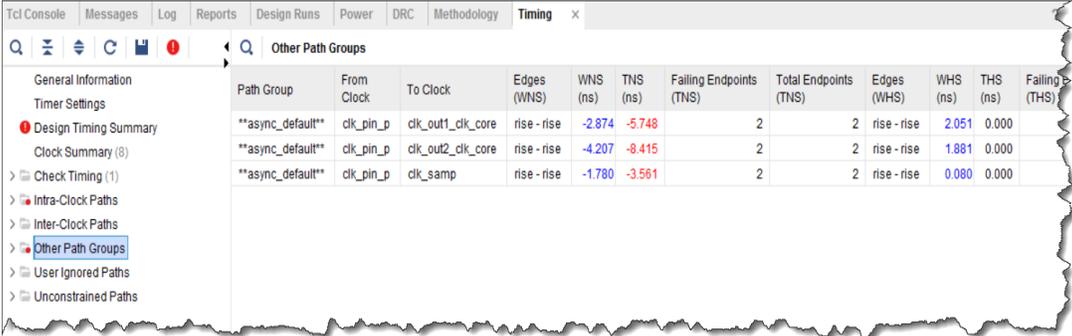


Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> <li>Select the <b>Intra-Clock Paths</b> section of the Timing Summary report.</li> </ul>	<ul style="list-style-type: none"> <li>This portion of the Timing Summary report displays timing paths with the same source and destination clock.</li> <li>Timing paths are automatically sorted by clock and worst slack values are listed.</li> <li>Which clock has some failing intra-clock paths?</li> <li>How many failing endpoints are reported? What do each of the failing paths have in common?</li> <li>Verify that you can successfully increase the number of failing endpoints that are reported by making a new timing report (increase to 20).</li> <li>What has changed about the paths shown?</li> <li>Verify that you can increase the number of worst paths per endpoint (increase to 10) by making a new report.</li> <li>How can you verify that this is working properly?</li> </ul>



**Note:** The timing numbers may vary depending on the version of the Vivado Design Suite and the OS.

Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> <li>• Select <b>Intra-Clock Paths &gt; clk_out1_clk_core &gt; Setup.</b></li> <li>• Right-click a path and explore the following options:                             <ul style="list-style-type: none"> <li>• Device viewer highlights the path (cross-probing)</li> <li>• Report timing on source to destination</li> <li>• Schematic generation</li> <li>• Path-specific constraint options</li> <li>• Floorplanning options</li> </ul> </li> </ul>	<ul style="list-style-type: none"> <li>• When you right-click any timing path, the Vivado IDE provides many options, such as schematic generation, defining a multicycle path timing constraint, false path, etc.</li> </ul>
<ul style="list-style-type: none"> <li>• Double-click a path to open the <b>Path Report</b> tab in the main workspace area.</li> </ul>	<ul style="list-style-type: none"> <li>• The Path Report provides detailed timing path information, including source and destination elements. It also describes the timing path with the logic element names and net delay values.</li> <li>• Introduce each section of the Path Properties: <b>Summary, Source Clock Path, Data Path, and Destination Clock Path.</b></li> <li>• Review the Requirement, Logic Levels, and other Summary contents.</li> </ul>
<ul style="list-style-type: none"> <li>• Select the <b>Inter-Clock Paths</b> section of the Timing Summary report.</li> </ul>	<ul style="list-style-type: none"> <li>• This portion of the Timing Summary report displays paths with different source and destination clocks.</li> </ul>
<ul style="list-style-type: none"> <li>• Select the <b>Other Path Groups</b> section of the Timing Summary report.</li> </ul>	<ul style="list-style-type: none"> <li>• The Other Path Groups section displays default groups and user-defined path groups.</li> </ul> <p><b>Note:</b> The <i>*async_default*</i> group is automatically created by the Vivado timing engine and includes all the paths ending with asynchronous timing checks.</p> <ul style="list-style-type: none"> <li>• What kind of paths are reported in the <i>*async_default*</i> group?</li> <li>• What do the path endpoints have in common (generate a schematic)?</li> <li>• Is this path constrained?</li> </ul>

Action with Description	Point of Emphasis and Key Takeaway
 <p><b>Note:</b> The timing numbers may vary depending on the version of the Vivado Design Suite and the OS.</p>	
<ul style="list-style-type: none"> <li>Select the <b>User Ignored Paths</b> section of the Timing Summary report.</li> </ul>	<ul style="list-style-type: none"> <li>This section displays the timing paths ignored during timing analysis due to timing exceptions constraints such as <code>set_clock_groups</code> and <code>set_false_path</code>, etc.</li> <li>How do you verify that the path is NOT constrained?</li> <li>What constraint was applied to these paths?</li> </ul>
<ul style="list-style-type: none"> <li>Select the <b>Unconstrained Paths</b> section of the Timing Summary report.</li> </ul>	<ul style="list-style-type: none"> <li>This section displays timing paths that are not timed since there is no constraint applied to these paths.</li> <li>How can you tell that there is no constraint applied to these paths?</li> </ul>
<ul style="list-style-type: none"> <li>Close the Timing Summary report and the Vivado Design Suite.</li> </ul>	

## Summary

Here you learned how to use the Timing Summary report to generate custom timing reports to meet a design's timing sign-off requirements. You also learned about various options available for building efficient timing reports.

References:

- Supporting materials
  - Vivado Design Suite User Guide: Design Analysis and Closure Techniques (UG906)*