

# Report Clock Interaction Demo Script

## Introduction

This demonstration script provides high-level instructions on the proper use of the Report Clock Interaction option available in the Vivado™ Design Suite.

### Preparation:

- Necessary files are located in the following directory:  
`$TRAINING_PATH/ClockInteraction/demo/KCU105/verilog`
- Required hardware: None

## Report Clock Interaction

Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> <li>Launch the Vivado Design Suite.</li> <li>Unzip the project using the Tcl Console:  <pre>exec unzip \$::env(TRAINING_PATH)/ClockInteraction/demo/KCU105/verilog.zip -d \$::env(TRAINING_PATH)/ClockInteraction/demo/KCU105/verilog</pre> </li> </ul>	
<ul style="list-style-type: none"> <li>Open the <b>wave_gen.xpr</b> project located in the following directory:  <code>\$TRAINING_PATH/ClockInteraction/demo/KCU105/verilog</code></li> </ul>	<ul style="list-style-type: none"> <li>The implemented design is provided for this demo.</li> </ul>
<ul style="list-style-type: none"> <li>Open the implemented design.</li> <li>Click <b>OK</b> in the dialog box if any warnings appear.</li> </ul>	<ul style="list-style-type: none"> <li>The implemented design enables you to analyze the design with various reports.</li> <li>The Clock Interaction Report can be accessed only when a synthesized or implemented design is open.</li> </ul>

Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> <li>• Generate the Clock Interaction Report with default settings from the menu <b>Reports &gt; Timing &gt; Report Clock Interaction</b> or from the Project Navigator under implemented design.               <ul style="list-style-type: none"> <li>• Alternatively, you can use the Tcl command  <code>report_clock_interaction -name timing_1</code> to generate the Clock Interaction Report.</li> </ul> </li> <li>• Review the options in Report Clock Interaction dialog box.</li> </ul>	<ul style="list-style-type: none"> <li>• The Clock Interaction Report analyzes the timing paths that cross from one clock domain to another.</li> <li>• The report displays the analysis in a nice graphical view.</li> <li>• This report is helpful to determine if the design needs any synchronization circuits and allows you to add timing exception constraints to cover paths between clock domains.</li> <li>• Use the Delay Type field in the dialog box to set the type of analysis to be run.</li> <li>• For implemented designs, both min delay and max delay analysis (setup/hold, recover/removal) are performed by default.</li> <li>• To run min delay analysis only (hold and removal), select delay type min.</li> </ul>

Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> <li>Review the generated Clock Interaction Report.</li> </ul>	<ul style="list-style-type: none"> <li>The report displays as a matrix of clock domains with the source clocks in the vertical axis and the destination clocks in horizontal axis.</li> <li>The tiles of the matrix are color coded.</li> <li>No Path - Black: There are no timing paths that cross from the source clock to the destination clock. In this case, there is no clock interaction and nothing to report.</li> <li>Timed - Green: The source clock and destination clock have a synchronous relationship and are safely timed together. This state is determined by the timing engine when the two clocks have a common primary clock and a simple period ratio.</li> <li>User Ignored Paths - Dark Blue: User-defined <code>false_path</code> or clock group constraints cover all paths crossing from the source clock to the destination clock.</li> <li>Partial False Path - Light Blue: User-defined <code>false_path</code> constraints cover some of the timing paths crossing from the source clock to the destination clock where the source clock and destination clock have a synchronous relationship.</li> <li>Timed (Unsafe) - Red: The source clock and destination clock have an asynchronous relationship. In this case, there is no common primary clock or no expandable period.</li> <li>Partial False Path (Unsafe) - Orange: This category is identical to Timed (Unsafe), except that at least one path from the source clock to the destination clock is ignored due to a false path exception.</li> <li>Max Delay Datapath Only - Gray: A <code>set_max_delay -datapath_only</code> constraint covers all paths crossing from the source clock to the destination clock clocks in the horizontal axis.</li> </ul>

Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> <li>Review the details provided in the Clock Pairs table.</li> </ul>	<ul style="list-style-type: none"> <li>The table provides a comprehensive overview of the timing slack for setup/recovery and/or for hold/removal for source/destination clock pair.</li> <li>It also shows useful information about the path requirement of the worst paths, common primary clock, and constraints status.</li> </ul>
<ul style="list-style-type: none"> <li>Review each column in the table.</li> </ul>	<ul style="list-style-type: none"> <li>ID: A numeric ID for the source/destination clock pair being displayed.</li> <li>Source Clock: The clock domain from which the path originates.</li> <li>Destination Clock: The clock domain within which the path terminates.</li> <li>Edges (WNS): The clock edges used to calculate the worst negative slack for max delay analysis (setup/recovery).</li> <li>WNS (Worst Negative Slack): The worst slack calculated for various paths crossing the specified clock domains. A negative slack indicates a problem in which the path violates a required setup (or recovery) time.</li> <li>TNS (Total Negative Slack): The sum of the worst slack violation for all the endpoints that belong to paths crossing the specified clock domains.</li> <li>Failing Endpoints (TNS): The number of endpoints in the crossing paths that fail to meet timing. The sum of the violations corresponds to TNS.</li> <li>Total Endpoints (TNS): The total number of endpoints in the crossing paths.</li> <li>Path Requirements (WNS): The timing path requirement corresponding to the path reported in the WNS column. There can be several path requirements between any clock pairs if both rising and falling edges are active for at least one of the two clocks, or some timing exceptions have been applied on paths between the two clocks. The value reported in this column is not always the most challenging requirement.</li> </ul>

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<ul style="list-style-type: none"> <li>Review the Clock Pair Classification and Inter-Clock Constraints columns.</li> </ul>	<ul style="list-style-type: none"> <li><b>Clock Pair Classification:</b> Provides information about the common node and common period between the clock pair. If either the source clock or the destination clock of the timing paths is, with respect to a virtual clock, Virtual is displayed in the Clock Pair Classification field.</li> <li><b>Inter-Clock Constraints:</b> Shows the constraints summary for all paths between the source clock and destination clock.</li> </ul>
<ul style="list-style-type: none"> <li>Close the Clock Interaction Report and the implemented design.</li> </ul>	
<ul style="list-style-type: none"> <li>Close the Vivado Design Suite.</li> </ul>	

## Summary

Here you learned how to use the Report Clock Interaction option before making timing constraints in the design.

References:

- Supporting materials
  - Vivado Design Suite User Guide: Design Analysis and Closure Techniques (UG906)*