

Report Datasheet Demo Script

Introduction

This demonstration script provides high-level instructions on the proper use of the Report Datasheet function when making I/O timing constraints in the Vivado™ Design Suite.

Preparation:

- Necessary files are located in the following directory:
`$TRAINING_PATH/Report_Datasheet/demo/KCU105`
- Required hardware: None

Report Datasheet

Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> Launch the Vivado Design Suite. Unzip the project using the Tcl Console: <pre>exec unzip \$::env(TRAINING_PATH)/Report_Da tasheet/demo/KCU105/netlist.zip -d \$::env(TRAINING_PATH)/Report_Da tasheet/demo/KCU105/netlist</pre> 	
<ul style="list-style-type: none"> Open the DDR_design.xpr project located in the following directory: <code>\$TRAINING_PATH/Report_Datasheet/demo/KCU105</code> 	<ul style="list-style-type: none"> The implemented design is provided for this demo.
<ul style="list-style-type: none"> Open the implemented design. Click OK in the dialog box if any warnings appear. 	<ul style="list-style-type: none"> The implemented design enables you to analyze the design with various reports. The Report Datasheet function can be accessed only when the synthesized or implemented design is open.

Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> Generate the datasheet report from the Reports > Timing > Report Datasheet menu in the Vivado Design Suite. <ul style="list-style-type: none"> Alternatively, you can also use the Tcl command <code>report_datasheet -name timing_1</code> to generate the datasheet report. Leave the result name as the default, <i>timing_1</i>. 	<ul style="list-style-type: none"> The datasheet report enables the user to understand the operating parameters of the FPGA for use in system-level integration. The Report Datasheet dialog box allows you to customize the report as per requirement. You can write the results to a file for later use. You can also sort the results by clock name or port name.
<ul style="list-style-type: none"> Review the General Information section in the generated datasheet report. 	<ul style="list-style-type: none"> The General Information section provides details of the design, tool environment, Vivado version, and equivalent Tcl command.
<ul style="list-style-type: none"> Review the Input Ports Setup/Hold section in the generated datasheet report. 	<ul style="list-style-type: none"> The section reports the worst-case setup and hold requirements for each input port with respect to the reference clock. The capture clock which is used to capture the input data is also reported in this report.
<ul style="list-style-type: none"> Review the Output Ports Clock-to-out section. 	<ul style="list-style-type: none"> This section reports worst-case maximum and minimum clock-to-output port delays for each output port with respect to the reference clock. The launch clock which is used to launch the output data is also reported.
<ul style="list-style-type: none"> Review the Setup between Clocks section. 	<ul style="list-style-type: none"> This section reports worst-case setup requirements for all clock edge combinations for every clock pair.
<ul style="list-style-type: none"> Review the Setup/Hold for Input Buses section 	<ul style="list-style-type: none"> This section reports worst-case setup and hold requirements for input bus. The worst-case data window for the entire input bus is the sum of largest setup and hold values. If the input ports are constrained than the slack is also reported.

Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> Review the Max/Min Delays for Output Buses section. 	<ul style="list-style-type: none"> This section reports the worst-case maximum and minimum clock to out delays for entire output bus. The bus skew is also reported which is calculated as follows. <ul style="list-style-type: none"> One bit is considered as the reference and offset of every other bit is calculated with respect to the reference bit. The worst offset is the skew for entire bus.
<ul style="list-style-type: none"> Close the datasheet report and the implemented design. 	
<ul style="list-style-type: none"> Close the Vivado Design Suite. 	

Summary

Here you learned how to use the Report Datasheet function to analyze making I/O constraints in the design.

References:

- Supporting materials
 - Vivado Design Suite User Guide: Design Analysis and Closure Techniques* (UG906)