

System-Synchronous I/O Timing Demo Script

Introduction

This demonstration provides high-level instructions on the proper use of the Timing Constraints Wizard when making SDR and DDR I/O timing constraints.

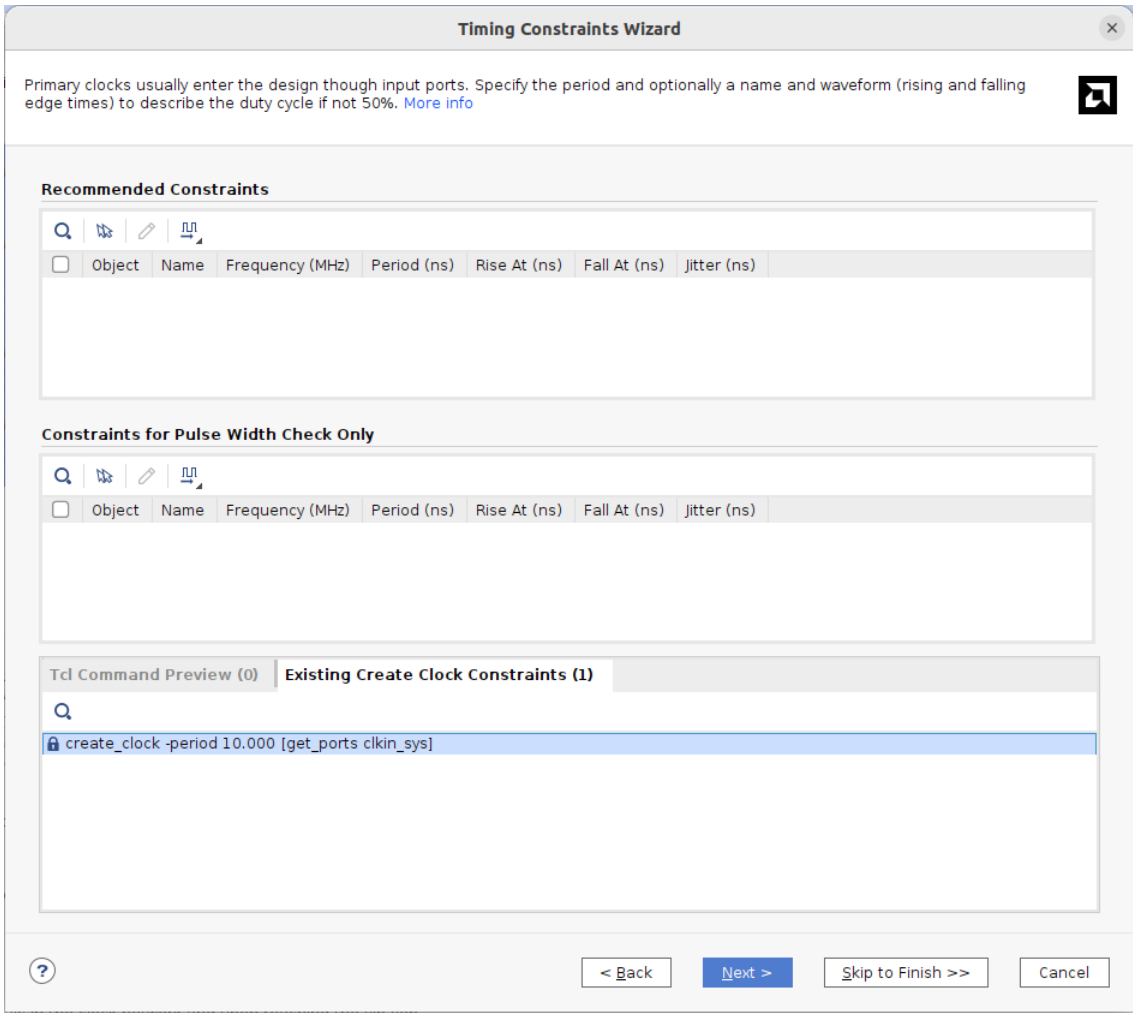
Preparation:

- Necessary project files are located in the following directory:
`$TRAINING_PATH/SystemSyncIO/demo/KCU105/vhdl`
- Required hardware: None
- Supporting materials:
`$TRAINING_PATH/SystemSyncIO/demo/KCU105/vhdl/reference`

System-Synchronous I/O Timing

Action with Description	Point of Emphasis and Key Takeaway
<i>Explore the design and walk through the I/O paths to be constrained.</i>	
<ul style="list-style-type: none"> Launch the Vivado™ Design Suite. Unzip the project using the Tcl Console: <pre>exec unzip \$:env(TRAINING_PATH)/SystemSyncIO/demo/KCU105/vhdl.zip -d \$:env(TRAINING_PATH)/SystemSyncIO/demo/KCU105/vhdl</pre> Open the sys_sync_io project available in the following directory: <code>\$TRAINING_PATH/SystemSyncIO/demo/KCU105/vhdl</code> Open the synthesized design and press <F4> to bring up the schematic. Notice the SDR and DDR input and output ports which describe the typical system-synchronous waveform. Notice the clock and data paths. Close the synthesized design. 	<ul style="list-style-type: none"> Before specifying I/O timing constraints, the user will need to understand the interfaces and identify the I/O timing case so as to choose the appropriate XDC/Wizard timing template. How will the use of MMCM help in system-synchronous I/O timing? <ul style="list-style-type: none"> Reduces clock path delay and also avoids PVT variations in clock path delays. Gives better timing margins and enables higher system clock frequencies. The MMCM negative delay to the clock will provide a better hold margin for the input of the data; for the outputs it minimizes the clock-to-out delay.

Action with Description	Point of Emphasis and Key Takeaway
<i>Apply I/O timing constraints using the Constraints Wizard.</i>	
<ul style="list-style-type: none"> Open sys_sync_io_timing.xdc. Comment out all the existing timing constraints. <ul style="list-style-type: none"> Select all lines and comment them out in the Vivado IDE editor and save the file. From the Flow Navigator, select Open Synthesized Design > Constraints Wizard. When prompted that synthesis is out-of-date, proceed to open the design by selecting Open Design. 	<ul style="list-style-type: none"> The Constraints Wizard will only show the unconstrained I/Os and clocks; it does not show existing constraints and you cannot modify existing constraints through the wizard.
<ul style="list-style-type: none"> Once the initial window of the Constraints Wizard opens, introduce the capabilities of the wizard. Select Define target in the No Target Constraints File dialog box. Select <i>sys_sync_io_timing.xdc</i> and click OK. Click the Constraints Wizard again. Click Next. 	<ul style="list-style-type: none"> The Constraints Wizard helps the user identify missing constraints.
<ul style="list-style-type: none"> The Constraints Wizard has detected that the primary clock is already defined. Where does it come from? Examine the XDC under IP sources if you wish. Click Next. 	<ul style="list-style-type: none"> The native XDC of the MMCM IP defines the clock.

Action with Description	Point of Emphasis and Key Takeaway
<div data-bbox="243 319 1369 1325">  </div> <ul style="list-style-type: none"> Click Next with each of the following pages until you see the Input Delays page. <ul style="list-style-type: none"> Generated clocks. Forwarded clocks. External Feedback delays. 	<ul style="list-style-type: none"> Since MMCM output clocks have been generated automatically (as can be seen with report_clocks), they are not shown in the Constraints Wizard. Only for the cases where the Vivado Design Suite cannot derive the generated clocks does it need manual specification.
<p>Note: While this design has three inputs and three outputs that can be constrained, you may select a few depending on your preference. Deselect the paths you would not want to constrain by unchecking. The demo below shows the steps for all the I/O paths.</p> <p>Ensure that the System is selected under the Synchronous column as it is a system-synchronous interface. The Data Rate and Edge column should have the appropriate value depending on the interface (Rise, Fall, or Dual).</p>	

Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> Click the Schematic icon to view the schematic of the selected port and observe the data path and clock path. Enter the rising edge SDR input delay for din_sys_re as follows: <ul style="list-style-type: none"> Clock = 10 ns Tco_min = 1.9 ns Tco_max = 3.1 ns trce_dly_min = 0.2 ns trce_dly_max = 0.5 ns 	

Timing Constraints Wizard

Input delays describe relative phase between reference clocks (usually board clocks) and input signals at the FPGA boundary. Inaccurate input delay values can make timing fail and affect implementation quality of results. [More info](#)

Recommended Constraints

Interface	Clock	Synchronous	Alignment	Data Rate and Edge
<input checked="" type="checkbox"/> din_sys_ddr	clk_in_sys	System	Edge	Dual
<input checked="" type="checkbox"/> din_sys_fe	clk_in_sys	System	Edge	Single Fall
<input checked="" type="checkbox"/> din_sys_re	clk_in_sys	System	Edge	Single Rise

Delay Parameters

Clock period: 10 ns

tco_min: 1.9 ns

tco_max: 3.1 ns

trce_dly_min: 0.2 ns

trce_dly_max: 0.5 ns

Rise Max = tco_max + trce_dly_max
Rise Min = tco_min + trce_dly_min

Tcl Command Preview (0) Existing Set Input Delay Constraints (0) Waveform - System Edge Single Rise

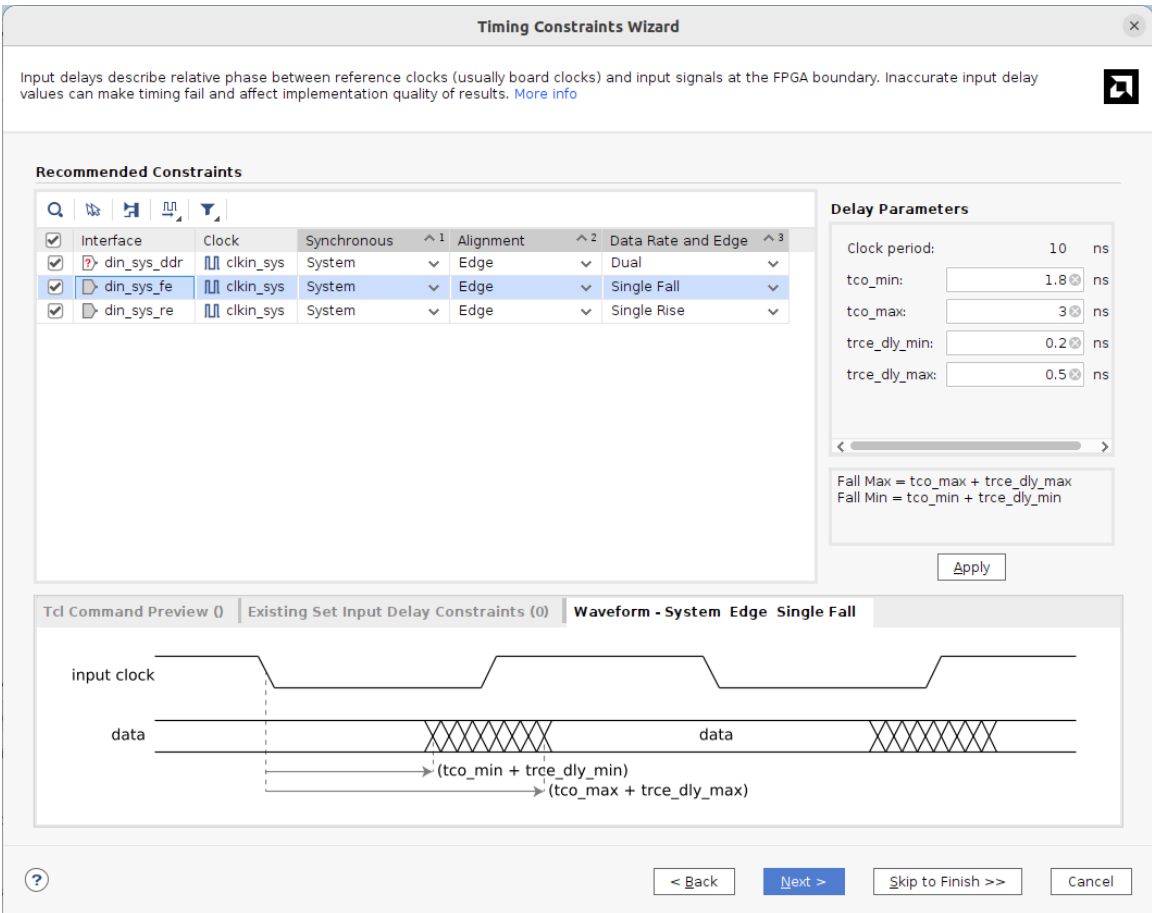
input clock

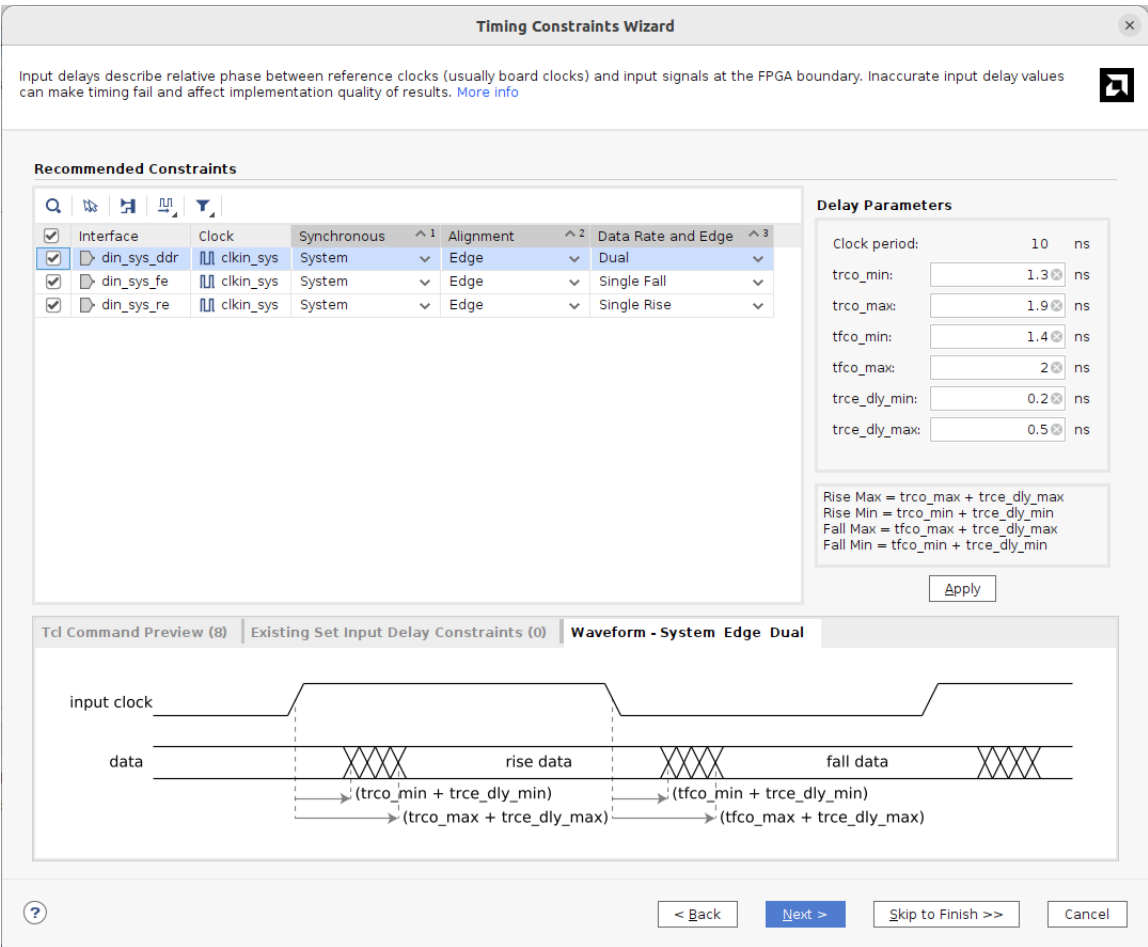
data

(tco_min + trce_dly_min)

(tco_max + trce_dly_max)

< Back Next > Skip to Finish >> Cancel

Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> Enter the falling edge SDR input delay for din_sys_fe as follows: <ul style="list-style-type: none"> Clock = 10 ns Tco_min = 1.8 ns Tco_max = 3 ns trce_dly_min = 0.2 ns trce_dly_max = 0.5 ns 	

Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> Enter the DDR input delay for <code>din_sys_ddr</code> as follows: <ul style="list-style-type: none"> Clock = 10 ns (5 ns/ 5 ns) Trco_min = 1.3 ns Trco_max = 1.9 ns Tfco_min = 1.4 ns Tfco_max = 2 ns trce_dly_min = 0.2 ns trce_dly_max = 0.5 ns 	
<ul style="list-style-type: none"> Click Next after all input delays are specified. This will take you to the Output Delays page. 	<ul style="list-style-type: none"> Ensure that all numbers entered are correct. The Tcl Command Preview tab lists the XDC constraints for all the actions to be performed in the wizard.

Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> Enter the rising edge SDR output delay for dout_sys_re as follows: <ul style="list-style-type: none"> Clock = 10 ns tsu = 1.1 ns thd = 0.9 ns trce_dly_max = 0.5 ns tce_dly_min = 0.2 ns 	

Timing Constraints Wizard

Output delays describe relative phase between reference clocks (usually board or forwarded clocks) and output signals at the FPGA boundary. Inaccurate output delay values can make timing fail and affect implementation quality of results. [More info](#)

Recommended Constraints

Interface	Clock	Synchronous	Alignment	Data Rate and Edge
<input checked="" type="checkbox"/> dout_sys_ddr	clk_sys	System	Setup/Hold	Dual
<input checked="" type="checkbox"/> dout_sys_fe	clk_sys	System	Setup/Hold	Single Fall
<input checked="" type="checkbox"/> dout_sys_re	clk_sys	System	Setup/Hold	Single Rise

Delay Parameters

Clock period: 10 ns
 tsu: 1.1 ns
 thd: 0.9 ns
 trce_dly_max: 0.5 ns
 trce_dly_min: 0.2 ns

Rise Max = trce_dly_max + tsu
 Rise Min = trce_dly_min - thd

Tcl Command Preview (8) Existing Set Output Delay Constraints (0) Waveform - System Setup/Hold Single Rise

destination clock

data

(trce_dly_max + tsu)

(trce_dly_min - thd)

< Back Next > Skip to Finish >> Cancel

Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> Enter the falling edge SDR output delay for dout_sys_fe as follows: <ul style="list-style-type: none"> Clock = 10 ns tsu = 1 ns thd = 0.8 ns trce_dly_max = 0.5 ns tce_dly_min = 0.2 ns 	

Timing Constraints Wizard

Output delays describe relative phase between reference clocks (usually board or forwarded clocks) and output signals at the FPGA boundary. Inaccurate output delay values can make timing fail and affect implementation quality of results. [More info](#)

Recommended Constraints

Interface	Clock	Synchronous	Alignment	Data Rate and Edge
<input checked="" type="checkbox"/> dout_sys_ddr	clkin_sys	System	Setup/Hold	Dual
<input checked="" type="checkbox"/> dout_sys_fe	clkin_sys	System	Setup/Hold	Single Fall
<input checked="" type="checkbox"/> dout_sys_re	clkin_sys	System	Setup/Hold	Single Rise

Delay Parameters

Clock period: 10 ns

tsu: 1 ns

thd: 0.8 ns

trce_dly_max: 0.5 ns

trce_dly_min: 0.2 ns

Fall Max = trce_dly_max + tsu
Fall Min = trce_dly_min - thd

Apply

Tcl Command Preview (8) Existing Set Output Delay Constraints (0) **Waveform - System Setup/Hold Single Fall**

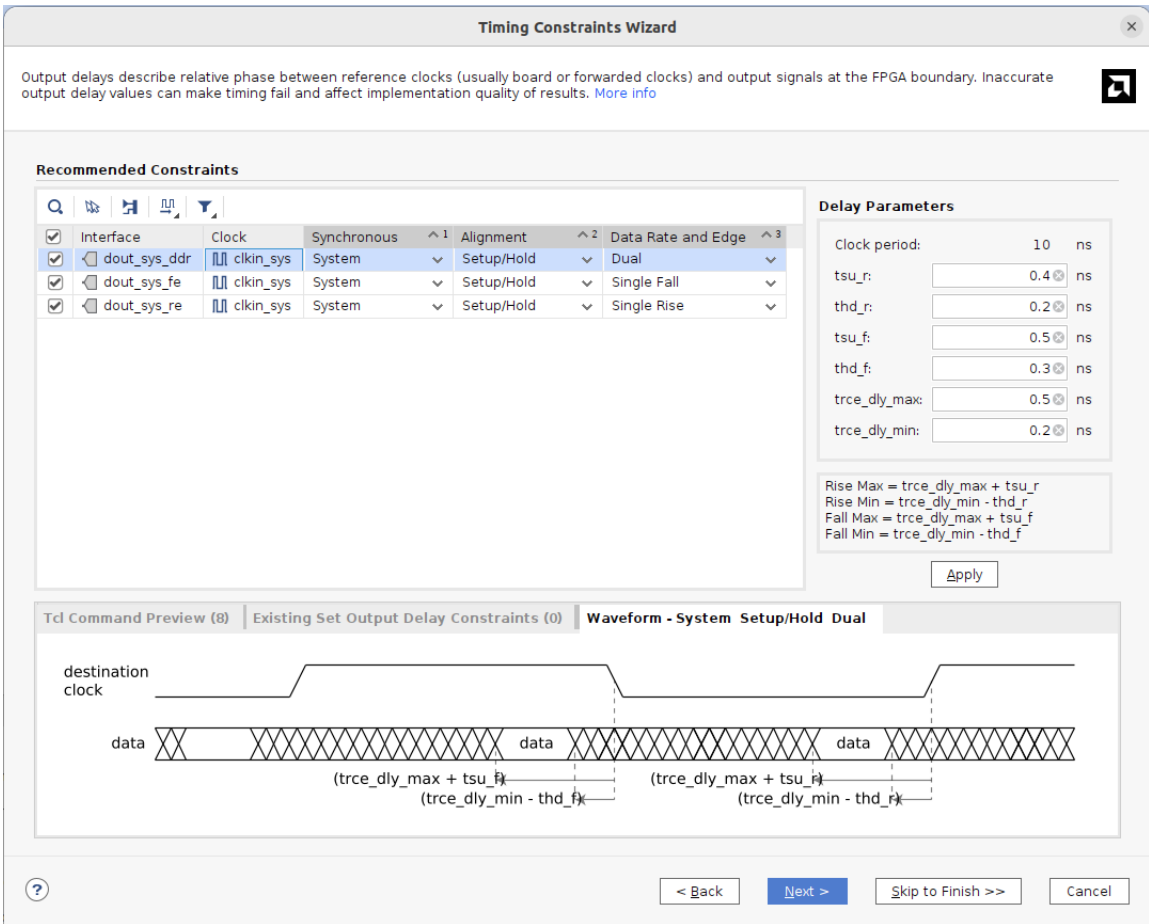
destination clock

data

(trce_dly_max + tsu)

(trce_dly_min - thd)

< Back Next > Skip to Finish >> Cancel

Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> Enter the DDR output delay for dout_sys_ddr as follows: <ul style="list-style-type: none"> Clock = 10 ns tsu_r = 0.4 ns thd_r = 0.2 ns tsu_f = 0.5 ns thd_f = 0.3 ns trce_dly_max = 0.5 ns trce_dly_min = 0.2 ns 	
<ul style="list-style-type: none"> Click Next after all output delays are specified. Click Next for each of the following pages until you reach the Constraints Summary page. 	<ul style="list-style-type: none"> Ensure that all numbers entered are correct. Once Next is clicked, the constraints are applied to the design in memory.

Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> Select all options in the Constraints Summary page and click Finish. 	<ul style="list-style-type: none"> The Constraint Summary page has options that allow you to review and edit the timing constraints, as well as generate the timing and DRC reports. The constraints will be automatically saved to the target XDC file by clicking Finish.
<ul style="list-style-type: none"> Review the wizard-generated timing constraints in the Timing Constraints window. Open (or reload) the sys_sync_io_timing.xdc file and see the appended constraints. 	<ul style="list-style-type: none"> After the wizard is run, the constraints are written to the target XDC file.
<ul style="list-style-type: none"> Review the Check Timing report for any missing input/output delays. Review the post-wizard Timing Summary report. 	<ul style="list-style-type: none"> Are there any missing I/O delays in the design? Are there any timing failures in the design? What is WNS?
<ul style="list-style-type: none"> From the Flow Navigator, click Run Implementation and then click Open Implemented Design. Click Yes to re-run Synthesis before running Implementation. Close the synthesized design if prompted. 	
<ul style="list-style-type: none"> Review the implemented Timing Summary report. 	Is timing met?
<ul style="list-style-type: none"> Close the Vivado Design Suite. 	

Summary

In this demonstration, you first explored a design that needs to be constrained for I/O timing. You used the Constraints Wizard to help you identify the missing constraints in the design and applied the required I/O timing.

After applying the constraints, you implemented the design and analyzed I/O timing. Based on the slacks seen, you also considered options for optimizing the timing for I/O interfaces.