

Zynq UltraScale+ MPSoC Architecture Overview – PS Demo Script

Introduction

This demonstration goes over the configuration of the Zynq™ UltraScale+™ MPSoC processing system (PS) using the Re-customize IP window and how configuration changes can affect the Zynq UltraScale+ PS block in the IP integrator (IPI).

The demonstration also highlights some unique aspects of the Zynq Re-customize IP window and the Zynq PS IP block relative to most other IP blocks representing soft logic cores.

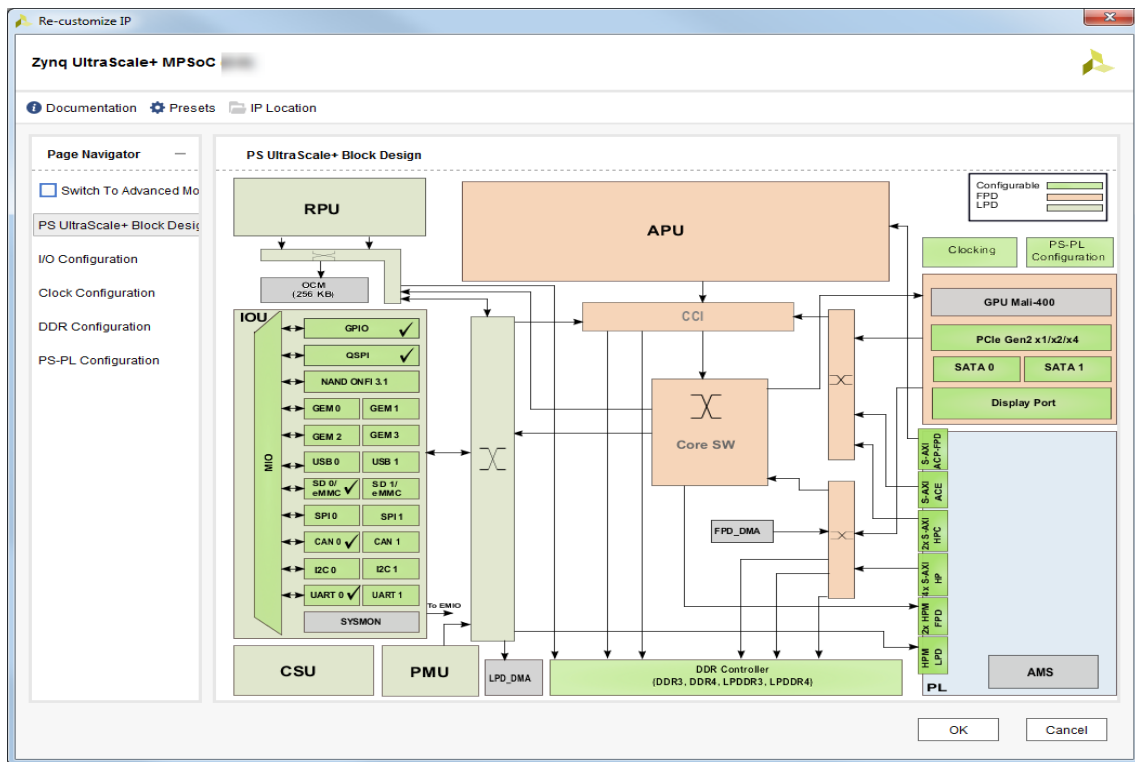
Preparation:

- Required files: None (uses the built-in Vivado™ Design Suite example project)
- Required hardware: None
- Required software: Vivado Design Suite (any edition)

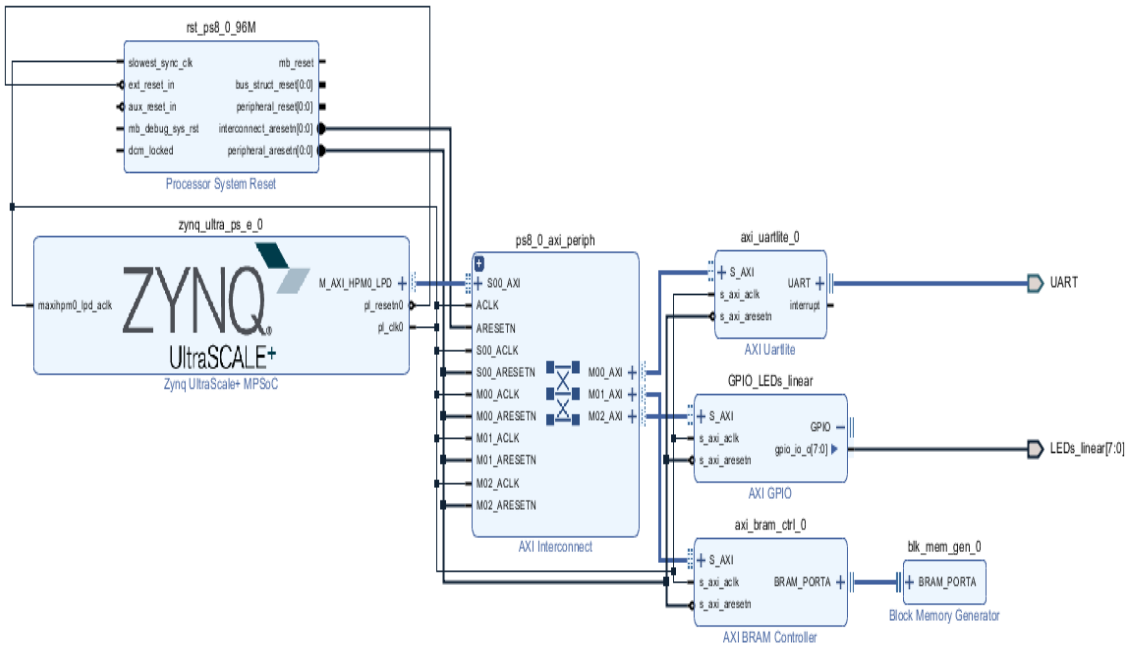
Zynq UltraScale+ MPSoC Architecture Overview – PS

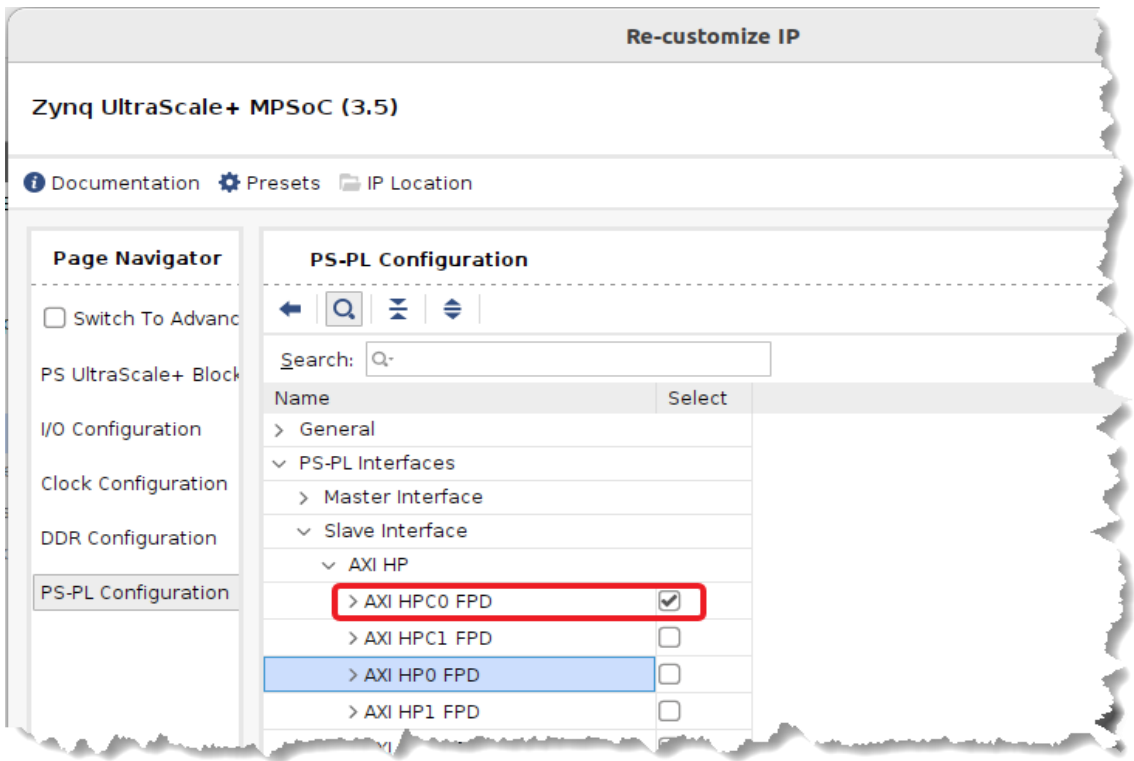
Action with Description	Point of Emphasis and Key Take Away
<ul style="list-style-type: none"> • Click the Vivado icon from the taskbar to launch the Vivado Design Suite. • Execute the script to generate the base design: <ul style="list-style-type: none"> • <code>cd \$::env(TRAINING_PATH) / ArchZynqMPSoC_Overview/support</code> • <code>source createZCU104Design.tcl</code> 	<p>Use a script as a rapid way to generate a new basic design. These scripts can then be reused with each new iteration of the tools to generate updated designs with the latest Vivado Design Suite tools.</p>
<ul style="list-style-type: none"> • Open the IPI block design, maximize its view, and quickly summarize the project. • Ask students to take note of the interfaces available on the ZYNQ UltraScale+ MPSoC block. • In particular, observe the M_AXI_HPM0_FPD, pl_resetrn0, and clock interfaces. 	<p>The Vivado IP integrator is used to create subsystems, including embedded subsystems. These IPI subsystems are referred to as block designs.</p> <p>The project is a basic example of a Zynq UltraScale+ MPSoC-based embedded design that interfaces with block RAM, an AXI Uart and AXI GPIO (LEDs) via the PL.</p>

Action with Description	Point of Emphasis and Key Take Away
<ul style="list-style-type: none"> Double-click the Zynq UltraScale+ MPSoC block to open the Re-customize IP window for the Zynq UltraScale+ MPSoC block. <p>The Zynq UltraScale+ MPSoC Re-customize IP window consists of multiple configuration pages listed on the left in a Page Navigator.</p> <ul style="list-style-type: none"> Identify the green components as configurable within the Re-customize IP window. The light orange components belong to the Full-Power Domain. The darker green belong to the Low-Power Domain. 	<p>The PS is configured and customized like any other IP block except that it represents hard silicon instead of logic in the PL.</p> <p>Most green components also act as shortcuts to the appropriate configuration section.</p>



Action with Description	Point of Emphasis and Key Take Away
<ul style="list-style-type: none"> Click the PS-PL Configuration component (top right) to navigate to the PS-PL Configuration page. <p>The PS-PL Configuration page covers all signals and interfaces available between the PS-PL, including AXI, DMA, interrupts, cross-trigger, and miscellaneous others (grouped under General).</p>	<p>The PS-PL Configuration page allows designers to enable/disable and/or configure interfaces and signals between the PS and PL.</p>
<ul style="list-style-type: none"> Expand all PS-PL Interfaces > Master Interface to show that only one AXI interface is enabled. Indicate the one enabled interface. 	
<ul style="list-style-type: none"> Move the Re-customize IP window out of the way on the desktop such that the IPI block design is visible (see the figure below) and then identify the M_AXI_HPM0_LPD interface on the Zynq UltraScale+ MPSoC block in the IPI diagram. <p>Only one AXI interface is available on the block, consistent with the PS-PL Configuration page.</p> <ul style="list-style-type: none"> Move the Re-customize IP window back to the center of view on the desktop before moving to the next step. 	<p>The Zynq UltraScale+ MPSoC PS block in the IPI only shows enabled interfaces. As a result, the Zynq SoC block representation in IPI dynamically updates to match its configuration.</p>

Action with Description	Point of Emphasis and Key Take Away
 <p>The diagram illustrates the Zynq UltraScale+ MPSoC architecture. It shows the Processor System Reset block (rst_ps8_0_96M) connected to the Zynq UltraScale+ MPSoC block (zynq_ultra_ps_e_0). The Zynq block is connected to the PS-PL Interconnect (ps8_0_axi_periph), which manages the communication between the PS and PL blocks. The interconnect is connected to various peripheral blocks: AXI UARTlite_0 (UART), AXI GPIO (GPIO_LEDs_linear), and AXI BRAM Controller (axi_bram_ctrl_0). The AXI BRAM Controller is connected to the Block Memory Generator (blk_mem_gen_0). The diagram also shows the connection of the Zynq block to the PS-PL Interconnect via the M_AXI_HP0_LPD and M_AXI_HP0_FPD interfaces.</p>	
<ul style="list-style-type: none"> Enable the first HP slave interface (PS-PL Interfaces > Slave Interface > AXI HP > AXI HPC0 FPD). <p>How this affects the Zynq UltraScale+ MPSoC block in the IPI will be shown at the end of this demo when all changes are applied.</p>	<p>The Zynq UltraScale+ MPSoC PS block in the IPI will not update at this point. Changes in the Re-customize IP windows are only applied once the window is closed.</p>

Action with Description	Point of Emphasis and Key Take Away
	
<ul style="list-style-type: none"> Select the I/O Configuration page from the Page Navigator. <p>This page uses drop-down lists to identify which peripherals are mapped to which MIO pins.</p> <p>If a selection is not red, it is an allowable assignment.</p>	<p>The I/O Configuration Pins page allows a designer to identify possible contentions when peripherals are being assigned to MIO pins.</p>
<ul style="list-style-type: none"> Set Low Speed > Processing Unit > TTC > TTC 0 > Clock to MIO6 to demonstrate how a mapping conflict is represented in red. <p>After assigning the clock to the pin, the Clock and Pin should be in red, indicating that there is a conflict found with the current pin assignments.</p> <ul style="list-style-type: none"> Hover the mouse over the pin selection and a tool tip will appear with more information on the conflict. In this case, the other pin is mapped to MIO 6, which is causing the conflict. 	<p>A mapping conflict is shown as a red MIO number.</p> <p>The assignment contention may not be readily visible when nodes are collapsed.</p>

Action with Description	Point of Emphasis and Key Take Away																																																												
<div><div>Re-customize IP</div><div>Zynq UltraScale+ MPSoC (3.5)</div><div><div>Documentation</div><div>Presets</div><div>IP Location</div></div><div><div>Page Navigator</div><div><div>Switch To Advanced</div><div>PS UltraScale+ Block</div><div>I/O Configuration</div><div>Clock Configuration</div><div>DDR Configuration</div><div>PS-PL Configuration</div></div></div><div><div>I/O Configuration</div><div><div>MIO Voltage Standard</div><div>Bank0 [MIO 0:25] Bank1 [MIO 26:51] Bank2 [MIO 52:77] Bank3 [Dedicated]</div><div>LVC MOS18 LVC MOS18 LVC MOS18 LVC MOS33</div></div><div><div>Search: Q-</div><table><tr><th>Peripheral</th><th>I/O</th><th>Signal</th><th>I/O Type</th><th>Drive Strength</th></tr><tr><td><input type="checkbox"/> Clock in</td><td></td><td></td><td></td><td></td></tr><tr><td><input type="checkbox"/> Reset out</td><td></td><td></td><td></td><td></td></tr><tr><td><div><input type="checkbox"/> Trace</div><div>Trace Width</div></td><td></td><td></td><td></td><td></td></tr><tr><td><div><input checked="" type="checkbox"/> TTC</div></td><td></td><td></td><td></td><td></td></tr><tr><td><div><input checked="" type="checkbox"/> TTC 0</div></td><td></td><td></td><td></td><td></td></tr><tr><td><div><input checked="" type="checkbox"/> Clock</div></td><td>MIO 6</td><td></td><td></td><td></td></tr><tr><td><div><input type="checkbox"/> Waveout</div></td><td></td><td></td><td></td><td></td></tr><tr><td><div><input checked="" type="checkbox"/> TTC 1</div></td><td></td><td></td><td></td><td></td></tr><tr><td><div><input type="checkbox"/> Clock</div></td><td></td><td></td><td></td><td></td></tr><tr><td><div><input type="checkbox"/> Waveout</div></td><td></td><td></td><td></td><td></td></tr><tr><td><div><input checked="" type="checkbox"/> TTC 2</div></td><td></td><td></td><td></td><td></td></tr></table></div><div>Validation failed for parameter 'TTC0 CLOCK IO(PSU__TTC0__CLOCK__IO)' with current value 'MIO 6' for BD Cell 'zynq_ultra_ps_e_0'. Conflict from PSS QSPI GRP FBCLK IO and TTC CLOCK 0</div></div></div>		Peripheral	I/O	Signal	I/O Type	Drive Strength	<input type="checkbox"/> Clock in					<input type="checkbox"/> Reset out					<div><input type="checkbox"/> Trace</div> <div>Trace Width</div>					<div><input checked="" type="checkbox"/> TTC</div>					<div><input checked="" type="checkbox"/> TTC 0</div>					<div><input checked="" type="checkbox"/> Clock</div>	MIO 6				<div><input type="checkbox"/> Waveout</div>					<div><input checked="" type="checkbox"/> TTC 1</div>					<div><input type="checkbox"/> Clock</div>					<div><input type="checkbox"/> Waveout</div>					<div><input checked="" type="checkbox"/> TTC 2</div>				
Peripheral	I/O	Signal	I/O Type	Drive Strength																																																									
<input type="checkbox"/> Clock in																																																													
<input type="checkbox"/> Reset out																																																													
<div><input type="checkbox"/> Trace</div> <div>Trace Width</div>																																																													
<div><input checked="" type="checkbox"/> TTC</div>																																																													
<div><input checked="" type="checkbox"/> TTC 0</div>																																																													
<div><input checked="" type="checkbox"/> Clock</div>	MIO 6																																																												
<div><input type="checkbox"/> Waveout</div>																																																													
<div><input checked="" type="checkbox"/> TTC 1</div>																																																													
<div><input type="checkbox"/> Clock</div>																																																													
<div><input type="checkbox"/> Waveout</div>																																																													
<div><input checked="" type="checkbox"/> TTC 2</div>																																																													
<div><ul style="list-style-type: none">Set the TTC 0 Clock back to MIO 14 to remove the conflict.<p>This will remove the conflict and both items should revert to their original black color.</p></div>	<p>MIO assignments can also be disabled or changed from the Peripherals column and the I/O column.</p>																																																												

Action with Description	Point of Emphasis and Key Take Away
<ul style="list-style-type: none"> Select the Clock Configuration page in the Page Navigator. <p>There are two tabs shown, one for Input Clocks, and one for Output Clocks.</p> <ul style="list-style-type: none"> Select the Input Clocks tab. Expand Peripheral Reference Frequency. <p>There is an entry for the TTC0 with an input frequency of 100 MHz. This can be customized here with any value between the allowed range shown in the Range (MHz) column.</p> <p>Any other TTC clocks enabled will also appear in this listing as well as clocks for other peripherals such as watch dog timers.</p> <ul style="list-style-type: none"> Expand Input Reference Frequency and highlight PSS_REF_CLK. <p>Question 1: What does this reference input frequency represent with respect to a demonstration board?</p>	<p>The Clock Configuration page provides access to PLL and clock frequency settings.</p> <ul style="list-style-type: none"> Answer 1: The frequency of an on-board crystal oscillator that feeds the PS and is used to generate all clock signals.
<ul style="list-style-type: none"> Select the Output Clocks tab. Expand PLL Options (under the check box for Enable Manual Mode). <p>Here the source clock can be assigned for each of the available PLLs. The PSS_REF_CLK is currently assigned as the source for all of the PLLs.</p> <p>The Multipliers and Divisors can be manually configured to generate a target output frequency if required.</p> <ul style="list-style-type: none"> Shrink the PLL options. Click the Expand All icon. <p>The frequencies for a wide range of clocks can be configured here from the Low-Power Domain through to the Full-Power Domain clocks and Advanced clocks for Interconnects and DMAs.</p> <p>Question 2: How many PLLs are available in the PS?</p>	<ul style="list-style-type: none"> Answer 2: Five in total identified in the Clock Source column as: <ul style="list-style-type: none"> DPLL - DDR APLL - APU RPLL - RPU IOPLL - I/O VPLL - Video

Action with Description	Point of Emphasis and Key Take Away
<ul style="list-style-type: none"> Focus on the PL Fabric Clocks sub listings. Identify the enabled PL0 clock and recall the same signal being available on the Zynq UltraScale+ MPSoC block in the IPI. 	PL fabric clocks feed clock signals from the PS to the PL.
<ul style="list-style-type: none"> Select the DDR Configuration page in the Page Navigator. <p>Although these can be customized freely, any labs using development boards will always populate this data automatically based on development board description files provided with the Vivado Design Suite.</p>	Typically, this data is auto-populated when a project targets a specific board or when a board preset is selected.
<ul style="list-style-type: none"> Select the PS-PL Configuration page from the Page Navigator. Expand General > Interrupts > PL to PS. Select RPU Legacy Interrupts (IRQ, nFIQ). Click OK. 	The Interrupts page handles the configuration of interrupts from the PS to the PL and vice versa.
<ul style="list-style-type: none"> Observe the updates to the Zynq UltraScale+ MPSoC block in the IPI by applying changes: <ul style="list-style-type: none"> HP slave AXI interface added on the input side. nfiq and nirq inputs added. 	<p>The Zynq UltraScale+ MPSoC block represents the initialized state of the PS at run time (as opposed to its physical state, which is fixed in silicon). The initialized state is the post-FSBL (First Stage Boot Loader) state.</p> <p>Contrast this to blocks that represent IP in the PL. In this case, a block represents a physical implementation.</p> <p>Initialization of the PS comes down to writing values to system-level control registers (SLCRs). This is what the FSBL does based on your IPI configuration. This is possible because SDK auto-generates the FSBL based on the hardware platform exported from the Vivado Design Suite.</p>
<ul style="list-style-type: none"> Close the Re-customize IP window. Close the Vivado Design Suite. 	

Summary

This demonstration illustrated many of the customizable features available for the Zynq UltraScale+ MPSoC processing system using the Re-customization Wizard. Changes made in the Re-customization Wizard are reflected, as applicable, to the graphical representation in the IP integrator.

The Zynq UltraScale+ MPSoC PS is a complex component and, although its initialization involves the configuration of numerous options, the IP Re-customization Wizard provides a convenient and intuitive interface that abstracts users from the complexities of low-level processor initialization.