

Configuring the DDR Controller in a Zynq UltraScale+ MPSoC Demo Script

Introduction

This demonstration will introduce you to the configuration of the DDR controller in the Zynq™ UltraScale+™ MPSoC. This demonstration highlights the use of the DDR Configuration menu in the Re-customize IP dialog box for the Zynq UltraScale+ MPSoC.

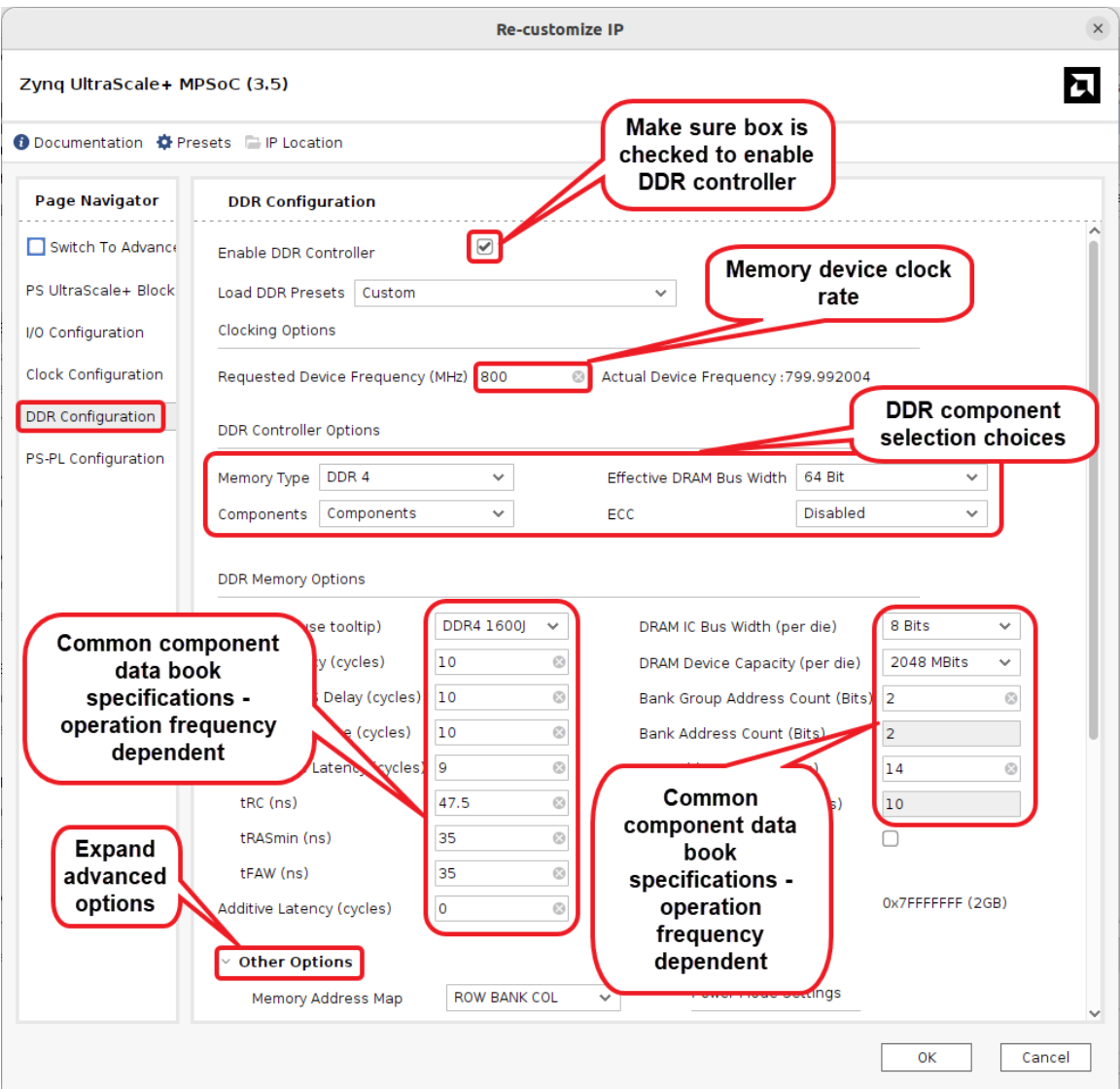
Preparation:

- Required files: None; you will open a blank project in the Vivado™ Design Suite for this demo
- Required software: Vivado Design Suite (any edition)
- Basic background of the DDR controller in the Zynq UltraScale+ MPSoC:
 - *Zynq UltraScale+ MPSoC TRM User Guide* (UG1085)

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Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> • Change the path to the demo directory: <code>[host] \$ cd \$TRAINING_PATH/ MPSoC_DDR/demo</code> 	<ul style="list-style-type: none"> • The <code>demo</code> directory contains all the files required for this demo.
<ul style="list-style-type: none"> • Open the project DDR_Demo.xpr from <code>\$TRAINING_PATH/MPSoC_DDR/demo</code> The Open Project selection provides designers with access to existing projects. 	<ul style="list-style-type: none"> • Use the Open Project option for quick access to existing designs from the specified directory location.

Action with Description	Point of Emphasis and Key Takeaway
	<ul style="list-style-type: none"> Open the IPI block design, maximize its view, and quickly summarize the project. <ul style="list-style-type: none"> The incomplete design consists of a Zynq UltraScale+ MPSoC. The purpose of this demo will be to examine the DDR Configuration menu in the Re-customize IP dialog box for the Zynq UltraScale+ MPSoC.
<ul style="list-style-type: none"> The Vivado IP integrator is used to create subsystems, including embedded subsystems. These IPI subsystems are referred to as block designs. The components of the design are constructed with IP cores from the IP catalog. 	
<ul style="list-style-type: none"> Double-click the Zynq UltraScale+ MPSoC core to open its Re-customize IP dialog box. Focus on the DDR Configuration menu of the Page Navigator. Expand Other Options (bottom left) to view all of the configuration items. Resize the dialog pane by grabbing the lower right-hand corner to fill the screen. Review the properties as shown below. 	<ul style="list-style-type: none"> Introduce the student to the Re-customize IP dialog box for the Zynq UltraScale+ MPSoC. Time and knowledge of the Re-customize IP dialog box for the Zynq UltraScale+ MPSoC permitting, quickly review the other menus in the Page Navigator. Explain the steps being taken to bring the DDR Configuration menu into focus.

Action with Description	Point of Emphasis and Key Takeaway
 <p>Make sure box is checked to enable DDR controller</p> <p>Memory device clock rate</p> <p>DDR component selection choices</p> <p>Common component data book specifications - operation frequency dependent</p> <p>Expand advanced options</p> <p>Common component data book specifications - operation frequency dependent</p>	<p>Common component data book specifications - operation frequency dependent</p> <p>Common component data book specifications - operation frequency dependent</p>

Action with Description	Point of Emphasis and Key Takeaway
<p>DDR controller talking points:</p> <ul style="list-style-type: none"> Make sure to select the Enable DDR Controller option. Set the clock rate for the memory device used. This clock is produced by the DDR PLL (DPLL), which is part of the PS clocking resources. The first group, DDR Controller Options, selects the DDR memory technology, chip topology (bus width and ECC). These selections are based on the DDR component selected and the schematic topology. As you select options in this section, various options in the Advanced Parameters section will be enabled or disabled (grayed out). The DDR Memory Options section is a common configuration area concerned with the size, number, and architecture of the external memory components. These include address sizing (row and column) and number of banks in the DDR RAM. It also concerns itself with DDR timing. This is probably the most important section and most difficult to complete. It is a delicate balance between component speed grade and DDR operating frequency to maximize the performance of the selected component. 	<ul style="list-style-type: none"> DDR system design architecture is not a straightforward topic. The good news is that since all of these parameters can be modified after the fact, problems that arise, such as intermittent operation and reliability issues, can be dealt with. Looking at things this way, the novice DDR system designer can become proficient. Other AMD tools, such as the Zynq UltraScale+ MPSoC and Zynq SoC DDR controllers, and the Memory Interface Generator (MIG), have a selection for preset options based on specific vendors and component part numbers. This eliminates a lot of the decision making as most of the dialog box is automatically filled in.
<p>DDR controller talking points:</p> <ul style="list-style-type: none"> The Other Options section provides the more advanced feature selections of the DDR controller and is beyond the scope of this demo. Direct the student to Chapter 15, "DDR Memory Controller" in the <i>Zynq UltraScale+ MPSoC Technical Reference Manual</i> (UG1085). 	
<ul style="list-style-type: none"> Cancel out of the properties to avoid any inadvertent changes. Select File > Exit to close the project. 	

Summary

This demonstration illustrated the configuration of the DDR controller in the Zynq UltraScale+ MPSoC. The use of the DDR Configuration menu in the Re-customize IP dialog box for the Zynq UltraScale+ MPSoC was highlighted.