

Using XPE to Predict Zynq UltraScale+ MPSoC Power Consumption Demo Script

Introduction

This demonstration illustrates how the Xilinx Power Estimator (XPE) spreadsheet tool can be used to predict power consumption for the Zynq™ UltraScale+™ device family.

The XPE spreadsheet is a power estimation tool typically used in the pre-design and pre-implementation phases of a project. XPE assists with architecture evaluation, device selection, appropriate power supply components, and thermal management components specific for your application. This is a first attempt to gain an understanding of the order of magnitude of the power that the device will consume and is based on best guesses of how the silicon will be utilized by the designer.

The Xilinx Power Analyzer tool provides a much better estimate on power consumption; however, considerably more effort needs to be made in terms of actually building both the hardware and software.

Preparation:

- OS limitations: This demo can only be run on Windows because of the need for Microsoft Excel to be installed.
- Required files: Follow the instructions below to download the XPE spreadsheet.
- Required hardware: None
- Supporting materials: *Xilinx Power Estimator User Guide* (UG440)

Using XPE to Predict Zynq UltraScale+ MPSoC Power Consumption

Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> • This demo can only be performed in the Microsoft Windows environment. • Acquire the XPE tool spreadsheet from the following location: https://www.xilinx.com/products/technology/power/xpe.html • Locate the "UltraScale+" device family and download the available version. • Log in with your AMD credentials if asked. 	<ul style="list-style-type: none"> • Students must download from website. • Multiple versions of the XPE are available for most of the SoC and FPGA families. • The Versal™ adaptive SoC is not supported with XPE. Versal devices use the Power Design Manager (PDM) tool. More information is available from the following location: https://www.xilinx.com/products/design-tools/power-design-manager.html

Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> Launch the XPE tool. Double-click the UltraScale_Plus_XPE_<version-number>.xlsm file. Enable macros (or content). 	<ul style="list-style-type: none"> Excel automatically blocks potential security threats that are possible with macros or active content. The functionality of this tool is in this active content so it must be enabled.
<ul style="list-style-type: none"> Introduce the Summary tab and basic settings. <ul style="list-style-type: none"> Device: <ul style="list-style-type: none"> Select the Zynq UltraScale+ MPSoC family. Select the XCZU9EG device. Select the FFVB1156 package. Select the -2L (0.72V) speed grade. Select the Extended temperature grade. Select the Typical process. Environment: <ul style="list-style-type: none"> Leave at the default settings. 	<ul style="list-style-type: none"> Explain the settings: <ul style="list-style-type: none"> Device. Speed grade: A low power speed grade of -2L means the VCCINT is 0.72v. The temperature range is set to Extended (0 -100 degree). Environmental settings enable you to add heat sinks and specify the number of board layers as well as other factors that add to the cooling ability of the device.
<ul style="list-style-type: none"> Note the current level of power consumption. <i>Why is this?</i> 	<ul style="list-style-type: none"> The Summary region within the Summary tab shows the static power consumption. A detailed breakdown of power is shown on the right-hand side of the Summary window.
<ul style="list-style-type: none"> Continue exploring the Summary tab. <ul style="list-style-type: none"> Look at On-Chip Power, which breaks down power consumption by region. 	<ul style="list-style-type: none"> 89% of the power is drawn from the PL static. 6% is from the PS static. 5% other.
<ul style="list-style-type: none"> Look at the Power Supply region. 	<ul style="list-style-type: none"> This shows the amount of current required for each voltage source. When the final approximations are entered, this region can be used to select power supplies; that is, select a switching supply suitable to drive each voltage rail to the total power identified in the corresponding column.

Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> Select the PS tab. <ul style="list-style-type: none"> Notice the organization. Select the user config from the Processing System drop-down list under On-Chip PS Power. For the Inside Processing System block change Dual RPU-R5 from Powered Down to Powered ON. 	<ul style="list-style-type: none"> The total supply current and power for each power rail is on top left. On-chip power requirements on the right are broken into source/power and summaries of the major blocks and their static and dynamic power consumption. This table is fed by the low power domain (LPD) dynamic, I/O power domains, and the full power (FPD) dynamic.
<ul style="list-style-type: none"> Select a clock frequency for the Arm® Cortex®-R5 processor in the LPD (0 MHz). 	<ul style="list-style-type: none"> Note that the dynamic power for the low power domain is now 0 W (top right domain box).
<ul style="list-style-type: none"> Select a clock frequency for the Cortex-R5 processor in the LPD (50 MHz). 	<ul style="list-style-type: none"> Note that the dynamic power for the low power domain changes to 0.007 W.
<ul style="list-style-type: none"> Select a clock frequency for the Cortex-A53 processor in the FPD (300 MHz). 	<ul style="list-style-type: none"> Note that there was no change in power utilization. This is because the FPD is disabled by default.
<ul style="list-style-type: none"> Enable the full power domain and select one APU core. <ul style="list-style-type: none"> Select Powered ON from the drop-down menu. Select 1 from the Number of CPUs Powered On the drop-down list. 	<ul style="list-style-type: none"> Now the FPD entry changes to 0.013 W dynamic and 0.003 W static. This is for a single processor only.
<ul style="list-style-type: none"> Enable all four of the Cortex-A53 processors. <ul style="list-style-type: none"> Select 4 from the Number of CPUs powered ON drop-down list. Enable the L2 cache controller. 	<ul style="list-style-type: none"> The FPD dynamic power draw is now 0.042 W and the static has increased to 0.012 W.
<ul style="list-style-type: none"> Enable the DDR subsystem. <ul style="list-style-type: none"> Select LPDDR3 for the memory mode under the full power dynamic and I/O domain. Select 9 bytes as the data width. Set the clock to 332 MHz. 	<ul style="list-style-type: none"> Using a low power DDR module: <ul style="list-style-type: none"> The DDR I/O and controller now push the on-chip PS power drawn (for all domains) to 0.516 W from 0.158 W.
<ul style="list-style-type: none"> Change the DDR memory mode. <ul style="list-style-type: none"> Select DDR3 as the memory mode. 	<ul style="list-style-type: none"> The on-chip power use is now 0.676 W.

Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none">Select the Graphs tab.	<ul style="list-style-type: none">This page shows various graphs relating to power usage, voltage, and temperature.This page is useful to quickly determine:<ul style="list-style-type: none">Which component is drawing power.The power draw over VCCINT.The static current leakage per voltage supply rail.The power over junction temperature.
<ul style="list-style-type: none">Select the Summary tab.	<ul style="list-style-type: none">The distribution of power is shown on the right side of the Summary section.

Summary

This demonstration showed you how to enter the estimated clock frequencies for the design by using the outline of the design in the Xilinx Power Estimator (XPE) spreadsheet. After entering the information, you reviewed the estimated power of the overall design.

References:

- Xilinx Power Estimator User Guide* (UG440)