

Zynq UltraScale+ MPSoC CSU Features Demo Script

Introduction

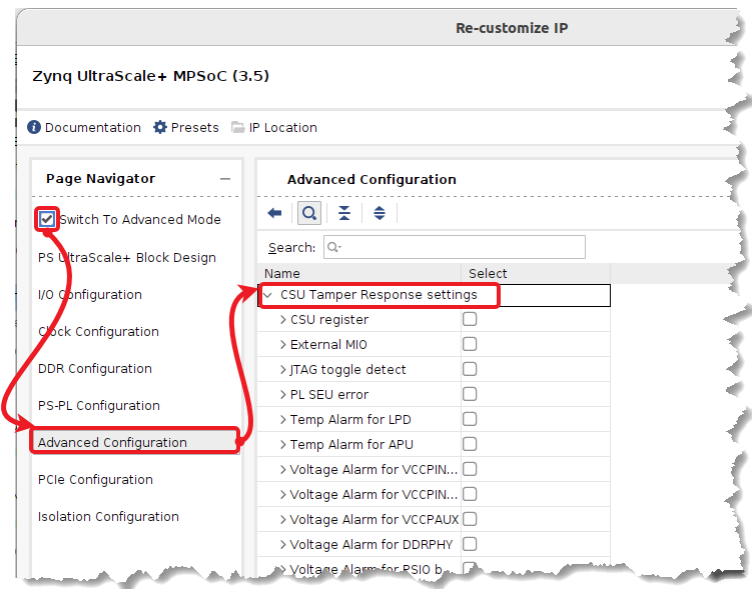
This demonstration provides high-level instructions for configuring the Zynq™ UltraScale™+ MPSoC Configuration Security Unit (CSU). It is designed to be used in conjunction with the "MPSoC Security Features" lecture.

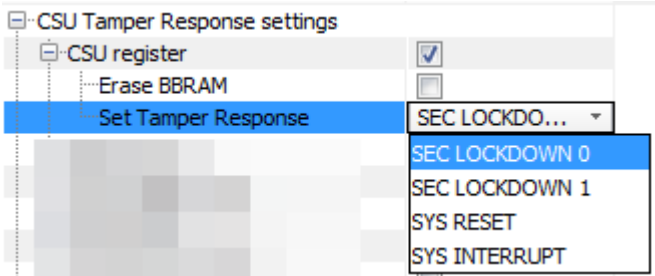
Preparation:

- Required files: None
- Required hardware: None
- Supporting materials:
 - *Zynq UltraScale+ MPSoC Technical Reference Manual (UG1085)*

Zynq UltraScale+ MPSoC CSU Features

Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> • Double-click the Vivado icon from the taskbar to launch the Vivado Design Suite. 	
Create a new project targeting the ZCU104 board called CSU_demo in the \$TRAINING_PATH/MPSoC_Security_Features/demo directory.	
<ul style="list-style-type: none"> • Create a new block design. • Name the block design <i>CSU_demo</i>. 	<ul style="list-style-type: none"> • A block design lets the user place and connect IP blocks into a working design. • Multiple block designs can be made in the same project.
<ul style="list-style-type: none"> • Click the Add IP icon. • Search for MPSoC. 	<ul style="list-style-type: none"> • Adding IP is how the block design diagram is built-up. • Searching for MPSoC yields one result; that is, the Zynq UltraScale+ MPSoC block.
<ul style="list-style-type: none"> • Add the Zynq UltraScale+ MPSoC block to the diagram. 	<ul style="list-style-type: none"> • The Zynq UltraScale+ MPSoC block can now be reconfigured from the default configuration.
<ul style="list-style-type: none"> • Double-click the placed MPSoC block. 	<ul style="list-style-type: none"> • The Re-customize IP pane will open. • The Re-customize IP pane lets you change PS functions and connections.

Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> In the Re-customize IP pane: <ul style="list-style-type: none"> Select the Switch to Advanced Mode option. Select Advanced Configuration in the Page Navigator. Expand CSU Tamper Response Settings. 	<ul style="list-style-type: none"> The Advanced Mode check box displays the Advanced Configuration tab, which controls CSU behavior, IPI configuration, GT lane configuration, and the Security Configuration tab, which controls XMPU and XPPU memory protection. The CSU is responsible for loading the processing system (PS) First Stage Boot Loader (FSBL) code into the on-chip RAM (OCM) in both secure and non-secure boot modes. You can select through the boot header to execute the FSBL on the Arm® Cortex®-R5 or Cortex-A53 processor. After FSBL execution starts, the CSU enters the post-configuration stage, which is responsible for the system tamper response.
	
<ul style="list-style-type: none"> Select and expand the CSU Registers section. Enable the CSU register. 	<ul style="list-style-type: none"> The possible responses for each entry are the same. Setting bits in this CSU register causes the CSU ROM to issue a system interrupt when the tamper event occurs.

Action with Description	Point of Emphasis and Key Takeaway
	
<ul style="list-style-type: none"> Close the Re-customize IP pane. 	
<ul style="list-style-type: none"> Close the Vivado Design Suite GUI. 	

Summary

This demonstration showed you how to configure the CSU.

References:

- Supporting materials:
 - Zynq UltraScale+ MPSoC Technical Reference Manual (UG1085)*